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STANDARDS PUBLICATION NO. TS 2

Traffic Controller Assemblies

NEMA

NATIONAL ELECTRICAL MANUFACTURERS ASSOCIATION ● 2101 L STREET, N.W., WASHINGTON, D.C. 20037

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NEMA STANDARDS PUBLICATIONS NO. TS 2-1992
TRAFFIC CONTROLLER ASSEMBLIES

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Foreword

This NEMA Standards Publication TS 2-1992, *Traffic Controller Assemblies*, identified as Suggested Standards for Future Design, has been developed as a design guide for traffic signaling equipment which can be safely installed and provide operational features not covered by the NEMA TS 1-1989 *Traffic Control Systems*. Within the standard, any reference to a specific manufacture is made strictly for the purpose of defining interchangeability where there exists no nationally recognized standard covering all the requirements. The manufacturer references do not constitute a preference.

As a Suggested Standard for Future Design, the requirements may not have been regularly applied to a commercial product, but suggest a sound engineering approach to future development. The TS 2 Standards Publication has been promulgated to reduce hazards to persons and property when traffic signaling equipment is properly selected and installed in conformance with the requirements herein.

The user's attention is called to the possibility that compliance with this standard may require use of an invention covered by patent rights. By publication of this standard, no position is taken with respect to the validity of this claim or of any patent rights in connection therewith.

Comments and suggestions for the improvement of this document are encouraged. They should be sent to:

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Scope

This Standards Publication covers traffic signaling equipment used to facilitate and expedite the safe movement of pedestrians and vehicular traffic.

Two approaches to expansion of traffic features of NEMA TS 1, *Traffic Control Systems* are provided:

Type 1—

- Entirely new performance oriented standard.

Type 2—

- Use of the MSA, B, and C connectors in common use with NEMA TS 1 equipment.

The Type 1 approach embraces:

- Controller Unit
    - Display-alphanumeric display–32 characters, 2 lines minimum
    - Port 1 Connector
        - High speed full duplex data channel connecting controller unit, conflict monitor (malfunction management unit), rear panel (terminals and facilities) and detectors.
        - All data exchange with rear panel.
        - Controller unit and conflict monitor exchange information on a regular basis, performing redundant checks on each other. Controller unit has access to all conflict monitor internal information, making enhanced event logging, remote intersection monitoring and remote diagnostics feasible.
        - All detector information, including detector diagnostics.
        - EIA-485 serial communications interface with noise immunity characteristics.
        - SDLC (synchronous data link) communication protocol with a bit rate of 153, 600 bits/second, utilizing sophisticated error checking.
        - Vast reduction in number of wires in the cabinet.
    - Port 2 Connector
        - EIA-232C connector.
        - Interface to personal computer.
        - Interface to printer.

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- Port 3 Connector
    - 1200 baud, FSK serial port for on-street communications.
- Standard Features
    - Actuated control.
    - Conditional service.
    - Additional detectors.
    - Delay/extension/switching detectors.
    - Dual entry.
    - Alternate phase sequences.
    - Start-up flash.
    - Automatic flash.
    - Dimming.
    - Coordination: 16 timing plans; one cycle length per timing plan; one split per timing plan; three offset per timing plan.
    - Preemption: six inputs; six sequences.
    - Time base: yearly clock; daylight savings; and leap year.
    - Internal diagnostics: memory diagnostics; processor monitoring; conflict monitoring checking; and detector diagnostics.

- Conflict Monitor (Malfunction Management Unit)
    - Single Type - configurable as 12 four-input channels or 16 three-input channels
    - Port 1 Connector
        - Communications with controller unit, as described above.
        - MSA, MSB connectors downward compatible with those on a TS 1 conflict monitor. Used primarily for sensing of voltages on field terminals.
        - Low voltage monitoring-monitor will be the first unit in a cabinet to sense a low voltage condition and will put

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intersection in flash in an orderly manner. This sequence will be reversed on power up.

- Detectors
    - Rack mounted, 16 detector channels per rack, up to four racks.
    - Port 1 connector: Pluggable, interchangeable Bus Interface unit to convert Port 1 high speed serial data to format required by individual detectors.
    - Communications with controller unit, as described above.
    - Per channel diagnostic data: Open loop; shorted loop; excessive inductance change; and watchdog failure.
    - Detector reset capability.
    - Operation from either 12 volt or 24 volt DC power supply.

- Rear Panel (Terminals and Facilities)
    - Conventional load switches, flasher, flash transfer relays.
    - Termination points for needed functions.
    - Port 1 connector: communications with controller unit, as described above, and pluggable, interchangeable Bus Interface Unit to convert Port 1 high speed serial data to format required by rear panel.

The TS 2 Type 2 is the same as the Type 1 with the following exceptions:

- The MSA, MSB, and MSC connectors for the Controller Unit are compatible with equipment conforming with the NEMA TS 1-1989 Standards Publication.

- MS connector pin-outs are configurable to one of eight modes to satisfy different applications and achieve different functionality. Default mode is pin conpatible with TS 1-1989.

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History

This Standards Publication is predicated upon an industry perceived need to overcome limitations of the NEMA Standards Publication TS 1 for *Traffic Control Systems* which in 1976 reflected the first industry documentation of technically adequate and safe traffic control equipment.

The NEMA TS 1 as subsequently revised and expanded and re-affirmed in 1989:

1. Defined effective actuated intersection control.
2. As a complete package defined all equipment within the cabinet and test procedures.
3. Provided equipment interchangeability between manufacturers.
4. As a minimum functional standard facilitated design innovations.

Limitations inherent in NEMA TS 1 were seen as follows:

1. Reliance on point-to-point wire connection for all functions with termination points for all wires, many of which are not utilized.
   a. Numerous connections increase failure potential
   b. Not cost effective
   c. Hardware limited expandability
2. Out-of-date technology.
3. Lack of uniformity in the implementation of the following functions and the resulting loss in equipment interchangeability:
   a. Coordination
   b. Time base control
   c. Preemption
   d. Uniform Code flash
   e. Communications
   f. Diagnostics
   g. User interface

The following industry guidelines were established to overcome the limitations in the NEMA TS 1 Standards Publication:

1. Equipment requirements based on valid engineering concepts.
2. Interchangeability, performance oriented, without precluding downward compatibility with TS 1 equipment.
3. Emphasis on use of enhanced diagnostic techniques.
4. Minimize potential for malfunctions.
5. Provide for future expandability.
6. Enhanced user interface.

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Four basic proposals were considered over a four-year period. These were:

1. Standardize the functions being provided on the MSD connector.

2. Free up seldom used pins on the MSA, MSB, and MSC connectors and reassign them to needed functions.

3. Develop an entirely new, performance oriented standard.

4. Proceed with Proposal 1, then move on to Proposal 3 for a long-term solution.

During the investigations, involving debate within the industry and inputs received from traffic engineers, and those responsible for the selection, installation and maintenance of traffic control equipment actions were taken on each proposal.

Industry debate of which approach to follow consumed approximately 2.5 years before approval of Proposal 3–proceed with the development of an entirely new, performance oriented standard. While the majority of the industry tended to favor this proposal, some members in opposition had concerns, many of which were valid, and each was carefully studied and evaluated, including joint consultations with delegations from the Institute of Transportation Engineers (ITE) and the International Municipal Signal Association (IMSA), as well as at NEMA sponsored open forums at Annual Meetings of ITE.

The advantages of a new performance oriented standard were identified as:

1. Communication between major equipment within the cabinet over a data channel with virtually unlimited capacity. Potential for future expandability is thereby maximized.

2. Use of a high speed data channel between the controller unit, malfunction management unit, detectors and rear panel reduces the number of connections and facilitates diagnostic testing, thereby reducing the potential for malfunction.

3. Cost effectiveness of communications protocols.

4. Enhanced user interface.

During the development of the new NEMA Standards Publication TS 2 two approaches evolved:

Type 1 which utilizes a high speed data channel between all major equipment to maximize the functionality andexpandability.

Type 2 which retains the MSA, MSB, and MSC connectors for data exchange with the rear panel, providing a degree of downward compatibility.

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SECTION 1
DEFINITIONS

These definitions reflect the consensus of the traffic control equipment industry as represented by NEMA and are intended to be in harmony with terminology in current usage, such as is published in the "Manual on Uniform Traffic Control Devices" and various technical reports of the Institute of Transportation Engineers, 525 School Street, S.W., Washington, D.C. 20024.

1.1 CONTROL EQUIPMENT

The abbreviations used in this Standard Publication are defined as follows:

AC - Alternating Current
BIU - Bus Interface Unit
CA - Controller Assembly
CU - Controller Unit
MMU - Malfunction Management Unit
TF - Terminals and Facilities

1.1.1 Auxiliary Equipment

Separate devices used to add supplementary features to a controller assembly.

1.1.2 Barrier

See 3.5.1.2.

1.1.3 Cabinet

An outdoor enclosure for housing the controller unit and associated equipment.

1.1.4 Call

A registration of a demand for right-of-way by traffic (vehicles or pedestrians) to a controller unit.

1.1.4.1 SERVICEABLE CONFLICTING CALL

A call which:

1. Occurs on a conflicting phase not having the right-of-way at the time the call is placed.
2. Occurs on a conflicting phase which is capable of responding to a call.
3. When occuring on a conflicting phase operating in an occupancy mode, remains present until given its right-of-way.

1.1.5 Check

An output from a controller unit that indicates the existence of unanswered call(s).

1.1.6 Connector

A device enabling outgoing and incoming electrical circuits to be connected and disconnected without the necessity of installing and removing individual wires leading from the control unit.

1.1.6.1 NOT USED CONNECTIONS

The "Not Used" connector pin terminations are used exclusively to prevent interchangeability with units already in use not in conformance to this publication. These connector pins are not to be internally connected.

1.1.6.2 RESERVED CONNECTIONS

The "Reserved" connector pin terminations are used exclusively for future assignment by NEMA of additional specific input/output functions. The control unit does not recognize any "Reserved" input as valid nor shall it provide a valid output on a "Reserved" output.

1.1.6.3 SPARE CONNECTIONS

The "Spare" connector pin terminations are exclusively for manufacturer specific applications.

A Controller Assembly wired to utilize one of these connections may not be compatible with all manufacturer's control units. (Authorized Engineering Information).

1.1.7 Controller Assembly

A complete electrical device mounted in a cabinet for controlling the operation of a traffic control signal.

1.1.7.1 FLASHER CONTROLLER ASSEMBLY

A complete electrical device for flashing a traffic signal or beacon.

1.1.7.2 FULL-TRAFFIC-ACTUATED CONTROLLER ASSEMBLY

A type of traffic-actuated controller assembly in which means are provided for traffic actuation on all approaches to the intersection.

1.1.7.3 ISOLATED CONTROLLER ASSEMBLY

A controller assembly for operating traffic signals not under master supervision.

1.1.7.4 MASTER CONTROLLER ASSEMBLY

A controller assembly for supervising a system of secondary controller assemblies.

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1.1.7.5 MASTER-SECONDARY CONTROLLER ASSEMBLY

A controller assembly operating traffic signals and providing supervison of other secondary controller assemblies.

1.1.7.6 OCCUPANCY CONTROLLER ASSEMBLY (LANE-OCCUPANCY CONTROLLER OR DEMAND CONTROLLER, AND PRESENCE CONTROLLER)

A traffic-actuated controller which responds to the presence of vehicles within an extended zone of detection.

1.1.7.7 PEDESTRIAN-ACTUATED CONTROLLER ASSEMBLY

A controller assembly in which intervals, such as pedestrian WALK and clearance intervals, can be added to or included in the controller cycle by the actuation of a pedestrian detector.

1.1.7.8 PRETIMED CONTROLLER ASSEMBLY

A controller assembly for the operation of traffic signals with predetermined:

1. Fixed cycle length(s).
2. Fixed interval duration(s).
3. Interval sequence(s).

1.1.7.9 SECONDARY CONTROLLER ASSEMBLY (SLAVE)

A controller assembly which operates traffic signals under the supervision of a master controller assembly.

1.1.7.10 SEMI-TRAFFIC-ACTUATED CONTROLLER ASSEMBLY

A type of traffic-actuated controller assembly in which means are provided for traffic actuation on one or more but not all approaches to the intersection.

1.1.7.11 TRAFFIC-ACTUATED CONTROLLER ASSEMBLY

A controller assembly for supervising the operation of traffic control signals in accordance with the varying demands of traffic as registered with the controller by detectors.

1.1.8 Controller Unit

A controller unit is that portion of a controller assembly that is devoted to the selection and timing of signal displays.

1.1.8.1 DIGITAL CONTROLLER UNIT

A controller unit wherein timing is based upon a defined frequency source such as a 60-hertz alternating current source. (See 1.1.48.3.)

1.1.8.2 MULTI-RING CONTROLLER UNIT

See 3.5.1.3.

1.1.8.3 SINGLE-RING CONTROLLER UNIT

See 3.5.1.4.

1.1.9 Coordination

The control of controller units in a manner to provide a relationship between specific green indications at adjacent intersections in accordance with a time schedule to permit continuous operation of groups of vehicles along the street at a planned speed. (See 1.1.30.)

1.1.10 Coordinator

A device or program/routine which provides coordination.

1.1.11 Cycle

The total time to complete one sequence of signalization around an intersection.

In an actuated controller unit, a complete cycle is dependent on the presence of calls on all phases. In a pretimed controller unit it is a complete sequence of signal indications.

1.1.11.1 CYCLE LENGTH

The time period in seconds required for one complete cycle.

1.1.12 Density

A measure of the concentration of vehicles, stated as the number of vehicles per mile per lane.

1.1.13 Detector

See 1.2.5.

1.1.14 Device

1.1.14.1 ELECTROMECHANICAL DEVICE

A device which is characterized by electrical circuits utilizing relays, step switches, motors, etc.

1.1.14.2 ELECTRONIC DEVICE

A device which is characterized by electrical circuits utilizing vacuum tubes, resistors, capacitors, inductors and which may include electromechanical and solid-state devices.

1.1.14.3 SOLID-STATE DEVICE

A device which is characterized by electrical circuits, the active components of which are semi-conductors, to the exclusion of electromechanical devices or tubes.

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1.1.15 Dial

The cycle timing reference or coordination input activating same. Dial is also frequently used to describe the cycle.

1.1.16 Dwell

See 1.1.42.

1.1.17 EXTENSION, UNIT

The timing interval during the extensible portion which is resettable by each detector actuation. The green interval of the phase may terminate on expiration of the unit extension time.

1.1.18 Entry

1.1.18.1 DUAL ENTRY

See 3.5.1.5.

1.1.18.2 SINGLE ENTRY

See 3.5.1.6.

1.1.19 Flasher

A device used to open and close signal circuits at a repetitive rate.

1.1.20 Force Off

A command to force the termination of the **green** interval. (See 3.4.5.2 and 3.5.4.1.)

1.1.21 Gap Reduction

A feature whereby the "unit extension" or allowed time spacing between successive vehicle actuations on the phase displaying the green in the extensible portion of the interval is reduced.

1.1.22 Hold

A command that retains the existing **Green** interval.

1.1.23 Interconnect

A means of remotely controlling some or all of the functions of a traffic signal.

1.1.24 Interval

The part or parts of the signal cycle during which signal indications do not change.

1.1.24.1 MINIMUM GREEN INTERVAL

The shortest green time of a phase. If a time setting control is designated as "minimum green," the green time shall be not less than that setting.

1.1.24.2 PEDESTRIAN CLEARANCE INTERVAL

The first clearance interval for the pedestrian signal following the pedestrian WALK indication.

1.1.24.3 RED CLEARANCE INTERVAL

A clearance interval which may follow the yellow change interval during which both the terminating phase and the next phase display **Red** signal indications.

1.1.24.4 SEQUENCE, INTERVAL

The order of appearance of signal indications during successive intervals of a cycle.

1.1.24.5 YELLOW CHANGE INTERVAL

The first interval following the green interval in which the signal indication for that phase is yellow.

1.1.25 Manual

1.1.25.1 MANUAL OPERATION

The operation of a controller assembly by means of a hand-operated device(s). A pushbutton is an example of such a device.

1.1.25.2 MANUAL PUSHBUTTON

An auxiliary device for hand operation of a controller assembly.

1.1.26 Maximum Green

The maximum green time with an serviceable opposing actuation, which may start during the initial portion.

1.1.27 Memory

1.1.27.1 DETECTOR MEMORY

The retention of a call for future utilization by the controller assembly.

1.1.27.2 NONLOCKING MEMORY

A mode of actuated-controller-unit operation which does not require detector memory.

1.1.27.3 NON-VOLATILE MEMORY

Read/Write memory that is capable of data retention during periods when AC power is not applied for a minimum period of 30 days.

1.1.27.4 VOLATILE MEMORY

Read/Write memory that loses data when power is removed.

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1.1.27.5 RANDOM ACCESS MEMORY (RAM)

Semiconductor Read/Write volatile memory. Data is lost if power is turned off.

1.1.27.6 READ ONLY MEMORY (ROM)

Read-Only, non-volatile, semiconductor memory manufactured with data content, permanently stored.

1.1.27.7 PROGRAMMABLE READ ONLY MEMORY (PROM)

Read-Only, non-volatile, semiconductor memory that allows a program to reside permanently in a piece of hardware.

1.1.27.8 PROGRAMMABLE READ ONLY MEMORY (EPROM)

Read-Only, non-volatile, semiconductor memory that is erasable (via ultra-violet light) and reprogrammable. (See 1.1.27.6 and 1.1.27.7)

1.1.28 Malfunction Management Unit

A device used to detect and respond to improper and conflicting signals and improper operating voltages in a traffic control system.

1.1.29 Modular Design

A design concept such that functions are sectioned into units which can be readily exchanged with similar units.

1.1.30 Offset

Offset is the time relationship, expressed in seconds or percent of cycle length, determined by the difference between a defined point in the coordinated green and a system reference point.

1.1.31 Omit, Phase (Special Skip, Force Skip)

A command that causes omission of a selected phase.

1.1.32 Overlap

A Green indication that allows traffic movement during the green intervals of and clearance intervals between two or more phases.

1.1.33 Passage Time

The time allowed for a vehicle to travel at a selected speed from the detector to the stop line.

1.1.34 Pattern

A unique set of coordination parameters (cycle value, split values, offset value, and sequence).

1.1.35 Phase

1.1.35.1 TRAFFIC PHASE

Those green, change and clearance intervals in a cycle assigned to any independent movement(s) of traffic.

1.1.35.2 CONFLICTING PHASES

Conflicting phases are two or more traffic phases which will cause interfering traffic movements if operated concurrently.

1.1.35.3 NONCONFLICTING PHASE

Nonconflicting phases are two or more traffic phases which will not cause interfering traffic movements if operated concurrently.

1.1.35.4 PEDESTRIAN PHASE

A traffic phase allocated to pedestrian traffic which may provide a right-of-way pedestrian indication either concurrently with one or more vehicular phases, or to the exclusion of all vehicular phases.

1.1.35.5 PHASE SEQUENCE

A predetermined order in which the phases of a cycle occur.

1.1.35.6 PARENT PHASE

A traffic phase with which a subordinate phase is associated.

1.1.35.7 VEHICULAR PHASE

A vehicular phase is a phase which is allocated to vehicular traffic movement as timed by the controller unit.

1.1.36 Portion

1.1.36.1 EXTENSIBLE PORTION

That portion of the green interval of an actuated phase following the initial portion which may be extended, for example, by traffic actuation.

1.1.36.2 INITIAL PORTION

The first timed portion of the green interval in an actuated controller unit:

1. Fixed Initial Portion: A preset initial portion that does not change.
2. Computed Initial Portion: An initial portion which is traffic adjusted.
3. Maximum Initial Portion: The limit of the computed initial portion.
4. Minimum Initial Portion: (See "Fixed Initial Portion.")

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5. Added Initial Portion: An increment of time added to the minimum initial portion in response to vehicle actuations.

1.1.36.3 INTERVAL PORTION

A discrete subdivision of an interval during which the signals do not change.

1.1.37 Preemption

The transfer of the normal control of signals to a special signal control mode for the purpose of servicing railroad crossings, emergency vehicle passage, mass transit vehicle passage, and other special tasks, the control of which require terminating normal traffic control to provide the priority needs of the special task.

1.1.38 Preemptor, Traffic Controller

A device or program/routine which provides preemption.

1.1.39 Preferred Sequence

See 3.5.1.8.

1.1.40 Progression

The act of various controller units providing specific green indications in accordance with a time schedule to permit continuous operation of groups of vehicles along the street at a planned speed.

1.1.41 Red Indication, Minimum (Red Revert)

Provision within the controller unit to assure a minimum **Red** signal indication in a phase following the **Yellow Change** interval of that phase.

1.1.42 Rest

The interval portion of a phase when present timing requirements have been completed.

1.1.43 Ring

See 3.5.1.1.

1.1.44 Split

The segment of the cycle length allocated to each phase or interval that may occur (expressed in percent or seconds).

In an actuated controller unit, split is the time in the cycle allocated to a phase.

In a pretimed controller unit, split is the time allocated to an interval.

1.1.45 Suppressors

1.1.45.1 SUPPRESSOR, RADIO INTERFERENCE

A device inserted in the power line in the controller assembly (cabinet) that reduces the radio interference.

1.1.45.2 SUPPRESSOR, TRANSIENT

A device which serves to reduce transient over-voltages.

1.1.46 Switch

1.1.46.1 AUTO/MANUAL SWITCH

A device which, when operated, discontinues normal signal operation and permits manual operation.

1.1.46.2 FLASH CONTROL SWITCH

A device which, when operated, discontinues normal signal operation and causes the flashing of any predetermined combination of signal indications.

1.1.46.3 POWER LINE SWITCH (DISCONNECT SWITCH)

A manual switch for disconnecting power to the controller assembly and traffic control signals.

1.1.46.4 RECALL SWITCH

A manual switch which causes the automatic return of the right-of-way to its associated phase.

1.1.46.5 SIGNAL LOAD SWITCH

A device used to switch power to the signal lamps.

1.1.46.6 SIGNAL SHUT-DOWN SWITCH

A manual switch to discontinue the operation of traffic control signals without affecting the power supply to other components in the controller cabinet.

1.1.46.7 TIME BASE CONTROL

A means for the automatic selection of modes of operation of traffic signals in a manner prescribed by a predetermined time schedule.

1.1.47 Terminals, Field

Devices for connecting wires entering the controller assembly.

1.1.48 Timing

1.1.48.1 ANALOG TIMING

Pertaining to a method of timing that measures continuous variables, such as voltage or current.

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1.1.48.2 CONCURRENT TIMING

A mode of controller unit operation whereby a traffic phase can be selected and timed simultaneously and independently with another traffic phase.

1.1.48.3 DIGITAL TIMING

Pertaining to a method of timing that operates by counting discrete units.

1.1.48.4 TIMING PLAN

The Split times for all segments (Phase/Interval) of the coordination cycle.

1.1.50 Yield

A command which permits termination of the green interval. (See 1.1.22.)

1.2 DETECTORS

1.2.1 Actuation

The operation of any type of detector.

1.2.2 Antenna

The radiating or receiving elements utilized in transmitting or receiving electromagnetic waves.

1.2.3 Call

See 1.1.4.

1.2.4 Detection

1.2.4.1 ADVISORY DETECTION

The detection of vehicles on one or more intersection approaches solely for the purpose of modifying the phase sequence and/or length for other approaches to the intersection.

1.2.4.2 PASSAGE DETECTION

The ability of a vehicle detector to detect the passage of a vehicle moving through the zone of detection and to ignore the presence of a vehicle stopped within the zone of detection.

1.2.4.3 PRESENCE DETECTION

The ability of a vehicle detector to sense that a vehicle, whether moving or stopped, has appeared in its zone of detection.

1.2.5 Detector

A device for indicating the presence or passage of vehicles or pedestrians.

1.2.5.1 BIDIRECTIONAL DETECTOR

A detector that is capable of being actuated by vehicles proceeding in either of two directions and of indicating in which of the directions the vehicles were moving.

1.2.5.2 CALLING DETECTOR

A detector that is installed in a selected location to detect vehicles which may not otherwise be detected and whose output may be modified by the controller unit.

1.2.5.3 CLASSIFICATION DETECTOR

A detector that has the capability of differentiating among types of vehicles.

1.2.5.4 DIRECTIONAL DETECTOR

A detector that is capable of being actuated only by vehicles proceeding in one specified direction.

1.2.5.5 EXTENSION DETECTOR

A detector that is arranged to register actuations at the controller unit only during the green interval for that approach so as to extend the green time of the actuating vehicles.

1.2.5.6 INFRARED DETECTOR

A detector that senses radiation in the infrared spectrum.

1.2.5.7 LIGHT-SENSITIVE DETECTOR

A detector that utilizes a light-sensitive device for sensing the passage of an object interrupting a beam of light directed at the sensor.

1.2.5.8 LOOP DETECTOR

A detector that senses a change in inductance of its inductive loop sensor by the passage or presence of a vehicle near the sensor.

1.2.5.9 MAGNETIC DETECTOR

A detector that senses changes in the earth's magnetic field caused by the movement of a vehicle near its sensor.

1.2.5.10 MAGNETOMETER DETECTOR

A detector that measures the difference in the level of the earth's magnetic forces caused by the passage or presence of a vehicle near its sensor.

1.2.5.11 NONDIRECTIONAL DETECTOR

A detector that is capable of being actuated by vehicles proceeding in any direction.

1.2.5.12 PEDESTRIAN DETECTOR

A detector that is responsive to operation by or the presence of a pedestrian.

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1.2.5.13 PNEUMATIC DETECTOR

A pressure-sensitive detector that uses a pneumatic tube as a sensor.

1.2.5.14 PRESSURE-SENSITIVE DETECTOR

A detector that is capable of sensing the pressure of a vehicle passing over the surface of its sensor.

1.2.5.15 RADAR DETECTOR

A detector that is capable of sensing the passage of a vehicle through its field of emitted microwave energy.

1.2.5.16 SYSTEM DETECTOR

Any type of vehicle detector used to obtain representative traffic flow information.

1.2.5.17 SIDE-FIRE DETECTOR

A vehicle detector with its sensor located to one side of the roadway.

1.2.5.18 SOUND-SENSITIVE VEHICLE DETECTOR

A detector that responds to sound waves generated by the passage of a vehicle near the surface of the sensor.

1.2.5.19 ULTRASONIC DETECTOR

A detector that is capable of sensing the passage or presence of a vehicle through its field of emitted ultrasonic energy.

1.2.6 Detector Mode

A term used to describe the operation of a detector channel output when a presence detection occurs.

1. Pulse Mode: Detector produces a short output pulse when detection occurs.
2. Controlled Output: The ability of a detector to produce a pulse that has a predetermined duration regardless of the length of time a vehicle is in the zone of detection.
3. Continuous-Presence Mode: Detector output continues if any vehicle (first or last remaining) remains in the zone of detection.
4. Limited-Presence Mode: Detector output continues for a limited period of time if vehicles remain in zone of detection.

1.2.7 Inductive Loop Detector System

See 6.5.1.2.

1.2.8 Inductive Loop Detector Unit

See 6.5.1.5.

1.2.9 Lead-in Cable

See 6.5.1.7.

1.2.10 Output

1.2.10.1 EXTENSION OUTPUT

The ability of a detector to continue its output for a predetermined length of time after the vehicle has left its zone of detection.

1.2.10.2 DELAYED OUTPUT

The ability of a detector to delay its output for a predetermined length of time after a vehicle has entered its zone of detection.

1.2.11 Probe

The sensor form that is commonly used with a magentometer type detector.

1.2.12 Sensor

The sensing element of a detector.

1.2.13 Vehicle Detector System

See 6.5.1.1.

1.2.14 Zone of Detection (Sensing Zone)

That area of the roadway within which a vehicle will be detected by a vehicle detector system.

1.3 SIGNAL

A device which is electrically operated by a controller assembly and which communicates a prescribed action (or actions) to traffic.

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1.4 CROSS-REFERENCE DEFINITIONS

Other Term	NEMA Term	NEMA No.
All-Red Interval	Red Clearance Interval	1.1.24.3
Control Box	Cabinet	1.1.3
Dispatcher	Controller Unit	1.1.8
Filter	Radio Interference Suppressor	1.1.45
Fire Preemptor	Traffic Controller Preemptor	1.1.38
Fixed Time Controller	Pretimed Controller Assembly	1.1.7.8
Housing	Cabinet	1.1.3
Line Filter	Radio Interference Suppressor	1.1.45
Lock-In	Detector Memory	1.1.27.1
Manual Control	Manual Operation	1.1.25.1
Pad	Pressure-Sensitive Detector	1.2.5.14
Progression	Coordinator	1.1.10
Railroad Preemptors	Traffic Controller Preemptor	1.1.38
Red Revert	Minimum Red Indication	1.1.41
Sequence	Interval Sequence	1.1.24.4
Time Cycle	Cycle	1.1.11
Timer	Controller Unit	1.1.8
Traffic Controllers	Controller Assembly	1.1.7
Traffic Phase	Phase	1.1.35
Treadle	Pressure-Sensitive Detector	1.2.5.14
Vehicle Interval	Unit Extension	1.1.17
Vehicle Interval	Passage Period	1.1.33
Volume-Density Operation	Gap Reduction	1.1.21
Volume-Density Operation	Added Initial Portion	1.1.36.2

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SECTION 2
ENVIRONMENTAL REQUIREMENTS

2.1 ENVIRONMENTAL AND OPERATING STANDARDS

2.1.1 Definitions of Major Units of the Controller Assembly

For the purpose of this clause, "Major units of the Controller Assembly (CA)" shall include the Controller Unit (CU), Malfunction Management Unit (MMU), Bus Interface Units (BIUs), Cabinet Power Supply, Load Switches, Flasher(s), and Detector(s).

2.1.2 Operating Voltage

The voltage range shall be 89 to 135 volts alternating current. The nominal voltage shall be 120 volts alternating current.

2.1.3 Operating Frequency

The operating frequency range shall be 60 hertz ±3.0 hertz.

2.1.4 Power Interruption

A power interruption is defined as 0 volts alternating current.

Two or more power interruptions which are separated by power restorations of 1500 or more milliseconds shall be considered as separate interruptions.

Three interruptions of 300 milliseconds or less which are separated by power restorations of 300 milliseconds or more shall not cause the CA to revert to its start-up state.

Detection of power interruption to the CA will be provided by the Malfunction Management Unit. (Authorized Engineering Information)

2.1.4.1 The CA Field Terminal Outputs shall react to a power interruption, upon restoration of power, as follows:

1. Interruption of 450 Milliseconds or Less: Shall continue to operate as though the power interruption had not occurred.
2. Interruption of More Than 450 Milliseconds and Less than 500 Milliseconds: Shall either continue to operate (2.1.4.1(1)) or shall revert to its start-up state (2.1.4.1(3)).
3. Interruption of 500 Milliseconds or More: Shall revert to its start-up state.

2.1.5 Temperature and Humidity

The CA shall maintain all of their programmed functions when the temperature and humidity ambients are within the specified limits defined herein (2.1.5.1 and 2.1.5.2).

2.1.5.1 AMBIENT TEMPERATURE

The operating ambient temperature range shall be from -34°C (-30°F) to +74°C (+165°F). The storage temperature range shall be from -45°C (-50°F) to +85°C (+185°F).

The rate of change in ambient temperature shall not exceed 17°C (30°F) per hour, during which the relative humidity shall not exceed 95 percent.

2.1.5.2 HUMIDITY

The relative humidity shall not exceed 95 percent non-condensing over the temperature range of +4.4°C (+40°F) to +43.3°C (+110°F).

Above +43.3°C (110°F), constant absolute humidity shall be maintained. This will result in the relative humidities shown in Table 2-1 for dynamic testing.

Table 2-1
WET-BULB DRY-BULB RELATIVE HUMIDITY AT BAROMETRIC PRESSURE OF 29.92 IN. HG.

Dry Bulb		Relative Humidity	Wet Bulb	
°F	°C	Percent*	°F	°C
40	4.4	75	37	2.8
50	10.0	80	47	8.3
60	15.6	83	57	13.9
70	21.1	86	67	19.4
80	26.7	87	77	25.0
90	32.2	89	87	30.6
100	37.8	89	97	36.1
110	43.3	90	107	41.7
120	48.9	70	109	42.8
130	54.4	50	109	42.8
140	60.0	38	109	42.8
150	65.6	28	109	42.8
160	71.1	21	109	42.8
165	73.9	18	109	42.8

* For dynamic testing.

2.1.6 Transients, Power Service

The CA shall maintain all defined functions when the independent test pulse levels specified in 2.1.6.1 and 2.1.6.2 occur on the alternating-current power service.

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2.1.6.1 HIGH-REPETITION NOISE TRANSIENTS

The test pulses shall not exceed the following conditions:

1. Amplitude: 300 volts, both positive and negative polarity.
2. Peak Power: 2500 watts.
3. Repetition: 1 pulse approximately every other cycle moving uniformly over the full wave in order to sweep across 360 degrees of the line cycle once every 3 seconds.
4. Pulse Rise Time: 1 microsecond.
5. Pulse Width: 10 microseconds.

2.1.6.2 LOW-REPETITION HIGH-ENERGY TRANSIENTS

The test pulses shall not exceed the following conditions:

1. Amplitude: 600 volts ± 5 percent, both positive and negative polarity.
2. Energy Source: Capacitor, oil filled, 10 microfarads ± 10 percent, internal surge impedance less than 1 ohm.
3. Repetition: 1 discharge every 10 seconds.
4. Pulse Position: Random across 360 degrees of the line cycle.

2.1.7 Transients, Input-Output Terminals

The CA shall maintain all defined functions, when the test pulse occurs on the input-output terminals.

1. Amplitude: 300 volts, both positive and negative polarity.
2. Pulse Source: 1000 ohms nominal impedance.
3. Repetition: 1 pulse per second, for a minimum of 5 pulses per selected terminal.
4. Pulse rise time: 1 microsecond.
5. Pulse width: 10 microseconds.

2.1.8 Nondestruct Transient Immunity

The CA shall be capable of withstanding a high energy transient having the following characteristics repeatedly applied to the alternating current input terminals (no other power connected to terminals) without failure of the test specimen:

1. Amplitude: 1000 volts ± 5 percent, both positive and negative polarity.
2. Energy Source: Capacitor, oil filled, 15 microfarads ± 10 percent, internal surge impedance less than 1 ohm.
3. Repetition: Applied to the CA once every 2 seconds for a maximum of three applications for each polarity.

After the foregoing, the CA shall perform all defined functions upon the application of nominal alternating current power.

2.1.9 Vibration

The major units of the CA shall maintain their programmed functions and physical integrity when subjected to a vibration of 5 to 30 cycles per second up to 0.5 gravity applied in each of three mutually perpendicular planes.

2.1.10 Shock

The major units of the CA shall suffer neither permanent mechanical deformation nor any damage that renders the unit inoperable, when subjected to a shock of 10 G applied in each of three mutually perpendicular planes.

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SECTION 3
CONTROLLER UNITS

This section defines the physical, interface, and functional requirements of solid state controller units which fully conform to this Standards Publication.

3.1 DEFINITIONS

These definitions define the nomenclature frequently used in this part of the Standard Publication.

3.1.1 CRC (Cyclic Redundancy Check)

An error checking technique where a mathematically derived code follows the transmission of a block of data; the code is recalculated and compared to be sure that the data has not changed during transmission.

3.1.2 Load Switch Driver Group

The set of three outputs which are used to drive load switch inputs to provide a **Green, Yellow,** or **Red** output condition for vehicle signals or **Walk, Ped Clear,** or **Dont Walk** output condition for pedestrian signals.

3.2 PHYSICAL STANDARDS

This standard covers four CU configurations. The configurations are:

Controller Unit	Type 1	Type 2
Actuated	A1	A2
Pretimed	P1	P2

The CU shall conform to these physical requirements:

3.2.1 Dimensions

The CU shall be capable of being shelf mounted. The CU shall also be capable of being mounted in a 19-inch rack (EIA Standard RS-310-C, 1982). The height of the CU shall not exceed 30.48 centimeters (12 inches). The depth of the unit, including connectors, harnesses, and protrusions, shall not exceed 36.83 centimeters (14.5 inches). On rack-mounted units, the mounting flanges of the control unit shall be so placed that no protrusion shall exceed 27.94 centimeters (11 inches) to the rear and 8.89 centimeters (3.5 inches) to the front.

3.2.2 Design

The CU shall be of modular design. Circuit boards shall be readily accessible for maintenance. It shall be permissible to accomplish this by the use of extender boards. All fuses, connectors, and controls shall be accessible from the front of the CU.

3.2.3 Material and Construction of Rigid Printed Circuit Assemblies

3.2.3.1 MATERIALS

All printed circuit boards shall be made from NEMA FR-4 glassepoxy or equivalent (see NEMA LI 1-1989, *Industrial Laminated Thermosetting Products*).

3.2.3.2 MATING SURFACES

All electrical mating surfaces shall be made of noncorrosive material.

3.2.3.3 COMPONENT IDENTIFICATION

The Printed Circuit Assembly shall be so designed that each component is identified with a circuit reference symbol. The identification shall be etched or silkscreened on circuit boards.

3.3 INTERFACE STANDARDS

This standard shall define Types 1 and 2 CUs.

Type A1 and P1 CUs shall utilize an Input/Output Interface conforming to the requirements of Section 3.3.1 for all Input/Output functions with the Terminals and Facilities, Malfunction Management Unit, Detector Rack(s), and Auxiliary Devices.

Type A2 and P2 CUs shall utilize an Input/Output Interface conforming to the requirements of Section 3.3.1 for Input/Output functions with the MMU and Detector Rack(s) and Section 3.3.5 for Input/Output functions with the TF, Detector(s), and Auxiliary Devices.

Type A2 CUs are included for the purpose of upgrading existing TS 1 installations (Authorized Engineering Information).

If input/output terminations in addition to those covered by these standards are required to allow inclusion of additional functional capabilities, such additional input/output terminations shall be provided on an additional connector. Such additional connector shall **not** be interchangeable with other connector(s) on the face of the CU. The provision of these additional functional capabilities shall not modify the operating capabilities of the CU covered by these standards when the additional input/output connector is disconnected.

The CU shall provide an input/output interface to meet the following requirements.

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3.3.1 Port 1 Physical and Protocol

3.3.1.1 CONNECTOR

The Port 1 connector shall be a 15 pin metal shell D subminiature type connector. The connector shall utilize female contacts with 15 millionths of an inch minimum gold plating in the mating area. The connector shall be equipped with latching blocks. The connector shall intermate with a 15 pin D type connector, Amp Incorporated part number 205206-1, or equivalent, which is equipped with spring latches, Amp Incorporated part number 745012-1, or equivalent. Pin connections shall be as follows:

Pin	Function
1	Tx Data +
2	Logic Ground
3	Tx Clock +
4	Logic Ground
5	Rx Data +
6	Logic Ground
7	Rx Clock +
8	Logic Ground
9	Tx Data -
10	Port 1 Disable (0VDC=disable)(*)
11	Tx Clock -
12	Earth Ground
13	Rx Data -
14	Reserved
15	Rx Clock -

* Pin 10 shall be connected to pin 8 when it is desirable to disable all Port 1 communications activity. This shall be accomplished by mating a connector (as described above) to this Port 1 connector, in which pin 8 and pin 10 are connected.

Port 1 shall be utilized to facilitate communications between the CU, the TF, the MMU, and the Detector Rack(s), as defined in this standard. Port 1 may also be used for manufacturer's use. In such instances, conformance with this standard shall be required.

It will be necessary to disable all Port 1 communications activity when a CU meeting the requirements of this standard is installed in a CA that has no accomodation for Port 1, such as a CA meeting the requirements of NEMA Standard TS 1-1989. (Authorized Engineering Information)

3.3.1.2 ELECTRICAL INTERFACE

3.3.1.2.1 Logic Ground and Earth Ground

1. **Logic Ground**—Voltage reference point and current return point for CU input and output logic circuits. This output shall not be connected to **AC Neutral** or **Earth Ground** within the CU.
2. **Earth Ground**—Terminal for connection to the chassis of the CU. **Earth Ground** shall be electrically connected to the shell of the connector(s) where applicable. This input shall not be connected to Logic Ground or AC Neutral within the CU.

3.3.1.2.2 Data and Clock Links

1. **Tx Data+, Tx Data-, Tx Clock+, Tx Clock-, Rx Data+, Rx Data-, Rx Clock+, and Rx Clock-** shall consist of four interface links conforming to the requirements of the Electronic Industries Association EIA-485, Standard for Electrical Characteristics of Generators and Receivers for use in Balanced Digital Multipoint Systems, dated April 1983. Where differences occur between the EIA-485 standard and this standard, this standard shall govern. **Tx Data+** shall be the non-inverting line and **Tx Data-** shall be the inverting line of one link. **Tx Clock+** shall be the non-inverting line and **Tx Clock-** shall be the inverting line of the second link. **Rx Data+** shall be the non-inverting line and **Rx Data-** shall be the inverting line of the third link. **Rx Clock+** shall be the non-inverting line and **Rx Clock-** shall be the inverting line of the fourth link.
2. All voltage potentials on the **Tx Data, Tx Clock, Rx Data,** and **Rx Clock** interface links shall be referenced to logic ground within the CA.
3. The interface links shall be connected within the CA in a full duplex party line configuration, as shown in Figure 3.3.1-1 for a Type 1 CU and Figure 3.3.1-2 for a Type 2 CU. The TF interface shall consist of up to eight identical stations, each as shown. The Detector interface shall consist of up to eight identical stations, each as shown. The **Rx Data** and **Rx Clock** links shall be terminated within the CU with resistors of 120 ohms, plus or minus 5%, connected between the + and - sides of the links, as shown in Figures 3.3.1-1 and 3.3.1-2 (total of two resistors within the CU).
4. Data and Clock Links: Additional Considerations
   a. The **Tx Data, Tx Clock, Rx Data,** and **Rx Clock** link connections within the CA shall utilize the TF as the common connection point. Refer to Section 5.3.3, Port 1 Communications Cables for details.
   b. The **Tx Data** and **Tx Clock** links shall be terminated within the MMU with resistors of 120 ohms, plus or minus 5%, connected between the + and - sides of the links, as shown in Figures 3.3.1-1 and 3.3.1-2 (total of two resistors within the MMU).
   c. The data and clock link connections may be used for purposes not defined in this standard at the manufacturers discretion. In the event that the data and clock link connections are used in this manner, such use shall conform to the requirements of Section 3.3.1.4, Information Field For-

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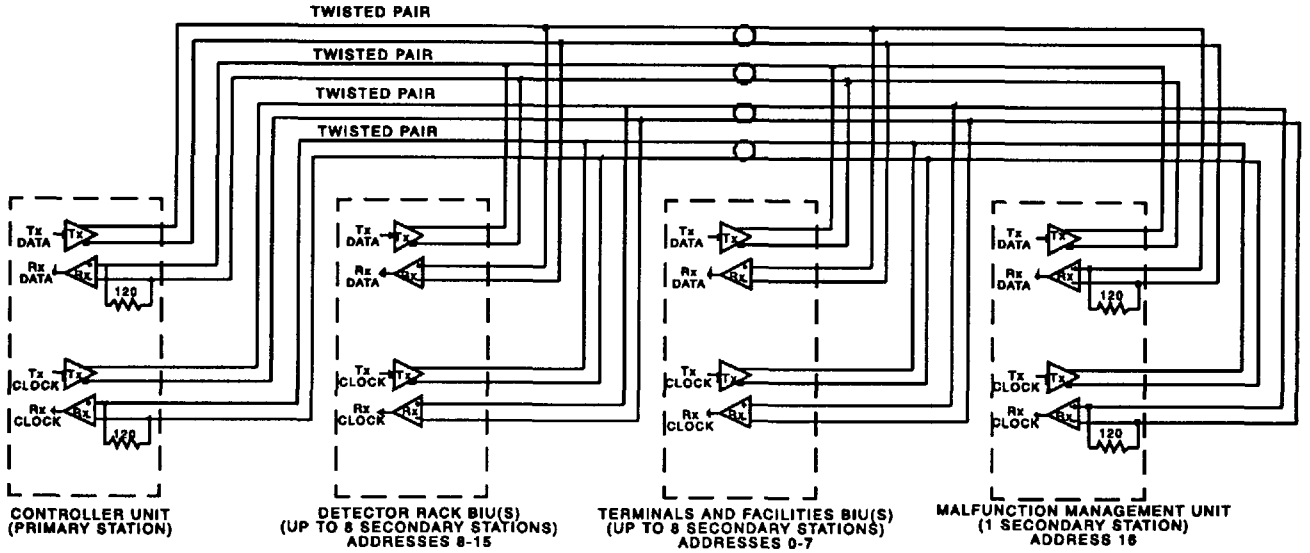

Figure 3.3.1-1
PORT 1 CONNECTIONS, TYPE 1 CONTROLLER ASSEMBLY

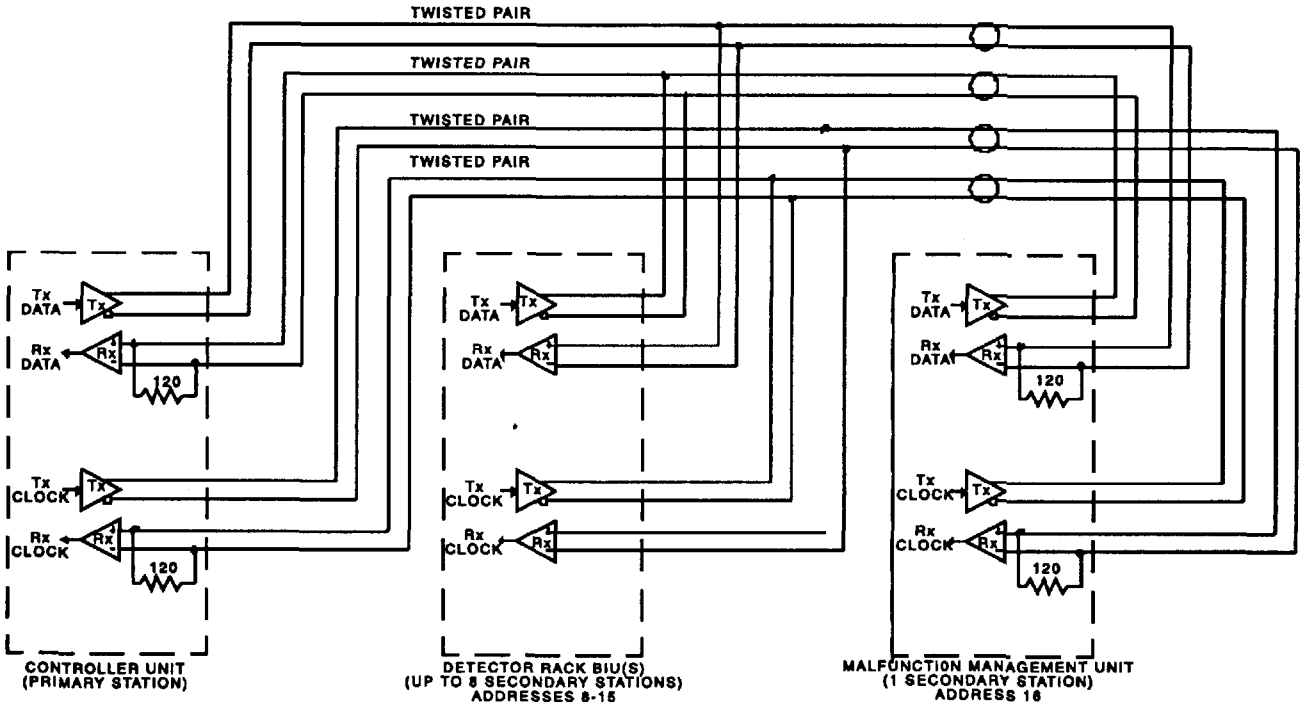

Figure 3.3.1-2
PORT 1 CONNECTIONS, TYPE 2 CONTROLLER ASSEMBLY

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mats, and 3.3.1.5, Frame Timing, of this standard. Further, any auxiliary equipment utilizing the data and clock link connections shall not have terminating resistors connected to these links.

3.3.1.3 DATA AND CLOCK COMMUNICATIONS PROTOCOL

The transfer of data shall take place over the data and clock links by means of the SDLC (Synchronous Data Link Control) Protocol, as defined by International Business Machines Corporation document GA27-3093-3, dated June 1986. Where differences occur between this standard and the IBM document, this standard shall govern.

1. Data shall be transmitted by the sending station on the **Tx Data+** and **Tx Data-** lines. The receiving station shall consider the data to be a binary "1" when the voltage potential of the **Tx Data+** line is more positive than the voltage potential of the **Tx Data-** line. The receiving station shall consider the data to be a binary "0" when the voltage potential of the **Tx Data+** line is more negative than the voltage potential of the **Tx Data-** line.
2. A clocking signal shall be transmitted by the sending station on the **Tx Clock+** and **Tx Clock-** lines. The receiving station shall read the data on the **Tx Data+** and **Tx Data-** lines when the voltage potential of the **Tx Clock+** line makes a positive going transition with respect to the **Tx Clock-** line, as shown in Figure 3.3.1-3.
3. The data transfer rate shall be 153,600 bits per second, plus or minus 1 percent. The width of the bit cell on the Data links shall be the reciprocal of the data transfer rate.
4. The clocking signal from the sending station shall be a square wave with a frequency of 153,600 hertz, plus or minus 1 percent, and shall be synchronous with the data on the Data links. The clocking signal shall make its positive going transition at the midpoint of the bit cell, plus or minus 10 percent of the bit cell width, as measured at the sending station.
5. Only one secondary station shall be sending data at a time, all others shall have their **Tx Data** link outputs and **Tx Clock** link outputs in the high impedance state.
6. The frame format of the data transmitted on the **Tx Data** links shall be as shown in Figure 3.3.1-4.
   a. The frame shall be bounded at the beginning and end by the opening and closing flags, respectively. The hexadecimal representation of these flags shall be 7E(hex).
   b. The address field shall be 8 bits in length. The usage of the address field shall be as shown below:

Address	Usage
0–18	Defined by TS 2
19–127	Reserved for TS 2
128–254	Manufacturers Use
255	Defined by TS 2

The CU shall be the primary station, the MMU shall be secondary station 16 (address=16), the TF shall be secondary stations 0 through 7 (addresses=0 through 7) and the Detectors shall be secondary stations 8 through 15 (addresses=8 through 15). Address 17 shall be used for diagnostic purposes, as described in 3.3.1.4. The CU shall be secondary station 18 (address=18) for the purpose of secondary to secondary messaging, as described in 3.3.1.4.1. When the primary station sends a frame it shall place the address of the station to whom it is sending the frame in the address field. The receiving station shall respond by sending a frame to the primary station with its own address in the address field. Secondary stations shall transmit only in response to a correctly received frame from the primary station. Frames transmitted by the primary station with an address of 255 shall be considered broadcast frames and shall be accepted by all secondary stations. Secondary stations shall not respond to broadcast frames.

Frames transmitted to the TF and to the Detector Racks shall be received by BIUs. There shall be a maximum of eight BIUs at the TF (TF). There shall be a maximum of eight Detector Racks, each having one BIU. There shall be programming means in the CU to identify the BIUs that are present in the CA. The addresses, usages, and descriptions of these BIUs are outlined on page 16:

   c. The control field shall be set to 83(hex) in all frame types.
   d. The information field shall be variable in length, depending on the type of frame being transmitted. The length of the information field shall be a multiple of eight bits.
   e. The CRC field shall be 16 bits in length. The receiving station shall utilize the CRC field for error checking of all received frames. Failure of the CRC check shall result in specific action, as defined in this standard.

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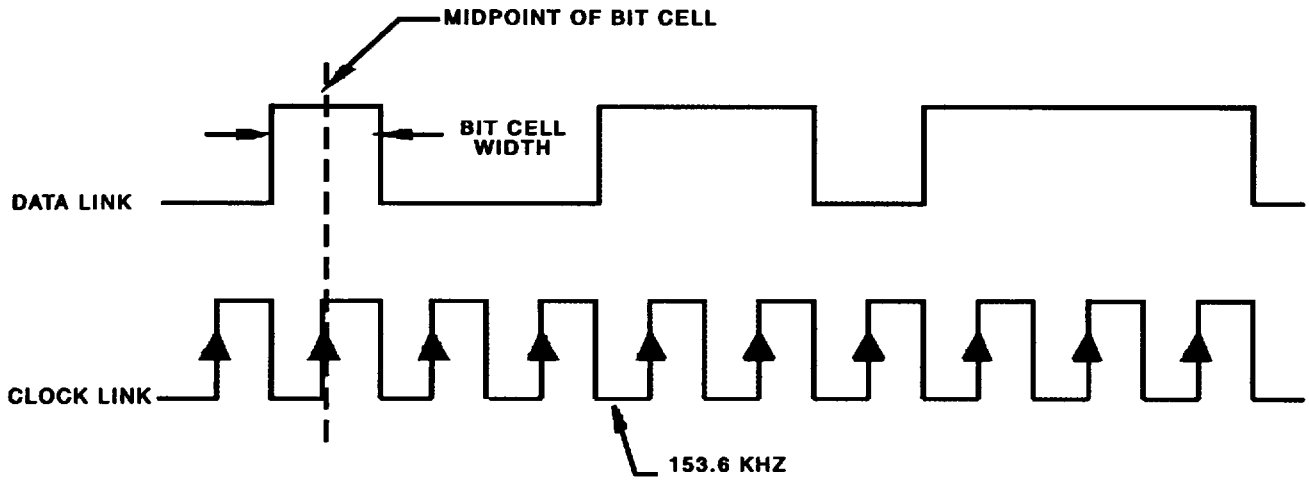

Figure 3.3.1-3
PORT 1 TIMING

OPENING FLAG	ADDRESS	CONTROL	INFORMATION	CRC	CLOSING FLAG
0111 1110	8 BITS	8 BITS	VARIABLE LENGTH	16 BITS	0111 110

Figure 3.3.1-4
PORT 1 FRAME FORMAT

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Address	Usage	Description
0	Defined by TS 2	TF BIU #1
1	Defined by TS 2	TF BIU #2
2	Defined by TS 2	TF BIU #3
3	Defined by TS 2	TF BIU #4
4	Reserved for TS 2	TF BIU #5
5	Reserved for TS 2	TF BIU #6
6	Manufacturers' use	TF BIU #7
7	Manufacturers' use	TF BIU #8
8	Defined by TS 2	DET BIU #1
9	Defined by TS 2	DET BIU #2
10	Defined by TS 2	DET BIU #3
11	Defined by TS 2	DET BIU #4
12	Reserved for TS 2	DET BIU #5
13	Reserved for TS 2	DET BIU #6
14	Manufacturers' use	DET BIU #7
15	Manufacturers' use	DET BIU #8

f. All stations transmitting a frame shall utilize zero bit insertion whereby during the transmission of the address, control, information and CRC fields the transmission of five consecutive binary 1's shall always be followed by the insertion of one binary 0. The receiving stations shall strip away these extra inserted 0's.

g. The address, control, and information fields shall be transmitted least significant bit first. The CRC field shall be transmitted most significant bit first.

h. All stations transmitting a frame shall have the capability to abort the transmission of the frame by sending a minimum of eight consecutive binary 1's. All stations receiving a frame shall have the capability of recognizing the abort sequence and terminating the reception of the frame.

3.3.1.4 INFORMATION FIELD FORMATS

Each station shall be responsible for transmitting frames containing information fields. Frames transmitted by the primary station shall be referred to as command frames and frames transmitted by secondary stations or other auxiliary equipment shall be referred to as response frames. Command frames transmitted to BIUs in the TF and in the Detector Racks shall be transmitted only to those BIUs that are present, as determined by the programming entries made in the CU. Response frames shall only be transmitted as a result of receiving a command frame. Unless otherwise indicated, a transmitted binary "1" shall represent the active state and a binary "0" shall represent the inactive state. The first eight bits in each information field shall contain the frame **Type Number**. There shall be a maximum of 64 different command frame types defined by this standard and 64 different response frame types defined by this standard. Additionally, there shall be 64 different command frame types reserved for manufacturers use and 64 different response frame types reserved for manufacturers use, as outlined below.

Frame Types	Function
0–63	Command Frame, Defined by TS 2
64–127	Command Frame, Manufacturers Use
128–191	Response Frame, Defined by TS 2
192–255	Response Frame, Manufacturers Use

The specific frame types, their usage, their destinations, the addresses that must be in their address fields and their functions are summarized in the **Command Frame** table and the **Response Frame** table. The "1" in the "usage" column indicates that the indicated frame type is used in a Type 1 CA. The "2" in the "usage" column indicates that the indicated frame type is used in a Type 2 CA.

The information fields of frame types 64 through 127 shall contain a manufacturer specific code. The manufacturer specific code is a 16 bit binary number which shall be placed in bits 9–24 of the information field. These codes are maintained and issued by NEMA.

Reserved bits shall always be set to zero by the transmitting station.

The intention in placing manufacturer specific codes in frame types that are reserved for manufacturers use is to allow manufacturers of secondary equipment to differentiate between frames that may contain the same frame type. (Authorized Engineering Information)

Command Frames

Type	Usage	Dest.,	Addr.	Function
0	1,2	MMU,	16	Load Switch Drivers
1	1,2	MMU,	16	Request For Input: MMU Status
3	1,2	MMU,	16	Request For Input: MMU Programming Status
9	1,2	ALL,	255	Date And Time Broadcast To All Secondary Stations
10	1	TF,	0	Outputs For TF BIU #1
11	1	TF,	1	Outputs For TF BIU #2
12	1	TF,	2	Outputs For TF BIU #3
13	1	TF,	3	Outputs For TF BIU #4
18	1	ALL	TF, 255	Output Transfer Frame Broadcast to all TF BIUs
20	1,2	DET,	8	Request For Input: DET BIU #1
21	1,2	DET,	9	Request For Input: DET BIU #2
22	1,2	DET,	10	Request For Input: DET BIU #3

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Type	Usage	Dest.,	Addr.	Function
23	1,2	DET,	11	Request For Input: DET BIU #4
24	1,2	DET,	8	Detector Resets and Request for Detector Rack Diagnostic Information (directed to DET BIU #1)
25	1,2	DET,	9	Detector Resets and Request for Detector Rack Diagnostic Information (directed to DET BIU #2)
26	1,2	DET,	10	Detector Resets and Request for Detector Rack Diagnostic Information (directed to DET BIU #3)
27	1,2	DET,	11	Detector Resets and Request for Detector Rack Diagnostic Information (directed to DET BIU #4)
30	1,2	(1)17		Request for Input: Diagnostic Information
40	1,2	ALL,	0–254	Poll for Service: Secondary to Secondary Messaging
41				Reserved
42	1,2	All,	0–254	Secondary Destination Message: Secondary to Secondary Messaging
43	1,2	ALL,	0–254	Secondary Exchange Status: Secondary to Secondary Messaging

(1) Frame Type 30 is for Diagnostic Purposes.

Response Frames

Type	Usage	Source,	Addr.	Function
128	1,2	MMU,	16	ACK for Type 0 Frame
129	1,2	MMU,	16	ACK With Response Data for Type 1 Frame
131	1,2	MMU,	16	ACK With Response Data for Type 3 Frame
138	1	TF,	0	ACK For Type 10 Frame Plus Input Data From TF BIU #1
139	1	TF,	1	ACK For Type 11 Frame Plus Input Data From TF BIU #2
140	1	TF,	2	ACK For Type 12 Frame Plus Input Data From TF BIU #3
141	1	TF,	3	ACK For Type 13 Frame Plus Input Data From TF BIU #4
148	1,2	DET,	8	ACK For Type 20 Frame Plus Input Data From DET BIU #1
149	1,2	DET,	9	ACK For Type 21 Frame Plus Input Data From DET BIU #2
150	1,2	DET,	10	ACK For Type 22 Frame Plus Input Data From DET BIU #3
151	1,2	DET,	11	ACK For Type 23 Frame Plus Input Data From DET BIU #4
152	1,2	DET,	8	ACK For Type 24 Frame Plus Detector Rack Diagnostic Information From DET BIU #1
153	1,2	DET,	9	ACK For Type 25 Frame Plus Detector Rack Diagnostic Information From DET BIU #2
154	1,2	DET,	10	ACK For Type 26 Frame Plus Detector Rack Diagnostic Information From DET BIU #3
155	1,2	DET,	11	ACK For Type 27 Frame Plus Detector Rack Diagnostic Information From DET BIU #4
158	1,2		17	ACK For Type 30 Frame
168	1,2	ALL,	0–254	No Service Required: Secondary To Secondary Messaging
169	1,2	ALL,	0–254	Secondary Source Message: Secondary To Secondary Messaging
170	1,2	ALL,	0–254	Secondary Negative Acknowledge: Secondary To Secondary Messaging
171	1,2	ALL,	0–254	Secondary Acknowledge: Secondary To Secondary Messaging

(DET=Detector Rack, ALL= All secondary stations, ACK=Acknowledge)

The detailed formats for the information fields of the frame types summarized above follows:

1. Primary station (CU)—The primary station shall transmit command frames containing information fields as follows:

   a. Type 0—Load switch drivers. The destination shall be the MMU. The "channel" numbers in the "function" column below refer to the channel numbers of the MMU. The CU shall include a definition, via program entry, of the MMU Channel to CU signal driver group utilization in the terminal facilities. The **Load Switch Flash** bit, when set to "1" shall cause the MMU to disable its **Red Monitoring** function, such that a **Red Failure** does not occur during times when the CU load switch drivers are flashing the load switch outputs. All states of CU No Fault Flash (i.e., Startup, Automatic, and Preempt) shall set Type 0 Command Frame Load Switch Flash bit to 1.

Bit Number	Function
1	0
2	0
3	0
4	0 **Type 0 Command Frame**
5	0
6	0
7	0
8	0
9	Channel 1 Green Driver + (walk)
10	Channel 1 Green Driver - (Walk)
11	Channel 2 Green Driver +(Walk)
12	Channel 2 Green Driver - (Walk)
13	Channel 3 Green Driver +(Walk)
14	Channel 3 Green Driver - (Walk)
15	Channel 4 Green Driver +(Walk)
16	Channel 4 Green Driver - (Walk)
17	Channel 5 Green Driver +(Walk)
18	Channel 5 Green Driver - (Walk)
19	Channel 6 Green Driver +(Walk)

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Bit Number	Function
20	Channel 6 Green Driver - (Walk)
21	Channel 7 Green Driver +(Walk)
22	Channel 7 Green Driver - (Walk)
23	Channel 8 Green Driver +(Walk)
24	Channel 8 Green Driver - (Walk)
25	Channel 9 Green Driver +(Walk)
26	Channel 9 Green Driver - (Walk)
27	Channel 10 Green Driver +(Walk)
28	Channel 10 Green Driver - (Walk)
29	Channel 11 Green Driver +(Walk)
30	Channel 11 Green Driver - (Walk)
31	Channel 12 Green Driver +(Walk)
32	Channel 12 Green Driver - (Walk)
33	Channel 13 Green Driver +(Walk)
34	Channel 13 Green Driver - (Walk)
35	Channel 14 Green Driver +(Walk)
36	Channel 14 Green Driver - (Walk)
37	Channel 15 Green Driver +(Walk)
38	Channel 15 Green Driver - (Walk)
39	Channel 16 Green Driver +(Walk)
40	Channel 16 Green Driver - (Walk)
41	Channel 1 Yellow Driver +(Ped Clear)
42	Channel 1 Yellow Driver -(Ped Clear)
43	Channel 2 Yellow Driver +(Ped Clear)
44	Channel 2 Yellow Driver -(Ped Clear)
45	Channel 3 Yellow Driver +(Ped Clear)
46	Channel 3 Yellow Driver -(Ped Clear)
47	Channel 4 Yellow Driver +(Ped Clear)
48	Channel 4 Yellow Driver -(Ped Clear)
49	Channel 5 Yellow Driver +(Ped Clear)
50	Channel 5 Yellow Driver -(Ped Clear)
51	Channel 6 Yellow Driver +(Ped Clear)
52	Channel 6 Yellow Driver -(Ped Clear)
53	Channel 7 Yellow Driver +(Ped Clear)
54	Channel 7 Yellow Driver -(Ped Clear)
55	Channel 8 Yellow Driver +(Ped Clear)
56	Channel 8 Yellow Driver -(Ped Clear)
57	Channel 9 Yellow Driver +(Ped Clear)
58	Channel 9 Yellow Driver -(Ped Clear)
59	Channel 10 Yellow Driver +(Ped Clear)
60	Channel 10 Yellow Driver -(Ped Clear)
61	Channel 11 Yellow Driver +(Ped Clear)
62	Channel 11 Yellow Driver -(Ped Clear)
63	Channel 12 Yellow Driver +(Ped Clear)
64	Channel 12 Yellow Driver -(Ped Clear)
65	Channel 13 Yellow Driver +(Ped Clear)
66	Channel 13 Yellow Driver -(Ped Clear)
67	Channel 14 Yellow Driver +(Ped Clear)
68	Channel 14 Yellow Driver -(Ped Clear)
69	Channel 15 Yellow Driver +(Ped Clear)
70	Channel 15 Yellow Driver -(Ped Clear)
71	Channel 16 Yellow Driver +(Ped Clear)
72	Channel 16 Yellow Driver -(Ped Clear)

Bit Number	Function
73	Channel 1 Red Driver + (Dont Walk)
74	Channel 1 Red Driver - (Dont Walk)
75	Channel 2 Red Driver + (Dont Walk)
76	Channel 2 Red Driver - (Dont Walk)
77	Channel 3 Red Driver + (Dont Walk)
78	Channel 3 Red Driver - (Dont Walk)
79	Channel 4 Red Driver + (Dont Walk)
80	Channel 4 Red Driver - (Dont Walk)
81	Channel 5 Red Driver + (Dont Walk)
82	Channel 5 Red Driver - (Dont Walk)
83	Channel 6 Red Driver + (Dont Walk)
84	Channel 6 Red Driver - (Dont Walk)
85	Channel 7 Red Driver + (Dont Walk)
86	Channel 7 Red Driver - (Dont Walk)
87	Channel 8 Red Driver + (Dont Walk)
88	Channel 8 Red Driver - (Dont Walk)
89	Channel 9 Red Driver + (Dont Walk)
90	Channel 9 Red Driver - (Dont Walk)
91	Channel 10 Red Driver + (Dont Walk)
92	Channel 10 Red Driver - (Dont Walk)
93	Channel 11 Red Driver + (Dont Walk)
94	Channel 11 Red Driver - (Dont Walk)
95	Channel 12 Red Driver + (Dont Walk)
96	Channel 12 Red Driver - (Dont Walk)
97	Channel 13 Red Driver + (Dont Walk)
98	Channel 13 Red Driver - (Dont Walk)
99	Channel 14 Red Driver + (Dont Walk)
100	Channel 14 Red Driver - (Dont Walk)
101	Channel 15 Red Driver + (Dont Walk)
102	Channel 15 Red Driver - (Dont Walk)
103	Channel 16 Red Driver + (Dont Walk)
104	Channel 16 Red Driver - (Dont Walk)
105	Reserved
106	Reserved
107	Reserved
108	Reserved
109	Reserved
110	Reserved
111	Reserved
112	Load Switch Flash

If both the **Load Switch+** and **Load Switch-** bits are 0, then the corresponding load switch shall not turn on. If the **Load Switch+** bit is 1 and the **Load Switch-** bit is 0, then the corresponding load switch shall cause the field indication to be dimmed by eliminating positive half wave segments from the alternating current sinusoid applied to the field indications. If the **Load Switch+** bit is 0 and the **Load Switch-** bit is 1, then the corresponding load switch shall cause the field indication to be dimmed by eliminating negative half wave segments from the alternating current sinusoid applied to the field indications. If both the **Load Switch+** and the **Load Switch-** bits are 1, then the

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corresponding load switch shall turn on continuously. See Section 3.9.2 for further information on dimming.

b. Type 1—Request for input: MMU status. The destination of these frames is the MMU.

Bit Number	Function	
1	1	Type 1 Command Frame
2	0	
3	0	
4	0	
5	0	
6	0	
7	0	
8	0	

c. Type 3—Request for input: MMU programming status. The destination of these frames is the MMU.

Bit Number	Function	
1	1	Type 3 Command Frame
2	1	
3	0	
4	0	
5	0	
6	0	
7	0	
8	0	

d. Type 9—Date and Time broadcast. The destination of this frame is all secondary stations.

Bit Number	Function	
1	1	Type 9 Command Frame
2	0	
3	0	
4	1	
5	0	
6	0	
7	0	
8	0	
9	Month, Bit 0	
10	Month, Bit 1	
11	Month, Bit 2	
12	Month, Bit 3	
13	Reserved	
14	Reserved	
15	Reserved	
16	Reserved	
17	Day, Bit 0	
18	Day, Bit 1	
19	Day, Bit 2	
20	Day, Bit 3	
21	Day, Bit 4	
22	Reserved	
23	Reserved	
24	Reserved	
25	Year, Bit 0	
26	Year, Bit 1	
27	Year, Bit 2	
28	Year, Bit 3	
29	Year, Bit 4	
30	Year, Bit 5	
31	Year, Bit 6	
32	Reserved	
33	Hour, Bit 0	
34	Hour, Bit 1	
35	Hour, Bit 2	
36	Hour, Bit 3	
37	Hour, Bit 4	
38	Reserved	
39	Reserved	
40	Reserved	
41	Minutes, Bit 0	
42	Minutes, Bit 1	
43	Minutes, Bit 2	
44	Minutes, Bit 3	
45	Minutes, Bit 4	
46	Minutes, Bit 5	
47	Reserved	
48	Reserved	
49	Seconds, Bit 0	
50	Seconds, Bit 1	
51	Seconds, Bit 2	
52	Seconds, Bit 3	
53	Seconds, Bit 4	
54	Seconds, Bit 5	
55	Reserved	
56	Reserved	
57	Tenths of Seconds, Bit 0	
58	Tenths of Seconds, Bit 1	
59	Tenths of Seconds, Bit 2	
60	Tenths of Seconds, Bit 3	
61	Reserved	
62	Reserved	
63	Reserved	
64	Reserved	
65	TF BIU #1 Present	
66	TF BIU #2 Present	
67	TF BIU #3 Present	
68	TF BIU #4 Present	
69	TF BIU #5 Present	
70	TF BIU #6 Present	
71	TF BIU #7 Present	
72	TF BIU #8 Present	
73	DET BIU #1 Present	
74	DET BIU #2 Present	
75	DET BIU #3 Present	
76	DET BIU #4 Present	
77	DET BIU #5 Present	

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78	DET BIU #6 Present
79	DET BIU #7 Present
80	DET BIU #8 Present

Bits 9–64 of this frame shall contain the real time as it currently exists within the CU. This time shall be referred to as the CU real time. The transmission of this frame shall begin within ± 100 milliseconds of the CU real time contained within the frame. Bits 9–16 of this frame shall contain a binary coded representation of the current month of year of the CU real time, in the range 1–12. Bits 17–24 of this frame shall contain a binary coded representation of the current day of month of the CU real time, in the range 1–31. Bits 25–32 of this frame shall contain a binary coded representation of the last two digits of the current year of the CU real time, in the range 0–99. Bits 33–40 of this frame shall contain a binary coded representation of the current hour of the CU real time, in the range 0–23. Bits 41–48 of this frame shall contain a binary coded representation of the current minute of the CU real time, in the range 0–59. Bits 49–56 of this frame shall contain a binary coded representation of the current second of the CU real time, in the range 0–59. Bits 57–64 of this frame shall contain a binary coded representation of the current tenths of seconds of the CU real time, in the range 0–9.

Bits 65–80 of this frame shall contain an exact representation of the programming data in the CU that signifies the presence or absence of TF BIUs 1–8 and Detector Rack BIUs 1–8. A value of "1" shall indicate the presence of the associated BIU and a value of "0" shall indicate the absence of the associated BIU.

All reserved bits in this frame shall be set to zero.

e. Type 10—Outputs for TF BIU #1. The destination of these frames is the TF. Refer to Section 5 of this document for a complete list of BIU #1 signal assignments. Input/Output pins below that are designated as Inputs or Reserved in Section 5 must be driven to the logic "0" state at all times in this Type 10 command frame.

Input/Output pins below that are designated as **Spares** in Section 5 may be driven to the logic "0" state or logic "1" state, at the manufacturer's discretion, in this Type 10 command frame. (Authorized Engineering Information)

Bit Number	Function	
1	0	**Type 10 Command Frame**
2	1	
3	0	
4	1	
5	0	
6	0	
7	0	
8	0	
9	Output 1 (Load Switch +)	
10	Output 1 (Load Switch -)	
11	Output 2 (Load Switch +)	
12	Output 2 (Load Switch -)	
13	Output 3 (Load Switch +)	
14	Output 3 (Load Switch -)	
15	Output 4 (load Switch +)	
16	Output 4 (Load Switch -)	
17	Output 5 (Load Switch +)	
18	Output 5 (Load Switch -)	
19	Output 6 (Load Switch +)	
20	Output 6 (Load Switch -)	
21	Output 7 (Load Switch +)	
22	Output 7 (Load Switch -)	
23	Output 8 (Load Switch +)	
24	Output 8 (Load Switch -)	
25	Output 9 (Load Switch +)	
26	Output 9 (Load Switch -)	
27	Output 10 (Load Switch +)	
28	Output 10 (Load Switch -)	
29	Output 11 (Load Switch +)	
30	Output 11 (Load Switch -)	
31	Output 12 (Load Switch +)	
32	Output 12 (Load Switch -)	
33	Output 13 (Load Switch +)	
34	Output 13 (Load Switch -)	
35	Output 14 (Load Switch +)	
36	Output 14 (Load Switch -)	
37	Output 15 (Load Switch +)	
38	Output 15 (Load Switch -)	
39	Input/Output 1 (Load Switch +)	
40	Input/Output 1 (Load Switch -)	
41	Input/Output 2 (Load Switch +)	
42	Input/Output 2 (Load Switch -)	
43	Input/Output 3 (Load Switch +)	
44	Input/Output 3 (Load Switch -)	
45	Input/Output 4 (Load Switch +)	
46	Input/Output 4 (Load Switch -)	
47	Input/Output 5 (Load Switch +)	
48	Input/Output 5 (Load Switch -)	
49	Input/Output 6 (Load Switch +)	
50	Input/Output 6 (Load Switch -)	
51	Input/Output 7 (Load Switch +)	
52	Input/Output 7 (Load Switch -)	
53	Input/Output 8 (Load Switch +)	
54	Input/Output 8 (Load Switch -)	
55	Input/Output 9 (Load Switch +)	
56	Input/Output 9 (Load Switch -)	
57	Input/Output 10	

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58	Input/Output 11
59	Input/Output 12
60	Input/Output 13
61	Input/Output 14
62	Input/Output 15
63	Input/Output 16
64	Input/Output 17
65	Input/Output 18
66	Input/Output 19
67	Input/Output 20
68	Input/Output 21
69	Input/Output 22
70	Input/Output 23
71	Input/Output 24
72	Reserved

If both the **Load Switch+** and **Load Switch-** bits are 0, then the corresponding load switch shall not turn on. If the **Load Switch+** bit is 1 and the **Load Switch-** bit is 0, then the corresponding load switch shall cause the field indication to be dimmed by eliminating positive half wave segments from the alternating current sinusoid applied to the field indications. If the **Load Switch+** bit is 0 and the **Load Switch-** bit is 1, then the corresponding load switch shall cause the field indication to be dimmed by eliminating negative half wave segments from the alternating current sinusoid applied to the field indications. If both the **Load Switch+** and the **Load Switch-** bits are 1, then the corresponding load switch shall turn on continuously. See Section 3.9.2 for further information on dimming.

f. Type 11—Outputs for TF BIU #2. The destination of these frames is the TF. Refer to Section 5 of this document for a complete list of BIU #2 signal assignments. Input/Output pins below that are designated as Inputs or Reserved in Section 5 must be driven to the logic "0" state at all times in this Type 11 command frame.

Input/Output pins below that are designated as **Spares** in Section 5 may be driven to the logic "0" state or logic "1" state, at the manufacturer's discretion, in this Type 11 command frame. (Authorized Engineering Information)

Bit Number	Function	
1	1	
2	1	
3	0	
4	1	**Type 11 Command Frame**
5	0	
6	0	
7	0	
8	0	
9	Output 1 (Load Switch +)	
10	Output 1 (Load Switch -)	
11	Output 2 (Load Switch +)	
12	Output 2 (Load Switch -)	
13	Output 3 (Load Switch +)	
14	Output 3 (Load Switch -)	
15	Output 4 (Load Switch +)	
16	Output 4 (Load Switch -)	
17	Output 5 (Load Switch +)	
18	Output 5 (Load Switch -)	
19	Output 6 (Load Switch +)	
20	Output 6 (Load Switch -)	
21	Output 7 (Load Switch +)	
22	Output 7 (Load Switch -)	
23	Output 8 (Load Switch +)	
24	Output 8 (Load Switch -)	
25	Output 9 (Load Switch +)	
26	Output 9 (Load Switch -)	
27	Output 10 (Load Switch +)	
28	Output 10 (Load Switch -)	
29	Output 11 (Load Switch +)	
30	Output 11 (Load Switch -)	
31	Output 12 (Load Switch +)	
32	Output 12 (Load Switch -)	
33	Output 13 (Load Switch +)	
34	Output 13 (Load Switch -)	
35	Output 14 (Load Switch +)	
36	Output 14 (Load Switch -)	
37	Output 15 (Load Switch +)	
38	Output 15 (Load Switch -)	
39	Input/Output 1 (Load Switch +)	
40	Input/Output 1 (Load Switch -)	
41	Input/Output 2 (Load Switch +)	
42	Input/Output 2 (Load Switch -)	
43	Input/Output 3 (Load Switch +)	
44	Input/Output 3 (Load Switch -)	
45	Input/Output 4 (Load Switch +)	
46	Input/Output 4 (Load Switch -)	
47	Input/Output 5 (Load Switch +)	
48	Input/Output 5 (Load Switch -)	
49	Input/Output 6 (Load Switch +)	
50	Input/Output 6 (Load Switch -)	
51	Input/Output 7 (Load Switch +)	
52	Input/Output 7 (Load Switch -)	
53	Input/Output 8 (Load Switch +)	
54	Input/Output 8 (Load Switch -)	
55	Input/Output 9 (Load Switch +)	
56	Input/Output 9 (Load Switch -)	
57	Input/Output 10	
58	Input/Output 11	
59	Input/utput 12	
60	Input/Output 13	
61	Input/Output 14	
62	Input/Output 15	

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63	Input/Output 16
64	Input/Output 17
65	Input/Output 18
66	Input/Output 19
67	Input/Output 20
68	Input/Output 21
69	Input/Output 22
70	Input/Output 23
71	Input/Output 24
72	Reserved

If both the **Load Switch+** and **Load Switch-** bits are 0, then the corresponding load switch shall not turn on. If the **Load Switch+** bit is 1 and the **Load Switch-** bit is 0, then the corresponding load switch shall cause the field indication to be dimmed by eliminating positive half wave segments from the alternating current sinusoid applied to the field indications. If the **Load Switch+** bit is 0 and the **Load Switch-** bit is 1, then the corresponding load switch shall cause the field indication to be dimmed by eliminating negative half wave segments from the alternating current sinusoid applied to the field indications. If both the **Load Switch+** and the **Load Switch-** bits are 1, then the corresponding load switch shall turn on continuously. See Section 3.9.2 for further information on dimming.

g. Type 12—Outputs for TF BIU #3. The destination of these frames is the TF. Refer to Section 5 of this document for a complete list of BIU #3 signal assignments. Input/Output pins below that are designated as **Inputs** or **Reserved** in Section 5 must be driven to the logic "0" state at all times in this Type 12 command frame.

Input/Output pins below that are designated as **Spares** in Section 5 may be driven to the logic "0" state or logic "1" state, at the manufacturer's discretion, in this Type 12 command frame. (Authorized Engineering Information)

Bit Number	Function	
1	0	**Type 12 Command Frame**
2	0	
3	1	
4	1	
5	0	
6	0	
7	0	
8	0	
9	Output 1	
10	Output 2	
11	Output 3	
12	Output 4	
13	Output 5	
14	Output 6	
15	Output 7	
16	Output 8	
17	Output 9	
18	Output 10	
19	Output 11	
20	Output 12	
21	Output 13	
22	Output 14	
23	Output 15	
24	Reserved	
25	Input/Output 1	
26	Input/Output 2	
27	Input/Output 3	
28	Input/Output 4	
29	Input/Output 5	
30	Input/Output 6	
31	Input/Output 7	
32	Input/Output 8	
33	Input/Output 9	
34	Input/Output 10	
35	Input/Output 11	
36	Input/Output 12	
37	Input/Output 13	
38	Input/Output 14	
39	Input/Output 15	
40	Input/Output 16	
41	Input/Output 17	
42	Input/Output 18	
43	Input/Output 19	
44	Input/Output 20	
45	Input/Output 21	
46	Input/Output 22	
47	Input/Output 23	
48	Input/Output 24	

h. Type 13—Outputs for TF BIU #4. The destination of these frames is the TF. Refer to Section 5 of this document for a complete list of BIU #4 signal assignments. Input/Output pins below that are designated as **Inputs** or **Reserved** in Section 5 must be driven to the logic "0" state at all times in this Type 13 command frame.

Input/Output pins below that are designated as **Spares** in Section 5 may be driven to the logic "0" state or logic "1" state, at the manufacturer's discretion, in this Type 13 command frame. (Authorized Engineering Information)

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Bit Number	Function	
1	1	Type 13 Command Frame
2	0	
3	1	
4	1	
5	0	
6	0	
7	0	
8	0	
9	Output 1	
10	Output 2	
11	Output 3	
12	Output 4	
13	Output 5	
14	Output 6	
15	Output 7	
16	Output 8	
17	Output 9	
18	Output 10	
19	Output 11	
20	Output 12	
21	Output 13	
22	Output 14	
23	Output 15	
24	Reserved	
25	Input/Output 1	
26	Input/Output 2	
27	Input/Output 3	
28	Input/Output 4	
29	Input/Output 5	
30	Input/Output 6	
31	Input/Output 7	
32	Input/Output 8	
33	Input/Output 9	
34	Input/Output 10	
35	Input/Output 11	
36	Input/Output 12	
37	Input/Output 13	
38	Input/Output 14	
39	Input/Output 15	
40	Input/Output 16	
41	Input/Output 17	
42	Input/Output 18	
43	Input/Output 19	
44	Input/Output 20	
45	Input/Output 21	
46	Input/Output 22	
47	Input/Output 23	
48	Input/Output 24	

i. Type 18—Output transfer broadcast frame. The destination of this frame is all TF BIUs. All other secondary stations shall ignore this frame. The receipt of this frame shall cause the TF BIUs to transfer their outputs, as defined in Section 8 of this standard.

Bit Number	Function	
1	0	Type 18 Command Frame
2	1	
3	0	
4	0	
5	1	
6	0	
7	0	
8	0	

j. Type 20—Request for Input: Detector Rack BIU #1.

Bit Number	Function	
1	0	Type 20 Command Frame
2	0	
3	1	
4	0	
5	1	
6	0	
7	0	
8	0	

k. Types 21–23—Request for Input: Detector Rack BIUs 2–4, respectively. These frame types are identical to Type 20 except that the frame type numbers and addresses are as noted in the **Command Frame** summary.

l. Type 24—Detector resets and request for detector rack diagnostic information. The destination of these frames is the Detector Rack BIU #1. A **Detector Reset** value of logic "1" shall cause the detectors in the associated detector card slots to be reset. A **Detector Reset** value of logic "0" shall have no effect on the associated detectors.

Bit Number	Function	
1	0	Type 24 Command Frame
2	0	
3	0	
4	1	
5	1	
6	0	
7	0	
8	0	
9	Detector Card Slots 1, 2 Reset	
10	Detector Card Slots 3, 4 Reset	
11	Detector Card Slots 5, 6 Reset	
12	Detector Card Slots 7, 8 Reset	
13	Reserved	

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Bit Number	Function
14	Reserved
15	Reserved
16	Reserved

m. Type 25—Detector resets and request for detector rack diagnostic information. The destination of these frames is the Detector Rack BIU #2. A **Detector Reset** value of logic "1" shall cause the detectors in the associated detector card slots to be reset. A **Detector Reset** value of logic "0" shall have no effect on the associated detectors.

Bit Number	Function
1	1 ┐
2	0
3	0
4	1 Type 25 Command Frame
5	1
6	0
7	0
8	0 ┘
9	Detector Card Slots 1, 2 Reset
10	Detector Card Slots 3, 4 Reset
11	Detector Card Slots 5, 6 Reset
12	Detector Card Slots 7, 8 Reset
13	Reserved
14	Reserved
15	Reserved
16	Reserved

n. Type 26—Detector resets and request for detector rack diagnostic information. The destination of these frames is the Detector Rack BIU #3. A **Detector Reset** value of logic "1" shall cause the detectors in the associated detector card slots to be reset. A **Detector Reset** value of logic "0" shall have no effect on the associated detectors.

Bit Number	Function
1	0 ┐
2	1
3	0
4	1 Type 26 Command Frame
5	1
6	0
7	0
8	0 ┘
9	Detector Card Slots 1, 2 Reset
10	Detector Card Slots 3, 4 Reset
11	Detector Card Slots 5, 6 Reset
12	Detector Card Slots 7, 8 Reset
13	Reserved
14	Reserved
15	Reserved
16	Reserved

o. Type 27—Detector resets and request for detector rack diagnostic information. The destination of these frames is the Detector Rack BIU #4. A **Detector Reset** value of logic "1" shall cause the detectors in the associated detector card slots to be reset. A **Detector Reset** value of logic "0" shall have no effect on the associated detectors.

Bit Number	Function
1	1 ┐
2	1
3	0
4	1 Type 27 Command Frame
5	1
6	0
7	0
8	0 ┘
9	Detector Card Slots 1, 2 Reset
10	Detector Card Slots 3, 4 Reset
11	Detector Card Slots 5, 6 Reset
12	Detector Card Slots 7, 8 Reset
13	Reserved
14	Reserved
15	Reserved
16	Reserved

p. Type 30—Request for input: diagnostic information. There shall be programming means in the CU to enable and disable the transmission of this command frame.

The destination of this frame is not defined in this standard. It is intended, however, that this frame will be used by diagnostic test equipment which may be utilized for testing the CU. (Authorized Engineering Information)

Bit Number	Function
1	0 ┐
2	1
3	1
4	1 Type 30 Command Frame
5	1
6	0
7	0
8	0 ┘

q. Type 40—Poll For Service (PFS). This frame type is used to poll the secondary stations for a secondary to secondary message exchange. The destination shall be each secondary station on the link in a sequential fashion. Thus the CU must be programmed with the addresses of all secondary stations which are to receive this frame type. If the addressed secondary station has a message to be sent it shall respond with an SSM Type 169 frame (and be referenced as the "source" secon-

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dary station). If the addressed secondary station does not have a message to be sent it shall respond with an NSR Type 168 frame.

Bit Number	Function	
1	0	Type 40 Command Frame
2	0	
3	0	
4	1	
5	0	
6	1	
7	0	
8	0	

r. Type 41—Reserved

s. Type 42—Secondary Destination Message (SDM). This frame carries the secondary source message from the primary station to the destination address. The destination shall be the secondary station which has been specified as the destination address in the SSM Type 169 response frame (and be referenced as the "destination" secondary station). Bits 9–24 are the source station manufacturer specific ID number, as described in 3.3.1.4. Bits 25–32 identify the source address. Bits 33–288 contain the message data.

Bit Number	Function	
1	1	Type 42 Command Frame
2	0	
3	0	
4	1	
5	0	
6	1	
7	0	
8	0	
9	Manufacturer ID, Bit 1	
10	Manufacturer ID, Bit 2	
11	Manufacturer ID, Bit 3	
12	Manufacturer ID, Bit 4	
13	Manufacturer ID, Bit 5	
14	Manufacturer ID, Bit 6	
15	Manufacturer ID, Bit 7	
16	Manufacturer ID, Bit 8	
17	Manufacturer ID, Bit 9	
18	Manufacturer ID, Bit 10	
19	Manufacturer ID, Bit 11	
20	Manufacturer ID, Bit 12	
21	Manufacturer ID, Bit 13	
22	Manufacturer ID, Bit 14	
23	Manufacturer ID, Bit 15	
24	Manufacturer ID, Bit 16	
25	Source Address, Bit 1	
26	Source Address, Bit 2	
27	Source Address, Bit 3	
28	Source Address, Bit 4	
29	Source Address, Bit 5	
30	Source Address, Bit 6	
31	Source Address, Bit 7	
32	Source Address, Bit 8	
33	Message Data, Bit 1	
.		
.		
.		
288	Message Data, Bit 256	

t. Type 43—Secondary Exchange Status (SES). This frame reports the resulting status of the message exchange to the original source station. The destination shall be the source secondary station. Bit 9 is set to indicate the message exchange is complete with no errors. Bit 10 is set to indicate an SSM Type 169 response frame was received from the source secondary station with an invalid destination address. Bit 11 is set to indicate the SDM Type 42 frame was received correctly but not accepted by the destination secondary due to an invalid manufacturer ID number. Bit 12 is set to indicate the SDM Type 42 command frame was not acknowledged by the destination secondary (CRC error or timeout error).

Bit Number	Function	
1	0	Type 43 Command Frame
2	1	
3	0	
4	1	
5	0	
6	1	
7	0	
8	0	
9	Status Complete	
10	Destination Address Error	
11	Manufacturer Id Error	
12	Destination Timeout	
13	Reserved	
14	Reserved	
15	Reserved	
16	Reserved	

2. Secondary stations—The secondary stations shall transmit response frames containing information fields as follows:

a. Type 128—Positive acknowledge for Type 0 frame from primary station. The source of these frames is the MMU. This frame type shall be transmitted only if a Type 0 frame has been correctly received from the primary station. If a Type 0 frame is received from the primary station with a CRC error, then this frame type shall not be issued.

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with a CRC error, then this frame type shall not be issued.

Bit Number	Function	
1	0	Type 128 Response Frame
2	0	
3	0	
4	0	
5	0	
6	0	
7	0	
8	1	

b. Type 129—Positive acknowledge, with response data, for Type 1 frame from primary station. The source of these frames is the MMU. This frame type shall be transmitted only if a Type 1 frame has been correctly received from the primary station. If a Type 1 frame is received from the primary station with a CRC error, then this frame type shall not be issued. If the MMU is in the "no failure" state and its output relay is energized, then bits 9 through 62 of the information field of this frame shall contain an exact image of the signals that are applied to the MMU front panel connectors and bits 65 through 77 shall be 0. In the event that the MMU has fewer than 16 channels, the bit positions of the nonexistent channels shall be set to 0. If the MMU is in the "failure state" and its output relay is de-energized, then bits 9 through 62 of the information field of this frame shall contain an exact image of the signals that were applied to the MMU front panel connectors at the point in time of the detection of the failure, one or more of bits 65 through 75 shall be set to 1 to indicate the type of failure(s) and bits 76 and 77 shall be 1. If the MMU is in the "failure state" and its output relay is energized, then bits 9 through 62 of the information field of this frame shall contain an exact image of the signals that are applied to the MMU front panel connectors, one or more of bits 65 through 75 shall be set to 1 to indicate the type of failure(s), bit 76 shall be 0 and bit 77 shall be 1.

Bit Number	Function	
1	1	Type 129 Response Frame
2	0	
3	0	
4	0	
5	0	
6	0	
7	0	
8	1	
9	Channel 1 Green	
10	Channel 2 Green	
11	Channel 3 Green	
12	Channel 4 Green	
13	Channel 5 Green	
14	Channel 6 Green	
15	Channel 7 Green	
16	Channel 8 Green	
17	Channel 9 Green	
18	Channel 10 Green	
19	Channel 11 Green	
20	Channel 12 Green	
21	Channel 13 Green	
22	Channel 14 Green	
23	Channel 15 Green	
24	Channel 16 Green	
25	Channel 1 Yellow	
26	Channel 2 Yellow	
27	Channel 3 Yellow	
28	Channel 4 Yellow	
29	Channel 5 Yellow	
30	Channel 6 Yellow	
31	Channel 7 Yellow	
32	Channel 8 Yellow	
33	Channel 9 Yellow	
34	Channel 10 Yellow	
35	Channel 11 Yellow	
36	Channel 12 Yellow	
37	Channel 13 Yellow	
38	Channel 14 Yellow	
39	Channel 15 Yellow	
40	Channel 16 Yellow	
41	Channel 1 Red	
42	Channel 2 Red	
43	Channel 3 Red	
44	Channel 4 Red	
45	Channel 5 Red	
46	Channel 6 Red	
47	Channel 7 Red	
48	Channel 8 Red	
49	Channel 9 Red	
50	Channel 10 Red	
51	Channel 11 Red	
52	Channel 12 Red	
53	Channel 13 Red	
54	Channel 14 Red	
55	Channel 15 Red	
56	Channel 16 Red	
57	Controller Voltage Monitor (1=fail)	
58	+24 Volt Monitor I (1=fail)	
59	+24 Volt Monitor II (1=fail)	
60	+24 Volt Monitor Inhibit (1=inhibit)	
61	Reset (1=reset)	

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Bit Number	Function
62	Red Enable (1=enable)
63	Reserved
64	Reserved
65	Conflict
66	Red Failure
67	Spare Bit 1
68	Spare Bit 2
69	Spare Bit 3
70	Spare Bit 4
71	Spare Bit 5
72	Spare Bit 6
73	MMU Diagnostic Failure
74	Minimum Clearance Failure
75	Port 1 Timeout Failure
76	Fail (1=failed, Output Relay Transferred)
77	Fail (1=failed, Immediate Response To Failure)
78	Reserved
79	Reserved
80	Reserved
81	Reserved
82	Reserved
83	Reserved
84	Reserved
85	Reserved
86	Reserved
87	Reserved
88	Reserved

Spare fault bits are used to indicate MMU detected failures which are not defined in this document. (Authorized Engineering Information)

c. Type 131—Positive acknowledge, with response data, for Type 3 frame from primary station. The source of these frames is the MMU. This frame type shall be transmitted only if a Type 3 frame has been correctly received from the primary station. If a Type 3 frame is received from the primary station with a CRC error, then this frame type shall not be issued. Bits 9–128 of this frame represent an exact image of the compatibility programming status of the MMU. A bit value of 1 indicates that the MMU has been programmed for compatibility between the associated 2 channels. In the event that the MMU has fewer than 16 channels, the bit positions corresponding to the nonexistent channels shall be set to 0. Bits 129–144 of this frame represent an exact image of the Minimum Yellow Change Disable status of the MMU. A bit value of 1 indicates that the Minimum Yellow Change feature has been disabled for the associated channel. Bits 145–148 of this frame represent a binary coded image of the minimum flash time setting in the MMU, in the range 6–16 seconds. Bit 145 shall be the least significant bit and bit 148 shall be the most significant bit. A binary value of 5 shall represent a minimum flash time setting of 6 seconds. Each increment of the binary value shall represent a one second increment of the minimum flash time setting, up to a maximum binary value of 15. Binary values of 0–4 shall not be used. Bit 149 of this frame represents an exact image of the latch setting for 24 volt failures in the MMU. A bit value of 1 indicates that the MMU has been programmed to latch 24 volt failures in the fault condition. Bit 150 of this frame represents an exact image of the latch setting for the controller voltage/fault monitor input in the MMU. A bit value of 1 indicates that the MMU has been programmed to latch CVM failures in the fault condition.

Bit Number	Function	
1	1	Type 131 Response Frame
2	1	
3	0	
4	0	
5	0	
6	0	
7	0	
8	1	
9	Chs. 1–2 Compatibility Status	
10	Chs. 1–3 Compatibility Status	
11	Chs. 1–4 Compatibility Status	
12	Chs. 1–5 Compatibility Status	
13	Chs. 1–6 Compatibility Status	
14	Chs. 1–7 Compatibility Status	
15	Chs. 1–8 Compatibility Status	
16	Chs. 1–9 Compatibility Status	
17	Chs. 1–10 Compatibility Status	
18	Chs. 1–11 Compatibility Status	
19	Chs. 1–12 Compatibility Status	
20	Chs. 1–13 Compatibility Status	
21	Chs. 1–14 Compatibility Status	
22	Chs. 1–15 Compatibility Status	
23	Chs. 1–16 Compatibility Status	
24	Chs. 2–3 Compatibility Status	
25	Chs. 2–4 Compatibility Status	
26	Chs. 2–5 Compatibility Status	
27	Chs. 2–6 Compatibility Status	
28	Chs. 2–7 Compatibility Status	
29	Chs. 2–8 Compatibility Status	

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Bit Number	Function
30	Chs. 2–9 Compatibility Status
31	Chs. 2–10 Compatibility Status
32	Chs. 2–11 Compatibility Status
33	Chs. 2–12 Compatibility Status
34	Chs. 2–13 Compatibility Status
35	Chs. 2–14 Compatibility Status
36	Chs. 2–15 Compatibility Status
37	Chs. 2–16 Compatibility Status
38	Chs. 3–4 Compatibility Status
39	Chs. 3–5 Compatibility Status
40	Chs. 3–6 Compatibility Status
41	Chs. 3–7 Compatibility Status
42	Chs. 3–8 Compatibility Status
43	Chs. 3–9 Compatibility Status
44	Chs. 3–10 Compatibility Status
45	Chs. 3–11 Compatibility Status
46	Chs. 3–12 Compatibility Status
47	Chs. 3–13 Compatibility Status
48	Chs. 3–14 Compatibility Status
49	Chs. 3–15 Compatibilitystatus
50	Chs. 3–16 Compatibility Status
51	Chs. 4–5 Compatibility Status
52	Chs. 4–6 Compatibility Status
53	Chs. 4–7 Compatibility Status
54	Chs. 4–8 Compatibility Status
55	Chs. 4–9 Compatibility Status
56	Chs. 4–10 Compatibility Status
57	Chs. 4–11 Compatibility Status
58	Chs. 4–12 Compatibility Status
59	Chs. 4–13 Compatibility Status
60	Chs. 4–14 Compatibility Status
61	Chs. 4–15 Compatibility Status
62	Chs. 4–16 Compatibility Status
63	Chs. 5–6 Compatibility Status
64	Chs. 5–7 Compatibility Status
65	Chs. 5–8 Compatibility Status
66	Chs. 5–9 Compatibility Status
67	Chs. 5–10 Compatibility Status
68	Chs. 5–11 Compatibility Status
69	Chs. 5–12 Compatibility Status
70	Chs. 5–13 Compatibility Status
71	Chs. 5–14 Compatibility Status
72	Chs. 5–15 Compatibility Status
73	Chs. 5–16 Compatibility Status
74	Chs. 6–7 Compatibility Status
75	Chs. 6–8 Compatibility Status
76	Chs. 6–9 Compatibility Status
77	Chs. 6–10 Compatibility Status
78	Chs. 6–11 Compatibility Status
79	Chs. 6–12 Compatibility Status
80	Chs. 6–13 Compatibility Status
81	Chs. 6–14 Compatibility Status
82	Chs. 6–15 Compatibility Status
83	Chs. 6–16 Compatibility Status
84	Chs. 7–8 Compatibility Status
85	Chs. 7–9 Compatibility Status
86	Chs. 7–10 Compatibility Status
87	Chs. 7–11 Compatibility Status
88	Chs. 7–12 Compatibility Status
89	Chs. 7–13 Compatibility Status
90	Chs. 7–14 Compatibility Status
91	Chs. 715 Compatibility Status
92	Chs. 716 Compatibility Status
93	Chs. 8–9 Compatibility Status
94	Chs. 8–10 Compatibility Status
95	Chs. 8–11 Compatibility Status
96	Chs. 8–12 Compatibility Status
97	Chs. 8–13 Compatibility Status
98	Chs. 8–14 Compatibility Status
99	Chs. 8–15 Compatibility Status
100	Chs. 8–16 Compatibility Status
101	Chs. 9–10 Compatibility Status
102	Chs. 9–11 Compatibility Status
103	Chs. 9–12 Compatibility Status
104	Chs. 9–13 Compatibility Status
105	Chs. 9–14 Compatibility Status
106	Chs. 9–15 Compatibility Status
107	Chs. 9–16 Compatibility Status
108	Chs. 10–11 Compatibility Status
109	Chs. 10–12 Compatibility Status
110	Chs. 10–13 Compatibility Status
111	Chs. 10–14 Compatibility Status
112	Chs. 10–15 Compatibility Status
113	Chs. 10–16 Compatibility Status
114	Chs. 11–12 Compatibility Status
115	Chs. 11–13 Compatibility Status
116	Chs. 11–14 Compatibility Status
117	Chs. 11–15 Compatibility Status
118	Chs. 11–16 Compatibility Status
119	Chs. 12–13 Compatibility Status
120	Chs. 12–14 Compatibility Status
121	Chs. 12–15 Compatibility Status
122	Chs. 12–16 Compatibility Status
123	Chs. 13–14 Compatibility Status
124	Chs. 13–15 Compatibility Status
125	Chs. 13–16 Compatibility Status
126	Chs. 14–15 Compatibility Status
127	Chs. 14–16 Compatibility Status
128	Chs. 15–16 Compatibility Status
129	Ch. 1 Minimum Yellow Change Disable

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Bit Number	Function
130	Ch. 2 Minimum Yellow Change Disable
131	Ch. 3 Minimum Yellow Change Disable
132	Ch. 4 Minimum Yellow Change Disable
133	Ch. 5 Minimum Yellow Change Disable
134	Ch. 6 Minimum Yellow Change Disable
135	Ch. 7 Minimum Yellow Change Disable
136	Ch. 8 Minimum Yellow Change Disable
137	Ch. 9 Minimum Yellow Change Disable
138	Ch. 10 Minimum Yellow Change Disable
139	Ch. 11 Minimum Yellow Change Disable
140	Ch. 12 Minimum Yellow Change Disable
141	Ch. 13 Minimum Yellow Change Disable
142	Ch. 14 Minimum Yellow Change Disable
143	Ch. 15 Minimum Yellow Change Disable
144	Ch. 16 Minimum Yellow Change Disable
145	Min. Flash Time, Bit 1
146	Min. Flash Time, Bit 2
147	Min. Flash Time, Bit 4
148	Min. Flash Time, Bit 8
149	24 Volt Latch
150	CVM/Fault Monitor Latch
151	Reserved
152	Reserved
153	Reserved
154	Reserved
155	Reserved
156	Reserved
157	Reserved
158	Reserved
159	Reserved
160	Reserved
161	Reserved
162	Reserved
163	Reserved
164	Reserved
165	Reserved
166	Reserved
167	Reserved
168	Reserved

d. Type 138—Positive acknowledge, with response data, for Type 10 frame from primary station. The source of these frames is the TF BIU #1. This frame type shall be transmitted only if a Type 10 frame has been correctly received from the primary station. If a Type 10 frame is received from the primary station with a CRC error, then this frame type shall not be issued. Refer to Section 5 of this document for a complete list of BIU #1 signal assignments. Input/Output pins below that are designated as **Outputs** in Section 5 shall not be used as inputs in this frame.

Bit Number	Function	
1	0	**Type 138 Response Frame**
2	1	
3	0	
4	1	
5	0	
6	0	
7	0	
8	1	
9	Input/Output 1	
10	Input/Output 2	
11	Input/Output 3	
12	Input/Output 4	
13	Input/Output 5	
14	Input/Output 6	
15	Input/Output 7	
16	Input/Output 8	
17	Input/Output 9	
18	Input/Output 10	
19	Input/Output 11	
20	Input/Output 12	
21	Input/Output 13	
22	Input/Output 14	
23	Input/Output 15	
24	Input/Output 16	
25	Input/Output 17	
26	Input/Output 18	
27	Input/Output 19	
28	Input/Output 20	
29	Input/Output 21	
30	Input/Output 22	
31	Input/Output 23	
32	Input/Output 24	
33	Input 1	
34	Input 2	
35	Input 3	
36	Input 4	
37	Input 5	
38	Input 6	
39	Input 7	
40	Input 8	
41	Opto-input 1	
42	Opto-input 2	
43	Opto-input 3	
44	Opto-input 4	
45	Reserved	
46	Reserved	
47	Reserved	
48	Reserved	

e. Types 139–141—These frame types are identical to Type 138 except that the frame type numbers

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and addresses are as noted in the **Response Frame** summary. Refer to Section 5 of this document for a complete list of signal assignments for BIUs 2–4.

f. Type 148—Positive acknowledge, with response data, for Type 20 frame from primary station. The source of these frames is the Detector Rack BIU #1. This frame type shall be transmitted only if a Type 20 frame has been correctly received from the primary station. If a type 20 frame is received from the primary station with a CRC error, then this frame type shall not be issued. The two detector call status bits for each detector channel shall be defined as follows:

Bit 1	Bit 0	Definition
0	0	The channel has no call, and there has been no change in this status since this frame was last transmitted (no call, no change).
0	1	The channel has a call, and there has been no change in this status since this frame was last transmitted (constant call, no change).
1	0	The channel has no call, and there has been a change in this status since this frame was last transmitted (call has gone away).
1	1	The channel has a call, and there has been a change in this status since this frame was last transmitted (new call).

The 16 detector time stamp bits for each detector channel (bits 0 through 15) shall contain the value of the detector BIU internal time stamp generator at the instant in time when the detector call last changed status. Each detector BIU shall contain an internal time stamp generator. This generator shall be a free running 16 bit binary counter that starts counting at 0 following the application of power to the BIU and counts up to 65,535. At the next increment after reaching a value of 65,535, the counter shall roll over to 0 and start over. The detector bus interface unit time stamp generator shall increment every 1.0 milliseconds ±0.05 percent. The time stamp generator shall not be effected by the reception of a Type 9 frame from the CU (date and time broadcast).

The detector BIU internal time stamp generator is intended to provide the means by which precision timing information about detector calls can be obtained. When only detector call status is needed without any timing information, then it is only necessary to use detector call status bit 0 for each channel. When precision occupancy data is needed or precision speed data for any detector pair(s) is needed, then the time stamp generator data for each detector channel may be used, with a resolution of 1.0 milliseconds. Since the time stamp generator in each detector BIU is not synchronous with the time stamp generators in the other detector BIUs, only pairs of detectors on a single BIU should be used for speed measurements. (Authorized Engineering Information)

Bit Number	Function	
1	0	**Type 148 Response Frame**
2	0	
3	1	
4	0	
5	1	
6	0	
7	0	
8	1	
9	Det 1 Time Stamp Bit 0	
10	Det 1 Time Stamp Bit 1	
11	Det 1 Time Stamp Bit 2	
12	Det 1 Time Stamp Bit 3	
13	Det 1 Time Stamp Bit 4	
14	Det 1 Time Stamp Bit 5	
15	Det 1 Time Stamp Bit 6	
16	Det 1 Time Stamp Bit 7	
17	Det 1 Time Stamp Bit 8	
18	Det 1 Time Stamp Bit 9	
19	Det 1 Time Stamp Bit 10	
20	Det 1 Time Stamp Bit 11	
21	Det 1 Time Stamp Bit 12	
22	Det 1 Time Stamp Bit 13	
23	Det 1 Time Stamp Bit 14	
24	Det 1 Time Stamp Bit 15	
25	Det 2 Time Stamp Bit 0	
26	Det 2 Time Stamp Bit 1	
27	Det 2 Time Stamp Bit 2	
28	Det 2 Time Stamp Bit 3	
29	Det 2 Time Stamp Bit 4	
30	Det 2 Time Stamp Bit 5	
31	Det 2 Time Stamp Bit 6	
32	Det 2 Time Stamp Bit 7	
33	Det 2 Time Stamp Bit 8	
34	Det 2 Time Stamp Bit 9	
35	Det 2 Time Stamp Bit 10	
36	Det 2 Time Stamp Bit 11	
37	Det 2 Time Stamp Bit 12	
38	Det 2 Time Stamp Bit 13	
39	Det 2 Time Stamp Bit 14	
40	Det 2 Time Stamp Bit 15	
41	Det 3 Time Stamp Bit 0	
42	Det 3 Time Stamp Bit 1	
43	Det 3 Time Stamp Bit 2	

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Bit Number	Function	Bit Number	Function
44	Det 3 Time Stamp Bit 3	95	Det 6 Time Stamp Bit 6
45	Det 3 Time Stamp Bit 4	96	Det 6 Time Stamp Bit 7
46	Det 3 Time Stamp Bit 5	97	Det 6 Time Stamp Bit 8
47	Det 3 Time Stamp Bit 6	98	Det 6 Time Stamp Bit 9
48	Det 3 Time Stamp Bit 7	99	Det 6 Time Stamp Bit 10
49	Det 3 Time Stamp Bit 8	100	Det 6 Time Stamp Bit 11
50	Det 3 Time Stamp Bit 9	101	Det 6 Time Stamp Bit 12
51	Det 3 Time Stamp Bit 10	102	Det 6 Time Stamp Bit 13
52	Det 3 Time Stamp Bit 11	103	Det 6 Time Stamp Bit 14
53	Det 3 Time Stamp Bit 12	104	Det 6 Time Stamp Bit 15
54	Det 3 Time Stamp Bit 13	105	Det 7 Time Stamp Bit 0
55	Det 3 Time Stamp Bit 14	106	Det 7 Time Stamp Bit 1
56	Det 3 Time Stamp Bit 15	107	Det 7 Time Stamp Bit 2
57	Det 4 Time Stamp Bit 0	108	Det 7 Time Stamp Bit 3
58	Det 4 Time Stamp Bit 1	109	Det 7 Time Stamp Bit 4
59	Det 4 Time Stamp Bit 2	110	Det 7 Time Stamp Bit 5
60	Det 4 Time Stamp Bit 3	111	Det 7 Time Stamp Bit 6
61	Det 4 Time Stamp Bit 4	112	Det 7 Time Stamp Bit 7
62	Det 4 Time Stamp Bit 5	113	Det 7 Time Stamp Bit 8
63	Det 4 Time Stamp Bit 6	114	Det 7 Time Stamp Bit 9
64	Det 4 Time Stamp Bit 7	115	Det 7 Time Stamp Bit 10
65	Det 4 Time Stamp Bit 8	116	Det 7 Time Stamp Bit 11
66	Det 4 Time Stamp Bit 9	117	Det 7 Time Stamp Bit 12
67	Det 4 Time Stamp Bit 10	118	Det 7 Time Stamp Bit 13
68	Det 4 Time Stamp Bit 11	119	Det 7 Time Stamp Bit 14
69	Det 4 Time Stamp Bit 12	120	Det 7 Time Stamp Bit 15
70	Det 4 Time Stamp Bit 13	121	Det 8 Time Stamp Bit 0
71	Det 4 Time Stamp Bit 14	122	Det 8 Time Stamp Bit 1
72	Det 4 Time Stamp Bit 15	123	Det 8 Time Stamp Bit 2
73	Det 5 Time Stamp Bit 0	124	Det 8 Time Stamp Bit 3
74	Det 5 Time Stamp Bit 1	125	Det 8 Time Stamp Bit 4
75	Det 5 Time Stamp Bit 2	126	Det 8 Time Stamp Bit 5
76	Det 5 Time Stamp Bit 3	127	Det 8 Time Stamp Bit 6
77	Det 5 Time Stamp Bit 4	128	Det 8 Time Stamp Bit 7
78	Det 5 Time Stamp Bit 5	129	Det 8 Time Stamp Bit 8
79	Det 5 Time Stamp Bit 6	130	Det 8 Time Stamp Bit 9
80	Det 5 Time Stamp Bit 7	131	Det 8 Time Stamp Bit 10
81	Det 5 Time Stamp Bit 8	132	Det 8 Time Stamp Bit 11
82	Det 5 Time Stamp Bit 9	133	Det 8 Time Stamp Bit 12
83	Det 5 Time Stamp Bit 10	134	Det 8 Time Stamp Bit 13
84	Det 5 Time Stamp Bit 11	135	Det 8 Time Stamp Bit 14
85	Det 5 Time Stamp Bit 12	136	Det 8 Time Stamp Bit 15
86	Det 5 Time Stamp Bit 13	137	Det 9 Time Stamp Bit 0
87	Det 5 Time Stamp Bit 14	138	Det 9 Time Stamp Bit 1
88	Det 5 Time Stamp Bit 15	139	Det 9 Time Stamp Bit 2
89	Det 6 Time Stamp Bit 0	140	Det 9 Time Stamp Bit 3
90	Det 6 Time Stamp Bit 1	141	Det 9 Time Stamp Bit 4
91	Det 6 Time Stamp Bit 2	142	Det 9 Time Stamp Bit 5
92	Det 6 Time Stamp Bit 3	143	Det 9 Time Stamp Bit 6
93	Det 6 Time Stamp Bit 4	144	Det 9 Time Stamp Bit 7
94	Det 6 Time Stamp Bit 5	145	Det 9 Time Stamp Bit 8

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Bit Number	Function	Bit Number	Function
146	Det 9 Time Stamp Bit 9	197	Det 12 Time Stamp Bit 12
147	Det 9 Time Stamp Bit 10	198	Det 12 Time Stamp Bit 13
148	Det 9 Time Stamp Bit 11	199	Det 12 Time Stamp Bit 14
149	Det 9 Time Stamp Bit 12	200	Det 12 Time Stamp Bit 15
150	Det 9 Time Stamp Bit 13	201	Det 13 Time Stamp Bit 0
151	Det 9 Time Stamp Bit 14	202	Det 13 Time Stamp Bit 1
152	Det 9 Time Stamp Bit 15	203	Det 13 Time Stamp Bit 2
153	Det 10 Time Stamp Bit 0	204	Det 13 Time Stamp Bit 3
154	Det 10 Time Stamp Bit 1	205	Det 13 Time Stamp Bit 4
155	Det 10 Time Stamp Bit 2	206	Det 13 Time Stamp Bit 5
156	Det 10 Time Stamp Bit 3	207	Det 13 Time Stamp Bit 6
157	Det 10 Time Stamp Bit 4	208	Det 13 Time Stamp Bit 7
158	Det 10 Time Stamp Bit 5	209	Det 13 Time Stamp Bit 8
159	Det 10 Time Stamp Bit 6	210	Det 13 Time Stamp Bit 9
160	Det 10 Time Stamp Bit 7	211	Det 13 Time Stamp Bit 10
161	Det 10 Time Stamp Bit 8	212	Det 13 Time Stamp Bit 11
162	Det 10 Time Stamp Bit 9	213	Det 13 Time Stamp Bit 12
163	Det 10 Time Stamp Bit 10	214	Det 13 Time Stamp Bit 13
164	Det 10 Time Stamp Bit 11	215	Det 13 Time Stamp Bit 14
165	Det 10 Time Stamp Bit 12	216	Det 13 Time Stamp Bit 15
166	Det 10 Time Stamp Bit 13	217	Det 14 Time Stamp Bit 0
167	Det 10 Time Stamp Bit 14	218	Det 14 Time Stamp Bit 1
168	Det 10 Time Stamp Bit 15	219	Det 14 Time Stamp Bit 2
169	Det 11 Time Stamp Bit 0	220	Det 14 Time Stamp Bit 3
170	Det 11 Time Stamp Bit 1	221	Det 14 Time Stamp Bit 4
171	Det 11 Time Stamp Bit 2	222	Det 14 Time Stamp Bit 5
172	Det 11 Time Stamp Bit 3	223	Det 14 Time Stamp Bit 6
173	Det 11 Time Stamp Bit 4	224	Det 14 Time Stamp Bit 7
174	Det 11 Time Stamp Bit 5	225	Det 14 Time Stamp Bit 8
175	Det 11 Time Stamp Bit 6	226	Det 14 Time Stamp Bit 9
176	Det 11 Time Stamp Bit 7	227	Det 14 Time Stamp Bit 10
177	Det 11 Time Stamp Bit 8	228	Det 14 Time Stamp Bit 11
178	Det 11 Time Stamp Bit 9	229	Det 14 Time Stamp Bit 12
179	Det 11 Time Stamp Bit 10	230	Det 14 Time Stamp Bit 13
180	Det 11 Time Stamp Bit 11	231	Det 14 Time Stamp Bit 14
181	Det 11 Time Stamp Bit 12	232	Det 14 Time Stamp Bit 15
182	Det 11 Time Stamp Bit 13	233	Det 15 Time Stamp Bit 0
183	Det 11 Time Stamp Bit 14	234	Det 15 Time Stamp Bit 1
184	Det 11 Time Stamp Bit 15	235	Det 15 Time Stamp Bit 2
185	Det 12 Time Stamp Bit 0	236	Det 15 Time Stamp Bit 3
186	Det 12 Time Stamp Bit 1	237	Det 15 Time Stamp Bit 4
187	Det 12 Time Stamp Bit 2	238	Det 15 Time Stamp Bit 5
188	Det 12 Time Stamp Bit 3	239	Det 15 Time Stamp Bit 6
189	Det 12 Time Stamp Bit 4	240	Det 15 Time Stamp Bit 7
190	Det 12 Time Stamp Bit 5	241	Det 15 Time Stamp Bit 8
191	Det 12 Time Stamp Bit 6	242	Det 15 Time Stamp Bit 9
192	Det 12 Time Stamp Bit 7	243	Det 15 Time Stamp Bit 10
193	Det 12 Time Stamp Bit 8	244	Det 15 Time Stamp Bit 11
194	Det 12 Time Stamp Bit 9	245	Det 15 Time Stamp Bit 12
195	Det 12 Time Stamp Bit 10	246	Det 15 Time Stamp Bit 13
196	Det 12 Time Stamp Bit 11	247	Det 15 Time Stamp Bit 14

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Bit Number	Function
248	Det 15 Time Stamp Bit 15
249	Det 16 Time Stamp Bit 0
250	Det 16 Time Stamp Bit 1
251	Det 16 Time Stamp Bit 2
252	Det 16 Time Stamp Bit 3
253	Det 16 Time Stamp Bit 4
254	Det 16 Time Stamp Bit 5
255	Det 16 Time Stamp Bit 6
256	Det 16 Time Stamp Bit 7
257	Det 16 Time Stamp Bit 8
258	Det 16 Time Stamp Bit 9
259	Det 16 Time Stamp Bit 10
260	Det 16 Time Stamp Bit 11
261	Det 16 Time Stamp Bit 12
262	Det 16 Time Stamp Bit 13
263	Det 16 Time Stamp Bit 14
264	Det 16 Time Stamp Bit 15
265	Det 1 Call Status Bit 0
266	Det 2 Call Status Bit 0
267	Det 3 Call Status Bit 0
268	Det 4 Call Status Bit 0
269	Det 5 Call Status Bit 0
270	Det 6 Call Status Bit 0
271	Det 7 Call Status Bit 0
272	Det 8 Call Status Bit 0
273	Det 9 Call Status Bit 0
274	Det 10 Call Status Bit 0
275	Det 11 Call Status Bit 0
276	Det 12 Call Status Bit 0
277	Det 13 Call Status Bit 0
278	Det 14 Call Status Bit 0
279	Det 15 Call Status Bit 0
280	Det 16 Call Status Bit 0
281	Det 1 Call Status Bit 1
282	Det 2 Call Status Bit 1
283	Det 3 Call Status Bit 1
284	Det 4 Call Status Bit 1
285	Det 5 Call Status Bit 1
286	Det 6 Call Status Bit 1
287	Det 7 Call Status Bit 1
288	Det 8 Call Status Bit 1
289	Det 9 Call Status Bit 1
290	Det 10 Call Status Bit 1
291	Det 11 Call Status Bit 1
292	Det 12 Call Status Bit 1
293	Det 13 Call Status Bit 1
294	Det 14 Call Status Bit 1
295	Det 15 Call Status Bit 1
296	Det 16 Call Status Bit 1

g. Types 149–151. These frame types are identical to Type 148 except that the frame type numbers and addresses are as noted in the **Response Frame** summary. Type 149 is the response data from BIU #2 for detectors 17–32; Type 150 is the response data from BIU #3 for detectors 33–48; Type 151 is the response data from BIU #4 for detectors 49–64.

h. Type 152. Positive acknowledge, with response data, for Type 24 frame from primary station. The source of these frames is the Detector Rack BIU #1. This frame type shall be transmitted only if a Type 24 frame has been correctly received from the primary station. If a Type 24 frame is received from the primary station with a CRC error, then this frame type shall not be issued. The bits designated "watchdog failure," "open loop," "shorted loop," and "excessive change in inductance" shall indicate failures. The logical 1 state shall represent the failed state and the logical 0 state shall represent the good state.

Bit Number	Function	
1	0	Type 152 Response Frame
2	0	
3	0	
4	1	
5	1	
6	0	
7	0	
8	1	
9	Det 1, Watchdog Failure	
10	Det 1, Open Loop	
11	Det 1, Shorted Loop	
12	Det 1, Excessive Change In Inductance	
13	Det 1, Bit 4 (reserved)	
14	Det 1, Bit 5 (reserved)	
15	Det 1, Bit 6 (reserved)	
16	Det 1, Bit 7 (reserved)	
17	Det 2, Watchdog Failure	
18	Det 2, Open Loop	
19	Det 2, Shorted Loop	
20	Det 2, Excessive Change In Inductance	
21	Det 2, Bit 4 (reserved)	
22	Det 2, Bit 5 (reserved)	
23	Det 2, Bit 6 (reserved)	
24	Det 2, Bit 7 (reserved)	
25	Det 3, Watchdog Failure	
26	Det 3, Open Loop	
27	Det 3, Shorted Loop	
28	Det 3, Excessive Change In Inductance	
29	Det 3, Bit 4 (reserved)	
30	Det 3, Bit 5 (reserved)	
31	Det 3, Bit 6 (reserved)	
32	Det 3, Bit 7 (reserved)	
33	Det 4, Watchdog Failure	

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Bit Number	Function
34	Det 4, Open Loop
35	Det 4, Shorted Loop
36	Det 4, Excessive Change In Inductance
37	Det 4, Bit 4 (reserved)
38	Det 4, Bit 5 (reserved)
39	Det 4, Bit 6 (reserved)
40	Det 4, Bit 7 (reserved)
41	Det 5, Watchdog Failure
42	Det 5, Open Loop
43	Det 5, Shorted Loop
44	Det 5, Excessive Change In Inductance
45	Det 5, Bit 4 (reserved)
46	Det 5, Bit 5 (reserved)
47	Det 5, Bit 6 (reserved)
48	Det 5, Bit 7 (reserved)
49	Det 6, Watchdog Failure
50	Det 6, Open Loop
51	Det 6, Shorted Loop
52	Det 6, Excessive Change In Inductance
53	Det 6, Bit 4 (reserved)
54	Det 6, Bit 5 (reserved)
55	Det 6, Bit 6 (reserved)
56	Det 6, Bit 7 (reserved)
57	Det 7, Watchdog Failure
58	Det 7, Open Loop
59	Det 7, Shorted Loop
60	Det 7, Excessive Change In Inductance
61	Det 7, Bit 4 (reserved)
62	Det 7, Bit 5 (reserved)
63	Det 7, Bit 6 (reserved)
64	Det 7, Bit 7 (reserved)
65	Det 8, Watchdog Failure
66	Det 8, Open Loop
67	Det 8, Shorted Loop
68	Det 8, Excessive Change In Inductance
69	Det 8, Bit 4 (reserved)
70	Det 8, Bit 5 (reserved)
71	Det 8, Bit 6 (reserved)
72	Det 8, Bit 7 (reserved)
73	Det 9, Watchdog Failure
74	Det 9, Open Loop
75	Det 9, Shorted Loop
76	Det 9, Excessive Change In Inductance
77	Det 9, Bit 4 (reserved)
78	Det 9, Bit 5 (reserved)
79	Det 9, Bit 6 (reserved)
80	Det 9, Bit 7 (reserved)
81	Det 10, Watchdog Failure
82	Det 10, Open Loop
83	Det 10, Shorted Loop
84	Det 10, Excessive Change in Inductance
85	Det 10, Bit 4 (reserved)
86	Det 10, Bit 5 (reserved)
87	Det 10, Bit 6 (reserved
88	Det 10, Bit 7 (reserved)
89	Det 11, Watchdog Failure
90	Det 11, Open Loop
91	Det 11, Shorted Loop
92	Det 11, Excessive Change in Inductance
93	Det 11, Bit 4 (reserved)
94	Det 11, Bit 5 (reserved)
95	Det 11, Bit 6 (reserved)
96	Det 11, Bit 7 (reserved)
97	Det 12, Watchdog Failure
98	Det 12, Open Loop
99	Det 12, Shorted Loop
100	Det 12, Excessive Change in Inductance
101	Det 12, Bit 4 (reserved)
102	Det 12, Bit 5 (reserved)
103	Det 12, Bit 6 (reserved)
104	Det 12, Bit 7 (reserved)
105	Det 13, Watchdog Failure
106	Det 13, Open Loop
107	Det 13, Shorted Loop
108	Det 13, Excessive Change In Inductance
109	Det 13, Bit 4 (reserved)
110	Det 13, Bit 5 (reserved)
111	Det 13, Bit 6 (reserved)
112	Det 13, Bit 7 (reserved)
113	Det 14, Watchdog Failure
114	Det 14, Open Loop
115	Det 14, Shorted Loop
116	Det 14, Excessive Change in Inductance
117	Det 14, Bit 4 (reserved)
118	Det 14, Bit 5 (reserved)
119	Det 14, Bit 6 (reserved)
120	Det 14, Bit 7 (reserved)
121	Det 15, Watchdog Failure
122	Det 15, Open Loop
123	Det 15, Shorted Loop
124	Det 15, Excessive Change In Inductance
125	Det 15, Bit 4 (reserved)
126	Det 15, Bit 5 (reserved)
127	Det 15, Bit 6 (reserved)
128	Det 15, Bit 7 (reserved)
129	Det 16, Watchdog Failure
130	Det 16, Open Loop
131	Det 16, Shorted Loop
132	Det 16, Excessive Change in Inductance
133	Det 16, Bit 4 (reserved)
134	Det 16, Bit 5 (reserved)
135	Det 16, Bit 6 (reserved)

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Bit Number	Function
136	Det 16, Bit 7 (reserved)

i. Types 153–155. These frame types are identical to Type 152 except that the frame type numbers and addresses are as noted in the **Response Frame** summary. Type 153 is the diagnostic response data from BIU #2 for detectors 17–32; Type 154 is the diagnostic response data from BIU #3 for detectors 33–48; Type 155 is the diagnostic response data from BIU #4 for detectors 49–64.

j. Type 158. Positive acknowledge, with response data, for Type 30 frame from primary station. This frame type shall be transmitted only if a Type 30 frame has been correctly received from the primary station. If a Type 30 frame is received from the primary station with a CRC error, then this frame Type shall not be issued. Bits 9–48 of this frame shall function identically to bits 9–48 of response frame Type 138 from TF BIU #1 and the CU shall act on them in an identical manner. Bits 49–88 of this frame shall function identically to bits 9–48 of response frame Type 139 from TF BIU #2 and the CU shall act on them in an identical manner. Bits 89–128 of this frame shall function identically to bits 9–48 of response frame Type 140 from TF BIU #3 and the CU shall act on them in an identical manner. Bits 129–168 of this frame shall function identically to bits 9–48 of response frame Type 141 from TF BIU #4 and the CU shall act on them in an identical manner. Bits 169–184 of this frame shall function identically to the 16 bits named **DET 1 Call Status Bit 0** through **DET 16 Call Status Bit 0** in response frame Type 148 and the CU shall act on them in an identical manner. Bits 185–200 of this frame shall function identically to the 16 bits named **DET 17 Call Status Bit 0** through **DET 32 Call Status Bit 0** in response frame Type 149 and the CU shall act on them in an identical manner. The CU shall logically "OR" all bits received in this frame with those received in other frames referenced here prior to acting on them.

Bit Number	Function	
1	0	**Type 158 Response Frame**
2	1	
3	1	
4	1	
5	1	
6	0	
7	0	
8	1	
9–168	See Text Above	
169	Detector Call #1	
170	Detector Call #2	
171	Detector Call #3	
172	Detector Call #4	
173	Detector Call #5	
174	Detector Call #6	
175	Detector Call #7	
176	Detector Call #8	
177	Detector Call #9	
178	Detector Call #10	
179	Detector Call #11	
180	Detector Call #12	
181	Detector Call #13	
182	Detector Call #14	
183	Detector Call #15	
184	Detector Call #16	
185	Detector Call #17	
186	Detector Call #18	
187	Detector Call #19	
188	Detector Call #20	
189	Detector Call #21	
190	Detector Call #22	
191	Detector Call #23	
192	Detector Call #24	
193	Detector Call #25	
194	Detector Call #26	
195	Detector Call #27	
196	Detector Call #28	
197	Detector Call #29	
198	Detector Call #30	
199	Detector Call #31	
200	Detector Call #32	

k. Type 168—No Service Required (NSR). Positive acknowledge for PFS Type 40 frame from the primary station. This frame Type shall be transmitted only if a Type 40 frame has been correctly received from the primary station and the secondary station does not have a message to exchange with another secondary station. If a Type 40 frame is received from the primary station with a CRC error, then this frame type shall not be issued.

Bit Number	Function	
1	0	**Type 168 Command Frame**
2	0	
3	0	
4	1	
5	0	
6	1	
7	0	
8	1	

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l. Type 169—Secondary Source Message (SSM). Positive acknowledge, with response data, for PFS Type 40 frame from the primary station. This frame type shall be transmitted only if a Type 40 frame has been correctly received from the primary station and the secondary station has a message to exchange with another secondary station. If a Type 40 frame is received from the primary station with a CRC error, then this frame type shall not be issued. Bits 9–24 are the source station manufacturer specific ID number, as described in 3.3.1.4. Bits 25–32 identify the destination address. Bits 33–288 contain the message data.

Bit Number	Function	
1	1	Type 169 Command Frame
2	0	
3	0	
4	1	
5	0	
6	1	
7	0	
8	1	
9	Manufacturer Id, Bit 0	
10	Manufacturer Id, Bit 1	
11	Manufacturer Id, Bit 2	
12	Manufacturer Id, Bit 3	
13	Manufacturer Id, Bit 4	
14	Manufacturer Id, Bit 5	
15	Manufacturer Id, Bit 6	
16	Manufacturer Id, Bit 7	
17	Manufacturer Id, Bit 8	
18	Manufacturer Id, Bit 9	
19	Manufacturer Id, Bit 10	
20	Manufacturer Id, Bit 11	
21	Manufacturer Id, Bit 12	
22	Manufacturer Id, Bit 13	
23	Manufacturer Id, Bit 14	
24	Manufacturer Id, Bit 15	
25	Dest Address, Bit 1	
26	Dest Address, Bit 2	
27	Dest Address, Bit 3	
28	Dest Address, Bit 4	
29	Dest Address, Bit 5	
30	Dest Address, Bit 6	
31	Dest Address, Bit 7	
32	Dest Address, Bit 8	
33	Message Data, Bit 1	
.		
.		
.		
288	Message Data, Bit 256	

m. Type 170—Secondary Negative Acknowledge (SNAC). Negative acknowledge for SDM Type 42 frame from the primary station. This frame type shall be transmitted only if a Type 42 frame has been correctly received from the primary station and the destination station determines the manufacturer specific ID number is not valid. If a Type 42 frame is received from the primary station with a CRC error, then this frame type shall not be issued.

Bit Number	Function	
1	0	Type 170 Command Frame
2	1	
3	0	
4	1	
5	0	
6	1	
7	0	
8	1	

n. Type 171—Secondary Acknowledge (SAC). Positive acknowledge for SDM Type 42 frame or SES Type 43 frame from the primary station. This frame type shall be transmitted only if a Type 42 or Type 43 frame has been correctly received from the primary station. If a Type 42 or Type 43 frame is received from the primary station with a CRC error, then this frame type shall not be issued.

Bit Number	Function	
1	1	Type 171 Command Frame
2	1	
3	0	
4	1	
5	0	
6	1	
7	0	
8	1	

3.3.1.4.1 Secondary to Secondary Messages

Secondary station to secondary station messaging provides a method of exchanging manufacturer specific data from one station to another station via the Port 1 data link. The message data contained in the information field of a Type 169 response frame is transmitted from the "source" secondary station through the primary station to the "destination" station. The message data contents are meaningful only to the secondary stations.

There shall be a programming means in the CU to identify the secondary station addresses which will receive the Type 40 frame. The primary station shall transmit a Type 40 command frame to each designated secondary station on the link in a sequential fashion. The broadcast address (255) shall be invalid as a destination address. If

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a secondary station has a message to exchange it shall respond to the Type 40 command frame with a Type 169 response frame. If the secondary station does not have a message to exchange it shall respond with a Type 168 response frame. Upon correct receipt of the Type 169 response frame from the source secondary station, the primary station shall transmit the message data to the destination secondary station in a Type 42 command frame. Upon correct receipt of the Type 42 command frame from the primary station, the destination secondary station shall acknowledge receipt with either a Type 171 or Type 170 response frame. The primary station shall complete the message exchange by transmitting a Type 43 command frame to the source secondary with the status of the exchange. This command frame shall be acknowledged by the source secondary station with a Type 171 response frame.

Secondary stations shall respond to command frames within the service time defined in Section 3.3.1.5.2.

A determined access time for service may not be provided due to variations in the number of stations, the amount of secondary messages transmitted, etc. Therefore, time critical (real time) messages should be discouraged. Since the message data contents are specific only to the source and destination stations, it is dependant on the user of manufacturer specific messages to assure validation of the sender and contents of the message. (Authorized Engineering Information)

3.3.1.5 FRAME TIMING

3.3.1.5.1 Primary Station

The CU shall be designated the Primary Station. The transmission of Port 1 command frames shall be controlled by the CU. The primary station shall transmit all frame types within a one second window, with the window repeating itself in a cyclical manner every second that the primary station is operating. Each one second window shall start with the beginning of the transmission of frame Type 9, the date and time broadcast to all secondary stations. The beginning of the transmission of frame Type 9 shall occur every 1.0 seconds ±0.01 seconds. Each frame type shall have a defined frequency of transmission, such that some frames shall be transmitted more frequently than once per second. Table 3.3.1-1 shows the command frames and their frequency of transmission. If the command frames are required to be transmitted, as determined by CU programming means described elsewhere in this standard, then the frequency of transmission shall be exactly as shown. The minimum number of command frames transmitted by the CU each second shall be determined by Equation 3.3.1-1, where T represents the number of TF BIUs present (as determined by CU programming means) and D represents the number of Detector Rack BIUs present (as determined by CU programming means).

Equation 3.3.1-1

$$\#\text{Command Frames} = 32 + 11D \quad (T = 0)$$

$$\#\text{Command Frames} = 42 + 10T + 11D \quad (T > 0)$$

Table 3.3.1-1
COMMAND FRAMES AND FREQUENCY OF TRANSMISSION

Type	Freq. of Trans.	Description
0	10 Times/Second	Load Switch Drivers
1	10 Times/Second	Request For Input:MMU Status
3	1 Time/Second	Request For Input:MMU Programming Status
9	1 Time/Second	Date and Time Broadcast to All Secondary Stations
10	10 Times/Second	Outputs For TF BIU #1
11	10 Times/Second	Outputs For TF BIU #2
12	10 Times/Second	Outputs For TF BIU #3
13	10 Times/Second	Outputs For TF BIU #4
18	10 Times/Second	Output Transfer Broadcast For TF BIUs
20	10 Times/Second	Request For Input:DET BIU #1
21	10 Times/Second	Request For Input:DET BIU #2
22	10 Times/Second	Request For Input:DET BIU #3
23	10 Times/Second	Request For Input:DET BIU #4
24	1 Time/Second	Detector Resets And Request For Detector Rack Diagnostic Information (directed to DET BIU #1)
25	1 Time/Second	Detector Resets And Request For Detector Rack Diagnostic Information (directed to DET BIU #2)
26	1 Time/Second	Detector Resets And Request For Detector Rack Diagnostic Information (directed to DET BIU #3)
27	1 Time/Second	Detector Resets And Request For Detector Rack Diagnostic Information (directed to DET BIU #4)
30	1 Time/Second	Request For Input: Diagnostic Information
40*	10 Times/Second	Poll for Status: Secondary to Secondary Messaging

* The Type 40 frame may be replaced by a Type 42 or 43, as required, during secondary to secondary messaging (See 3.3.1.5.4).

3.3.1.5.2 Secondary Stations

The MMU, TF and the Detector Racks shall be designated secondary stations. Secondary stations shall begin their response to command frames from the primary station within a designated period of time following the complete reception of each command frame. This period shall be known as the **Service Time at Secondaries** and shall have a maximum value of 0.5 milliseconds. Secondary stations may begin their responses to command frames

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immediately following the complete reception of command frames. The secondary's **Tx Clock** and **Tx Data** link output shall be in its high impedance state outside of the interval defined by its service time plus response time.

3.3.1.5.3 Handshaking

The transmission of command and response frames shall take place using a full duplex arrangement. The transmission of command frames shall begin at the start of each one second window. Following the transmission of each command frame there shall be a **Dead Time** during which the CU does not transmit. Following the **Dead Time** interval, the CU shall begin the transmission of the next frame in the prescribed sequence. Each secondary station shall begin its response to command frames following the reception of command frames, as outlined in 3.3.1.5.2. Failure to receive at the CU a given complete response frame type from a secondary station prior to receiving any other complete response frame type shall be cause to count a **No Response** for the given response frame type. The transmission of each response frame shall be completed before the completion of the transmission of the next command frame in the prescribed sequence. This is illustrated in Figure 3.3.1-5. In order to meet this requirement, the inequality shown in Equation 3.3.1-2 shall be met at all times.

Equation 3.3.1-2

$$[\text{Service}(N)+\text{Response}(N)] \leq [\text{Dead}(N)+\text{Command}(N+1)]$$

Where **Service**(N) represents the maximum service time at secondaries for any frame (i.e., 0.5 milliseconds), **Response**(N) represents the maximum response frame transmission time at a secondary in responding to a given frame (i.e., frame number N), **Dead**(N) represents the minimum dead time following the transmission of a given frame (i.e., frame number N), and **Command**(N+1) represents the minimum command frame transmission time for the next frame in the prescribed sequence (i.e., frame number N+1). Thus, the **Dead Time** following the transmission of each command frame shall have a minimum value that meets the requirements of Equation 3.3.1-3, where **Dead**(N), **Service**(N), **Response**(N) and **Command**(N+1) are as described above. In no event, however, shall the **Dead Time** be less than 0.5 milliseconds.

Equation 3.3.1-3

$$\text{Dead}(N) = \text{Service}(N) + \text{Response}(N) - \text{Command}(N+1)$$

For the purpose of calculating the minimum **Dead Time** from Equation 3.3.1-3, the values for **Service, Response,** and **Command** for each command frame type shall be taken from Table 3.3.1-2, where each of the values shown represents milliseconds.

Table 3.3.1-2
SERVICE, RESPONSE, AND COMMAND VALUES (MILLISECONDS)

Frame Type	Service	Response	Command
0	0.5	0.442	1.031
1	0.5	1.074	0.360
3	0.5	1.705	0.360
9	0.5	n/a	0.825
10	0.5	0.758	0.773
11	0.5	0.758	0.773
12	0.5	0.758	0.618
13	0.5	0.758	0.618
18	0.5	n/a	0.360
20	0.5	2.715	0.360
21	0.5	2.715	0.360
22	0.5	2.715	0.360
23	0.5	2.715	0.360
24	0.5	1.453	0.412
25	0.5	1.453	0.412
26	0.5	1.453	0.412
27	0.5	1.453	0.412
30	0.5	1.957	0.360
40	0.5	2.652	0.360
42	0.5	0.442	2.166
43	0.5	0.442	0.360

The values shown in Table 3.3.1-2 are based on the following considerations: The maximum service time at secondaries shall be 0.5 milliseconds. The maximum response frame transmission time at secondaries shall be equal to the total number of bits in the response frame (which is equal to the number of information field bits

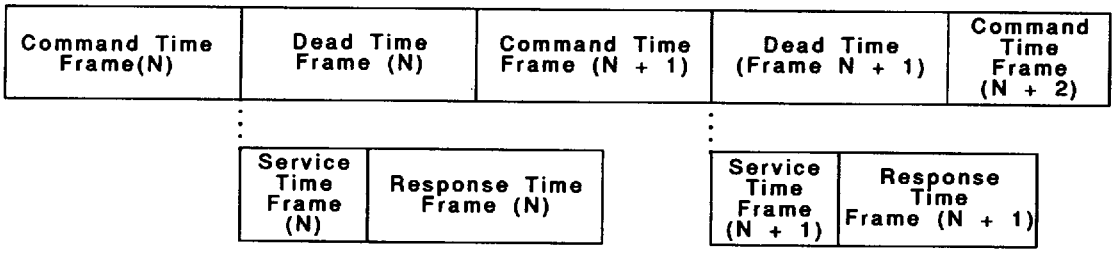

Figure 3.3.1-5
COMMAND AND RESPONSE FRAME TIMING

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specified in 3.3.1.4 plus 48) divided by the minimum data transfer rate specified in 3.3.1.3 and multiplied by 1.2 (to account for the extreme of maximum zero bit insertion). Thus the maximum response frame transmission time at secondaries shall be equal to the total number of bits in the response frame divided by 126,720. The minimum command frame transmission time shall be equal to the total number of bits in the command frame (which is equal to the number of information field bits specified in 3.3.1.4 plus 48) divided by the maximum data transfer rate specified in 3.3.1.3 (to account for the extreme of no zero bit insertion). Thus the minimum command frame transmission time shall be equal to the total number of bits in the command frame divided by 155,136.

In the event that manufacturer specific command and response frames are generated, the calculation of the minimum **Dead Time** following the transmission of each command frame shall be based on the same considerations specified above.

3.3.1.5.4 Command Frame Scheduling

The one second window described in 3.3.1.5.1, during which time all frame types shall be transmitted, shall be divided into ten 100 millisecond windows, each of which shall have a duration of 100 ± 10 milliseconds. The summation of the durations of the ten 100 millisecond windows in each one second window shall be 1.0 ± 0.01 seconds.

All command frames shown in Table 3.3.1-1 and shown as having a frequency of transmission of 10 times/second and required to be transmitted by the CU, as determined by CU programming means, shall be transmitted in their entirety in each of the 100 millisecond windows. The scheduling of the transmission of these frames shall be such that they are transmitted in the following order in each of the 100 millisecond windows: frame Type 0, 1, 10, 11, 12, 13, 18, 20, 21, 22, 23, 40.

All command frames shown in Table 3.3.1-1 and shown as having a frequency of transmission of 1 time/second and required to be transmitted by the CU, as determined by CU programming means, shall be transmitted in their entirety in each of the one second windows. The scheduling of the transmission of these frames shall be such that they are transmitted in the following order in each of the one second windows: frame Type 9, 3, 24, 25, 26, 27, 30. Only one of these frames shall be transmitted in each of the 100 millisecond windows. Thus frame Type 9 shall be transmitted in the first 100 millisecond window of each one second window, frame Type 3 shall be transmitted in the second 100 millisecond window, etc.

At a minimum, one Type 40, 42, or 43 command frame shall be transmitted in each 100 millisecond window. Only one command frame type shall be transmitted within each 100 millisecond window. In the event of link errors caused by CRC or timeouts, retries by the primary station shall be optional and shall occur within the same 100 millisecond window. Receipt of a new Type 40 command frame by a source secondary instead of the Type 43 command frame will indicate to the source secondary that the current message exchange may not have been completed successfully and has been aborted.

At the manufacturers discretion, the transmission of manufacturer specific command frames may take place at any point in the one second window, except that frame Type 9 shall be the first frame transmitted in each one second window. The use of manufacturer specific command and response frames shall not preclude the transmission of frame Types 9, 3, 24, 25, 26, 27, 30, 0, 1, 10, 11, 12, 13, 18, 20, 21, 22, 23, 40 and their response frames, in the manner specified on the previous page.

3.3.2 Port 2 RS-232C Interface

An RS-232C Data Terminal Equipment (DTE) interface and connector shall be provided for interconnecting to a printer or personal computer.

The connector shall be mounted on the front of the CU and shall be a 25 pin metal shell "D" subminiature type connector. The connector shall utilize female contacts with 15 millionths of an inch minimum gold plating in the mating areas. The connector shall be equipped with latching blocks. The connector shall mate with a 25 pin "D" type connector, AMP Incorporated part number 205208-1, or equivalent, which is equipped with spring latches, AMP Incorporated part number 745013-1, or equivalent.

Pin	Function	I/O
1	Earth Ground	[-]
2	Transmit Data	[O]
3	Receive Data	[I]
4	Request To Send	[O]
5	Clear To Send	[I]
6	Not Used	
7	Logic Ground	[-]
8	Data Carrier Detect	[I]
9–19	Not Used	
20	Data Terminal Ready	[O]
21–25	Not Used	

The RS232C function reference for Pin 1 is Frame Ground and Pin 7 is Signal Ground.

3.3.2.1 UNIT TO PRINTER

The CU timing data, operational data, and reports shall be capable of being transmitted to the printer.

The CU shall interface with a printer capable of eighty columns or more.

The CU shall provide for asynchronous serial data communications with RS-232C signal levels, X-On/X-Off handshaking protocols, a word structure of 1 Start Bit + 7

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Data Bits + 1 Parity Bit (Even) + 1 Stop Bit, transmit and receive ASCII coded 1200 Bits Per Second serial data.

3.3.2.2 UNIT TO PERSONAL COMPUTER

The CU shall be capable of transmitting and receiving 1) unit timing and operations data, 2) activity status, and 3) unit reports to a personal computer running the appropriate software. The data transmissions shall be checked for accuracy.

3.3.3 Port 3 System Interface

An interface and connector shall be provided for interconnecting the CU to the system interconnect lines.

3.3.3.1 CONNECTOR

The Port 3 connector shall be mounted on the front of the CU and shall be a 9 pin metal shell "D" subminiature type connector. The connector shall utilize male contacts with 15 millionths of an inch minimum gold plating in the mating areas. The connector shall be equipped with latching blocks. The connector shall mate with a 9 pin "D" type connector, AMP Incorporated part number 205203-1, or equivalent, which is equipped with spring latches, AMP Incorporated part number 745011-1, or equivalent.

Pin connections shall be as follows:

Pin	Function	I/O
1	Transmit 1	[O]
2	Transmit 2	[O]
3	Reserved	
4	Receive 1	[I]
5	Receive 2	[I]
6	Earth Ground	[-]
7	Reserved	
8	Reserved	
9	Earth Ground	[-]

Pins 6 and 9 are provided for connection to an external cable shield, if appropriate (Authorized Engineering Information).

3.3.3.2 INTERFACE

The system interface shall provide four-wire full duplex communications over an unconditioned Type 3002 voice grade private line channel or equivalent customer owned cable.

3.3.3.2.1 Transmission Method

Communications over the system interface shall utilize time division multiplex techniques. Transmissions shall use phase coherent frequency shift keying (FSK) modulation at a data rate of 1200 bps. Data format shall be asynchronous, bit serial.

3.3.3.2.2 Transmitter Characteristics

The transmitter portion of the system interface shall be a digital to FSK modulator. Output level shall be 0 dBm ±15% into a 600 ohm load. Frequency stability of the transmitted signal shall be ±5% over the CU operating temperature range. Transmit frequencies shall be 1200 Hz for MARK (logic 1) and 2200 Hz for Space (logic 0).

3.3.3.2.3 Receiver Characteristics

The receiver portion of the system interface shall be a FSK to digital demodulator. Receiver sensitivity shall be a minimum of -34dBm. In band signal-to-noise ratio shall be 10dB or greater.

3.3.4 Type 1—Interface Standards

A Type A1 or P1 CU shall provide an input/output interface to meet the following requirements.

The connector shall have a metallic shell, be connected to the Earth Ground internally, be mounted on the front of the unit, and intermate with a MS3106( )-18-1S.

Input/Output connector pin terminations shall be as follows:

Connector "A" Pin/Function

Pin	Function	I/O
A	AC Neutral	[I]
B	Not Used	
C	AC Line	[I]
D	Not Used	
E	Not Used	
F	Fault Monitor	[O]
G	Logic Ground	[O]
H	Earth Ground	[I]
I	Not Used	
J	Not Used	

3.3.5 Type 2—Interface Standards

A Type A2 or P2 CU shall provide an input/output interface to meet the following requirements.

3.3.5.1 ELECTRICAL LIMITS OF INPUT/OUTPUT TERMINATIONS

3.3.5.1.1 Logic Levels

All logic signals (except as explicitly defined elsewhere in these standards) shall be low state (nominal 0 volts) for the True (operate) state of all input and output terminations. Input/Output terminations, when not activated, shall be internally biased to the False (high) nonoperate state (+24 volts DC).

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3.3.5.1.2 Transient Immunity

The operation of the CU shall not be affected during operation by the application to any input or output terminal of pulses of 10 microseconds duration, 300-volt positive or negative amplitude, and with a maximum repetition rate of 1 pulse per second. For the purposes of this requirement, a pulse source having an output impedance of not less than 1K ohms, nor greater than 10K ohms shall be used.

3.3.5.1.3 Inputs

Inputs shall have the following characteristics:

1. A voltage between 0 and 8 volts shall be considered the **Low** state.
2. A voltage greater than 16 volts shall be considered the **High** state.
3. The transition from the **Low** state to **High** state (and vice versa) shall occur between 8 and 16 volts.
4. External transition from the **Low** state to **High** state (and vice versa) shall be accomplished within 0.1 millisecond.
5. Over the voltage range 0 to 26 volts DC, the maximum current **In** or **Out** of any input control terminal shall be less than 10 milliamperes. Input impedance shall not exceed 11K ohms to 24 volts DC, nor shall the surge impedance be less than 100 ohms resistive.
6. Any input signal dwelling in a defined logic state for less than 8 milliseconds shall not be recognized. Any input signal dwelling in a defined logic state for more than 17 milliseconds shall be recognized. Successive similar logic state transitions shall not be recognized when occurring less than 8 milliseconds apart, and shall be recognized when occurring more than 34 milliseconds apart.

3.3.5.1.4 Outputs

Electrical outputs shall have the following characteristics:

1. Output Circuits
   a. The **Low** (operate) voltage shall be between 0 and 4 volts.
   b. Current sinking capability in the **Low** state (**True**) shall be at least 200 milliamperes from an inductive load.
   c. With an external impedance of 100K ohms or greater, the transition from 4 to 16 volts (and vice versa) shall be accomplished within 0.1 millisecond.
   d. The **High** state impedance shall not exceed 11K ohms to 24 volts DC.
   e. Any external steady-state voltage applied to an output terminal shall not exceed +30 volts DC, nor shall it cause flow of more than 3 milliamperes into the terminal, when the output is in the **High** state.
   f. Any valid **True** output signal, except Load Switch Driver outputs when Dimming is enabled, shall dwell in this state for at least 50 milliseconds.
2. Regulated 24 Volts DC for External Use
   a. Positive 24 ± 2 volts DC shall be regulated over an AC line voltage variation from 89 to 135 volts and from no load to full load.
   b. Current capability shall be 500 milliamperes continuous with less than 0.5 volt peak-to-peak ripple.

3.3.5.2 PIN CONNECTIONS

The Type A2 and P2 CU shall provide input/output interface pin connections per 3.3.5.2.1 and 3.3.5.2.2.

3.3.5.2.1 Connectors Used

The connector on the CU shall have a metallic shell. The connector shall be connected to the chassis internally. The connectors shall be mounted on the front of the unit in accordance with the following:

1. Connector A shall intermate with a MS3116( )-22-55S
2. Connector B shall intermate with a MS3116( )-22-55P
3. Connector C shall intermate with a MS3116( )-24-61P

Controller Unit	Conn A	Conn B	Conn C
Type A2 Actuated	X	X	X
Type P2 Pretimed	X	X	

3.3.5.2.2 Input/Output Connector Pin Terminations

Input/Output connector pin terminations shall be in accordance with the following:

Connnector "A" Pin/Function

55 Pin (Plug) Type # -22-55P

Pin	Function	I/O
A	Fault Monitor	[O]
B	+24 VDC (External)	[O]
C	Voltage Monitor	[O]
D	Vehicle 1 Red	[O]
E	Pedest. 1 Dont Walk	[O]
F	Vehicle 2 Red	[O]
G	Pedest. 2 Dont Walk	[O]
H	Pedest. 2 Ped Clear	[O]
J	Pedest. 2 Walk	[O]
K	Vehicle 2 Detector	[I]
L	Pedest. 2 Detector	[I]
M	Input 1	[I]
N	Input 2	[I]
P	Input 3	[I]
R	Input 4	[I]
S	Input 5	[I]
T	Input 6	[I]
U	AC Neutral	[I]

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Pin	Function	I/O
V	Earth Ground	[I]
W	Logic Ground	[O]
X	Flashing Logic	[O]
Y	Output 1	[O]
Z	Vehicle 1 Yellow	[O]
a	Pedest. 1 Ped Clear	[O]
b	Vehicle 2 Yellow	[O]
c	Vehicle 2 Green	[O]
d	Output 2	[O]
e	Output 3	[O]
f	Vehicle 1 Detector	[I]
g	Pedest. 1 Detector	[I]
h	Input 7	[I]
i	Input 8	[I]
j	Input 9	[I]
k	Input 10	[I]
m	Input 11	[I]
n	Test A	[I]
p	AC Line	[I]
q	I/O Mode Bit A	[I]
r	Output 4	[O]
s	Vehicle 1 Green	[O]
t	Pedest. 1 Walk	[O]
u	Output 5	[O]
v	Input 12	[I]
w	Input 13	[I]
x	Input 14	[I]
y	I/O Mode Bit B	[I]
z	Input 15	[I]
AA	Test B	[I]
BB	Input 16	[I]
CC	Output 6	[O]
DD	Output 7	[O]
EE	Input 17	[I]
FF	Input 18	[I]
GG	Input 19	[I]
HH	I/O Mode Bit C	[I]

Connector "B" Pin/Function

55 Pin (Socket) Type # -22-55S

Pin	Function	I/O
A	Output 8	[O]
B	Input 20	[I]
C	Output 9	[O]
D	Vehicle 3 Green	[O]
E	Vehicle 3 Yellow	[O]
F	Vehicle 3 Red	[O]
G	Vehicle 4 Red	[O]
H	Pedest. 4 Ped Clear	[O]
J	Pedest. 4 Dont Walk	[O]
K	Output 10	[O]
L	Vehicle 4 DET	[I]
M	Pedest. 4 DET	[I]
N	Vehicle 3 DET	[I]
P	Pedest. 3 DET	[I]
R	Input 21	[I]
S	Input 22	[I]
T	Input 23	[I]
U	Input 24	[I]
V	Input 25	[I]
W	Input 26	[I]
X	Input 27	[I]
Y	Pedest. 3 Walk	[O]
Z	Pedest. 3 Ped Clear	[O]
a	Pedest. 3 Dont Walk	[O]
b	Vehicle 4 Green	[O]
c	Vehicle 4 Yellow	[O]
d	Pedest. 4 Walk	[O]
e	Output 11	[O]
f	Output 12	[O]
g	Input 28	[I]
h	Input 29	[I]
i	Input 30	[I]
j	Input 31	[I]
k	Input 32	[I]
m	Input 33	[I]
n	Input 34	[I]
p	Vehicle A Yellow	[O]
q	Vehicle A Red	[O]
r	Output 13	[O]
s	Output 14	[O]
t	Output 15	[O]
u	Vehicle D Red	[O]
v	Input 35	[I]
w	Vehicle D Green	[O]
x	Input 36	[I]
y	Input 37	[I]
z	Input 38	[I]
AA	Vehicle A Green	[O]
BB	Vehicle B Yellow	[O]
CC	Vehicle B Red	[O]
DD	Vehicle C Red	[O]
EE	Vehicle D Yellow	[O]
FF	Vehicle C Green	[O]
GG	Vehicle B Green	[O]
HH	Vehicle C Yellow	[O]

Connector "C" Pin/Function

61 Pin (Socket) Type # -24-61S

Pin	Function	I/O
A	Output 16	[O]
B	Output 17	[O]
C	Pedest. 8 Dont Walk	[O]
D	Vehicle 8 Red	[O]

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Pin	Function	I/O
E	Vehicle 7 Yellow	[O]
F	Vehicle 7 Red	[O]
G	Vehicle 6 Red	[O]
H	Vehicle 5 Red	[O]
J	Vehicle 5 Yellow	[O]
K	Pedest. 5 Ped Clear	[O]
L	Pedest. 5 Dont Walk	[O]
M	Output 18	[O]
N	Output 19	[O]
P	Vehicle 5 Detector	[I]
R	Pedest. 5 Detector	[I]
S	Vehicle 6 Detector	[I]
T	Pedest. 6 Detector	[I]
U	Pedest. 7 Detector	[I]
V	Vehicle 7 Detector	[I]
W	Pedest. 8 Detector	[I]
X	Input 39	[I]
Y	Input 40	[I]
Z	Input 41	[I]
a	Input 42	[I]
b	Test C	[I]
c	Output 20	[O]
d	Pedest. 8 Walk	[O]
e	Vehicle 8 Yellow	[O]
f	Vehicle 7 Green	[O]
g	Vehicle 6 Green	[O]
h	Vehicle 6 Yellow	[O]
i	Vehicle 5 Green	[O]
j	Pedest. 5 Walk	[O]
k	Output 21	[O]
m	Input 44	[I]
n	Input 45	[I]
p	Input 46	[I]
q	Input 47	[I]
r	Input 48	[I]
s	Input 49	[I]
t	Vehicle 8 Detector	[I]
u	Input 50	[I]
v	Input 51	[I]
w	Pedest. 8 Ped Clear	[O]
x	Vehicle 8 Green	[O]
y	Pedest. 7 Dont Walk	[O]
z	Pedest. 6 Dont Walk	[O]
AA	Pedest. 6 Ped Clear	[O]
BB	Output 23	[O]
CC	Output 24	[O]
DD	Output 25	[O]
EE	Input 52	[I]
FF	Output 26	[O]
GG	Output 27	[O]
HH	Output 28	[O]
JJ	Pedest. 7 Walk	[O]
KK	Pedest. 7 Ped Clear	[O]
LL	Pedest. 6 Walk	[O]
MM	Output 29	[O]
NN	Output 30	[O]
PP	Output 31	[O]

3.4 PRETIMED CONTROL

The Standards in Section 3.4 respond to the need for the functional interchangeability of Solid State Traffic Signal CUs, pretimed type. Interchangeability of equipment manufactured in conformance with these standards has been promoted by connector plug compatibility.

Interchangeability of equipment can be achieved only when units are configured to produce the same functional operation utilizing exactly the same inputs and outputs.

Configurations 'P1' and 'P2' CUs (see Section 3.2) shall provide functional capability to meet the pretimed control requirement herein.

3.4.1 Definitions

3.4.1.1 SIGNAL PLAN

A unique set of parameters that define the sequence and control for one cycle.

3.4.2 General

The solid state pretimed CU shall be an interval oriented device. The conditions of the output circuits (Load Switch Drivers) shall be programmable as to condition in each of the Signal Plan intervals. The interval sequence, interval timing, and output circuit condition are used to control the order in which traffic movements are assigned the right-of-way at the intersection and the time allocated to each.

The CU shall be capable of operating as a master controller, isolated controller, or secondary controller without changes or additions.

The CU shall accept Timing Plan and Offset commands from traditional interconnect systems, the internal system interface, and/or from a companion Time Base program.

The CU shall be capable of providing the following features:

3.4.2.1 TIMING PLANS

The CU shall provide control for a minimum of sixteen timing plans. The CU shall select the timing plan to be used, according to the current status of the Timing Plan request.

3.4.2.1.1 Cycles

The CU shall be capable of providing a minimum of one cycle length for each timing plan. Each cycle length shall

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be adjustable over a range of 30 to 255 seconds in 1 second increments.

3.4.2.1.2 Splits

The CU shall be capable of providing a minimum of one set of splits for each timing plan. Each split shall provide an adjustable time for each interval in the sequence in accordance with the following:

a. 0 to 25.5 seconds in 0.1 second increments, and
b. 0 to 255 seconds in 1 second increments, or
c. 0 to 99 percent (of cycle length) in 1% increments.

3.4.2.2 INTERVALS

The CU shall be capable of providing a minimum of 24 intervals per Timing Plan. When less than 24 intervals are required, it shall be possible to program only the number used.

3.4.2.3 SIGNAL PLANS

The CU shall be capable of implementing four different signal plans. All signal plans shall have the same number of intervals.

Signal Plans shall be capable of being selected based on program entry, interconnect inputs, time base control events, and a system interface.

The CU shall provide the following capability within each signal plan:

3.4.2.3.1 Minimum Time

Means shall be provided, for user definition, of a Minimum Time for each interval (0 to 25.5 seconds in 0.1 second increments).

3.4.2.3.2 Load Switch Driver Condition

Means shall be provided, for user definition, of the output condition (**Green, Yellow,** or **Red**) of each Vehicle Load Switch Driver Group for each interval. A circuit closure to **Logic Ground** shall be maintained at one of these three outputs at all times. The three outputs shall energize the appropriate vehicle signal load switching circuit to result in a **Green, Yellow**, or **Red** indication for the duration of such required indication.

Means shall be provided, for user definition, of the output condition (**Walk, Ped Clear**, or **Dont Walk**) of each Pedestrian Load Switch Drivers Group for each interval. A circuit closure to **Logic Ground** shall be maintained on at least one of these three outputs at all times. The three outputs shall energize the appropriate pedestrian signal load switching circuit to result in a **Walk, Pedestrian Clearance**, or **Dont Walk** indication. The **Dont Walk** output shall flash only during the **Pedestrian Clearance** interval(s).

3.4.2.3.3 Timing Plan Transfer

Means shall be provided, for user definition, of the interval end at which a Timing Plan transfer may occur.

3.4.2.3.4 Signal Plan Transfer

Means shall be provided, for user definition, of the interval end at which a Signal Plan transfer may occur.

3.4.2.3.5 Variable Interval

Means shall be provided, for user definition, of the intervals which shall be considered "variable" for offset correction, force off, and manual control enable operation.

3.4.2.3.6 Automatic Flash

Means shall be provided, for user definition, of the interval end as the Automatic Flash Entry point and the interval beginnning as the Automatic Flash Exit point.

3.4.2.3.7 Actuated Interval(s)

Means shall be provided, for user definition, of the interval(s) which are serviced based on the activity of vehicle and/or pedestrian detectors.

3.4.2.4 OFFSET

The CU shall provide three offset settings for each of the Timing Plans.

Each offset shall provide an adjustable interval time in accordance with either of the following:

a. 0 to 254 seconds in 1.0 second increments, or
b. 0 to 99 percent (of cycle length) in 1% increments.

The values shall determine the time in seconds that the starting point of Interval #1, local time zero, shall lag the Synchronization pulse, system time zero.

The CU shall recognize when the sync reference and local offset in control indicate local zero is not correct. When establishing its offset based on the sync pulse, the CU shall reference only the leading edge, regardless of the width of the sync pulse.

3.4.2.5 SYNC MONITOR

The CU shall monitor the Offset command requests for validity of the imposed sync reference.

The CU shall revert to Free mode when:

1. No sync pulse is received for 3 consecutive cycles
2. No offset line is active for 15 seconds
3. More than one offset line is active for 15 seconds

During Sync Monitor **Free** mode, the Offset command requests shall continue to be monitored and should the command request return to valid operation, the CU shall implement the pattern commanded.

The Sync Monitor **Free** mode may be replaced by a Time Base Control event. See the **On-Line** definition in the Time Base section.

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3.4.2.6 MANUAL CONTROL

The CU shall be capable of being set to manually operate in any pattern (Timing Plan plus Offset) and Signal Plan via program entry. A manual selection of pattern and signal plan shall override all other pattern interface commands.

3.4.2.7 FREE MODE

The CU shall be capable of Free mode of operation. During this mode all pattern inputs (**Timing Plan** and **Offset**) shall be ignored and offset correction shall not occur.

The coordinator shall be capable of being set to the Free mode defined under Sync Monitor and via program entry.

The coordinator shall recognize input requests that conflict with coordinated operation and automatically revert to Free mode while the inputs are active. The inputs that conflict with internal coordination are:

1. Manual Control Enable
2. Stop Time
3. Automatic Flash
4. Any Preemption

3.4.3 Initialization

Initialization shall occur under either of the following conditions:

1. Restoration of power after a defined power interruption.
2. Activation of **External Start** input.

A program entry for initialization shall be provided to cause the CU to start at the beginning of the defined signal plan interval.

As part of the initialization routine, calls shall be placed on all actuated movements and retained until serviced.

3.4.4 Actuated Movements

The CU shall provide actuated operation to the extent that the signal sequence may be dependent on vehicle and/or pedestrian detector actuations.

3.4.4.1 PROVISION FOR STORING A DEMAND

There shall be a provision for storing a call for vehicle service on four vehicle movements when the specific movement is not displaying a **Green** indication. The vehicle memory feature shall be capable of being disabled via program entry.

There shall be a provision for storing a call for pedestrian service on each of the four movements, when the movement is not displaying a **Walk** indication.

3.4.4.2 PLACEMENT OF VEHICLE RECALL

Means shall be provided, via program entry, to place a recurring demand for vehicle service on the movement when that movement is not in its **Green** interval.

3.4.4.3 PLACEMENT OF PEDESTRIAN RECALL

Means shall be provided, via program entry, to place a recurring demand for pedestrian service on the movement when that movement is not in its **Walk** interval.

3.4.5 External Interface

The CU shall operate with an external interface as follows:

3.4.5.1 PIN CONNECTIONS

A Type P2 CU shall provide input-output connector pin terminations in accordance with the following:

Connector "A" Pin/Function
55 Pin (Plug) Type # -22-55P

Pin	Function	I/O
A	Fault Monitor	[O]
B	+24 VDC (External)	[O]
C	Voltage Monitor	[O]
D	Vehicle 1 Red	[O]
E	Pedest 1 Dont Walk	[O]
F	Vehicle 2 Red	[O]
G	Pedest 2 Dont Walk	[O]
H	Pedest 2 Ped Clear	[O]
J	Pedest 2 Walk	[O]
K	Vehicle 2 Detector	[I]
L	Pedest 2 Detector	[I]
M	Mode* Input 2	[I]
N	Stop Time	[I]
P	Reserved	[I]
R	External Start	[I]
S	Interval Advance	[I]
T	Ind. Lamp Control	[I]
U	AC Neutral	[I]
V	Earth Ground	[I]
W	Logic Ground	[O]
X	Flashing Logic	[O]
Y	Status Bit C	[O]
Z	Vehicle 1 Yellow	[O]
a	Pedest 1 Ped Clear	[O]
b	Vehicle 2 Yellow	[O]
c	Vehicle 2 Green	[O]
d	Mode* Output 10	[O]
e	Mode* Output 2	[O]
f	Vehicle 1 Detector	[I]
g	Pedest 1 Detector	[I]
h	Mode* Input 1	[I]
i	Force Off	[I]
j	External Recall	[I]
k	Man Cont Enable	[I]
m	Reserved	[I]
n	Test A	[I]
p	AC Line	[I]

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Pin	Function	I/O
q	I/O Mode Bit A	[I]
r	Status Bit B	[O]
s	Vehicle 1 Green	[O]
t	Pedest 1 Walk	[O]
u	Mode* Output 9	[O]
v	Mode* Input 10	[I]
w	Reserved	[I]
x	Reserved	[I]
y	I/O Mode Bit B	[I]
z	Reserved	[I]
AA	Test B	[I]
BB	Reserved	[I]
CC	Status Bit A	[O]
DD	Mode* Output 1	[O]
EE	Mode* Input 9	[I]
FF	Reserved	[I]
GG	Reserved	[I]
HH	I/O Mode Bit C	[I]

Connector "B" Pin/Function
55 Pin (Socket) Type # -22-55S

Pin	Function	I/O
A	Mode* Output 5	[O]
B	Preempt 2 Detector	[I]
C	Mode* Output 6	[O]
D	Vehicle 3 Green	[O]
E	Vehicle 3 Yellow	[O]
F	Vehicle 3 Red	[O]
G	Vehicle 4 Red	[O]
H	Pedest 4 Ped Clear	[O]
J	Pedest 4 Dont Walk	[O]
K	Mode* Output 12	[O]
L	Vehicle 4 Detector	[I]
M	Pedest 4 Detector	[I]
N	Vehicle 3 Detector	[I]
P	Pedest 3 Detector	[I]
R	Mode* Input 7	[I]
S	Mode* Input 6	[I]
T	Mode* Input 13	[I]
U	Mode* Input 5	[I]
V	Reserved	[I]
W	Preempt 4 Detector	[I]
X	Preempt 5 Detector	[I]
Y	Pedest 3 Walk	[O]
Z	Pedest 3 Ped Clear	[O]
a	Pedest 3 Dont Walk	[O]
b	Vehicle 4 Green	[O]
c	Vehicle 4 Yellow	[O]
d	Pedest 4 Walk	[O]
e	Mode* Output 4	[O]
f	Mode* Output 8	[O]
g	Mode* Input 8	[I]
h	Mode* Input 4	[I]
i	Mode* Input 3	[I]
j	Mode* Input 11	[I]
k	Mode* Input 14	[I]
m	Mode* Input 15	[I]
n	Mode* Input 16	[I]
p	Vehicle A Yellow	[O]
q	Vehicle A Red	[O]
r	Mode* Output 11	[O]
s	Mode* Output 3	[O]
t	Mode* Output 7	[O]
u	Vehicle D Red	[O]
v	Preempt 6 Detector	[I]
w	Vehicle D Green	[O]
x	Mode* Input 12	[I]
y	Free Mode	[I]
z	Reserved	[I]
AA	Vehicle A Green	[O]
BB	Vehicle B Yellow	[O]
CC	Vehicle B Red	[O]
DD	Vehicle C Red	[O]
EE	Vehicle D Yellow	[O]
FF	Vehicle C Green	[O]
GG	Vehicle B Green	[O]
HH	Vehicle C Yellow	[O]

* Input/Output Functions are dependent on the I/O Mode Bit inputs. See 3.4.5.2 for a definition of the function assigned to each mode.

3.4.5.2 INPUTS

1. **AC Line**—Current protected side of 120 VAC 60 Hertz power source within the CU.

   The CU shall have a front panel mounted over-current protection device in the 120 VAC input to the unit.
2. **AC Neutral**—Unfused and unswitched side of 120 VAC 60 Hertz power source taken from neutral output of AC power source.

   This input must not be connected to **Logic Ground** or **Earth Ground** within the CU.
3. **Earth Ground**—Terminal for connection to the chassis of the CU. Earth Ground shall be electrically connected to the shell of the connector(s) where applicable. This input shall not be connected to **Logic Ground** or **AC Neutral** within the CU.
4. **External Start**—An input to cause the CU to revert to its programmed initialization interval upon application. Upon removal of this input the CU shall commence normal timing.
5. **Interval Advance**—A complete On-Off operation of this input shall cause immediate termination of the interval in process of timing. The CU shall select the next interval to service based on it's normal sequence control method.

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Interval Advance shall be used in conjunction with **Manual Control Enable** to produce manual control of the programmable variable intervals with the remaining intervals self timing (see **Manual Control Enable**).

Interval Advance shall be used in conjunction with **Stop Time** to advance through all serviceable intervals. The termination of all signal plan intervals will be controlled by the **Interval Advance** input.

6. **Stop Timing**—An input which when activated causes cessation of CU interval timing for the duration of such activation. Upon removal of activation from this input, all portions which were timing will resume timing.

   During stop timing, the CU shall not terminate any signal plan, interval or interval portion, except by activation of the **Interval Advance** input.
7. **Force Off**—An input when active causes the termination of the signal plan variable interval subject to the completion of any programmed signal plan Minimum Interval timing.
8. **Manual Control Enable**—An input to place calls on all actuated movements, stop CU timing in programmed variable intervals, and inhibit the operation of **Interval Advance** during all other intervals.
9. **External Recall**—Input to place a recurring demand for service on all actuated vehicle movements.
10. **Indicator Lamp Control**—Input to disable CU indicators.

    The CU might not employ this input. (Authorized Engineering Information)
11. **Test Input** (Two per Unit)—Test Input, two per unit, for manufacturer's use only.
12. **Pattern Inputs**—The CU shall select the pattern to be used, according to the current status of the Timing Plan and Offset requests. In the applicable mode, seven inputs for a hardwire type interconnect interface shall be available.

    Pattern inputs shall be interpreted as command requests in accordance with Tables 3.4-1 and 3.4-2.

Table 3.4-1
TIMING PLAN

Command Request	TP A Input	TP B Input	TP C Input	TP D Input	Reference
TP 00	OFF	OFF	OFF	OFF	Dial 1 Split 1
TP 01	OFF	OFF	ON	OFF	Dial 1 Split 2
TP 02	OFF	OFF	OFF	ON	Dial 1 Split 3
TP 03	OFF	OFF	ON	ON	Dial 1 Split 4
TP 04	ON	OFF	OFF	OFF	Dial 2 Split 1
TP 05	ON	OFF	ON	OFF	Dial 2 Split 2
TP 06	ON	OFF	OFF	ON	Dial 2 Split 3
TP 07	ON	OFF	ON	ON	Dial 2 Split 4
TP 08	OFF	ON	OFF	OFF	Dial 3 Split 1
TP 09	OFF	ON	ON	OFF	Dial 3 Split 2
TP 10	OFF	ON	OFF	ON	Dial 3 Split 3
TP 11	OFF	ON	ON	ON	Dial 3 Split 4
TP 12	ON	ON	OFF	OFF	Dial 4 Split 1
TP 13	ON	ON	ON	OFF	Dial 4 Split 2
TP 14	ON	ON	OFF	ON	Dial 4 Split 3
TP 15	ON	ON	ON	ON	Dial 4 Split 4

For the purpose of utilization in an existing traditional interconnect system, a Reference with Dial and Split numbers is provided.

Table 3.4-2
OFFSET

Command Request	Off 1 Input	Off 2 Input	Off 3 Input
Offset 1	ON	OFF	OFF
Offset 2	OFF	ON	OFF
Offset 3	OFF	OFF	ON
Sync	OFF	OFF	OFF

Voltage Levels: OFF = +24V; ON = 0V

13. **Signal Plan** Inputs—The CU shall select the signal plan to be used, according to the current status of the **Signal Plan** requests. In the applicable mode, two inputs for a hardwire type interconnect interface shall be available.

    Signal Plan inputs shall be interpreted as command requests in accordance with Tables 3.4-3.

Table 3.4-3
SIGNAL PLAN

Command Request	Sig Plan A Input	Sig Plan B Input
Signal Plan 1	OFF	OFF
Signal Plan 2	ON	OFF
Signal Plan 3	OFF	ON
Signal Plan 4	ON	ON

Voltage Levels: OFF = +24V; ON = 0V

14. **Vehicle Detector**—Provision to enter a vehicle call into the CU.

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Vehicle Detector inputs shall be provided as follows:

a. Type P1 CU—10

b. Type P2 CU—4 (10 in the applicable mode)

As a minimum, each **Vehicle Detector** input shall be enabled by assignment to any one movement, via program entry. Each shall be capable of Delay, and Extension as follows:

a. Delay—The vehicle detector actuation (input recognition) shall be capable of being delayed, by an adjustable program entered time (0–255 seconds in increments of 1 second), when the movement is not green. Once the actuation has been present for the delay time it shall be continued for as long as it is present.

b. Extension—The vehicle detector actuation (input duration) shall be capable of being extended from the point of termination by an adjustable program entered time (0–25.5 seconds in increments of 0.1 second), when the movement is green.

The special vehicle detector functions shall be capable of being used in any combination.

As a minimum, the following number of **Vehicle Detector** inputs shall be capable of assignment to a System Detector function, via program entry.

a. Type P1 Unit—8

b. Type P2 Unit—6 (in the applicable mode)

15. **Pedestrian Detector**—Provision to enter a pedestrian call into the CU.

As a minimum, each **Pedestrian Detector** input shall be enabled by assignment to any one movement, via program entry.

16. **System Address Bits**—Five System Address inputs shall be provided. The CU shall respond to the system address defined by the binary decoding of these five inputs.

17. **Input/Output Mode** (Three per Unit)—The CU shall select the input/output function of specific hardware I/O based on the current status of these three inputs.

I/O Mode Bits (3 Per Unit)

Mode	Bit States			State
#	A	B	C	Names
0	OFF	OFF	OFF	Not Used
1	ON	OFF	OFF	Hardwire Interconnect
2	OFF	ON	OFF	System Interface
3	ON	ON	OFF	Hardwire Interconnect
4	OFF	OFF	ON	Reserved
5	ON	OFF	ON	Reserved
6	OFF	ON	ON	Manufacturer Specific
7	ON	ON	ON	Manufacturer Specific

Voltage Levels: OFF = +24; ON = 0V

a. Mode 0 Input/Output Functions

Mode 0 is not used. The CU shall not recognize any mode dependent input as valid nor shall it provide a valid output on any mode dependent output when Input/Output Mode 0 is active.

b. Mode 1 Input/Output Functions

Inputs:

Pin	Function
A-h	Preempt 1
A-M	Preempt 3
B-i	Signal Plan A
Pin	**Function**
B-h	Signal Plan B
B-U	Reserved
B-S	Reserved
B-R	Timing Plan C
B-g	Timing Plan D
A-EE	Dimming Enable
A-v	Automatic Flash
B-j	Timing Plan A
B-x	Timing Plan B
B-T	Offset 1
B-k	Offset 2
B-m	Offset 3
B-n	TBC On Line

Outputs:

Pin	Function
A-DD	Preempt 1 Status
A-e	Preempt 3 Status
B-s	TBC Auxiliary 1
B-e	TBC Auxiliary 2
B-A	Preempt 2 Status
B-C	Preempt 4 Status
B-t	Preempt 5 Status
B-f	Preempt 6 Status
A-u	Reserved
A-d	Automatic Flash
B-r	TBC Auxiliary 3
B-K	Reserved

c. Mode 2 Input/Output Functions

Inputs:

Pin	Function
A-h	Preempt 1
A-M	Preempt 3
B-i	Vehicle Detector 5
B-h	Vehicle Detector 6
B-U	Vehicle Detector 7
B-S	Vehicle Detector 8
B-R	Vehicle Detector 9
B-g	Vehicle Detector 10
A-EE	Dimming Enable

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Pin	Function
A-v	Local Flash Status
B-j	Address Bit 0
B-x	Address Bit 1
B-T	Address Bit 2
B-k	Address Bit 3
B-m	Address Bit 4
B-n	MMU Flash Status

Outputs:

Pin	Function
A-DD	Preempt 1 Status
A-e	Preempt 3 Status
Pin	**Function**
B-s	TBC Auxiliary 1
B-e	TBC Auxiliary 2
B-A	Preempt 2 Status
B-C	Preempt 4 Status
B-t	Preempt 5 Status
B-f	Preempt 6 Status
A-u	Reserved
A-d	Automatic Flash
B-r	TBC Auxiliary 3
B-K	Reserved

c. Mode 3 Input/Output Functions

Inputs:

Pin	Function
A-h	Preempt 1
A-M	Preempt 3
B-i	Signal Plan A
B-h	Signal Plan B
B-U	Reserved
B-S	Reserved
B-R	Timing Plan C
B-g	Timing Plan D
A-EE	Dimming Enable
A-v	Automatic Flash
B-j	Timing Plan A
B-x	Timing Plan B
B-T	Offset 1
B-k	Offset 2
B-m	Offset 3
B-n	TBC On Line

Outputs:

Pin	Function
A-DD	Timing Plan A
A-e	Timing Plan B
B-s	TBC Auxiliary 1
B-e	TBC Auxiliary 2
B-A	Timing Plan C
B-C	Timing Plan D
B-t	Offset 1
Pin	**Function**
B-f	Offset 2
A-u	Offset 3
A-d	Automatic Flash
B-r	Signal Plan A
B-K	Signal Plan B

d. Mode 4 and 5 Input/Output Functions

Mode 4 and 5 are reserved for future definition and use by NEMA. The CU shall not recognize any mode dependent input as valid nor shall it provide a valid output on any mode dependent output when one of these Input/Output Modes is active.

e. Mode 6 and 7 Input/Output Functions

Mode 6 and 7 are for manufacturer specific applications.

A Terminal and Facilities wired to utilize Mode 6 or Mode 7 may not be compatible with other manufacturer's CUs. (Authorized Engineering Information)

18. Free Mode—An input when activated causes the CU to operate in Free Mode (See Section 3.4.2.7).

3.4.5.3 OUTPUTS

1. **Logic Ground**—Voltage reference point and current return for CU input and output logic circuits. This output must not be connected to AC Neutral or Earth Ground within the CU.
2. **Fault Monitor**—An open collector output which is maintained true (low state) as long as the voltages within the CU do not drop below predetermined levels required to provide normal operation.

   The output will also be **false** (hi state) during CU generated flash modes as defined elsewhere in this section.
3. **CU Voltage Monitor** (Type P2 Only)—An open collector output which is maintained **true** (low state) as long as the voltages within the CU do not drop below predetermined levels required to provide normal operation.

   The output will also be **false** (hi state) during CU generated flash modes as defined elsewhere in this section.

   This output operates concurrently with Fault Monitor output except during periods of No Fault Flash (i.e., Startup Flash, Automatic Flash and Preempt Flash).
4. **Regulated 24 Volts DC For External Use** (Type P2 Only)—Positive 24 ± 2 volts DC shall be regulated over an AC line voltage variation from 89 to 135 volts from no-load to full-load. Current capability shall be 500 milliamperes continuous with less than 0.5 volt peak-to-peak ripple.

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5. **Flashing Logic Output** (Type P2 Only)—Alternating True/False logic output at 1 pulse per second repetition rate with 50 ± 2 percent duty cycle. In its **False** state, this output shall be capable of providing 50 milliamperes of current. In its **True** state, this output shall be capable of sinking 200 milliamperes. This output shall switch within 5 degrees of the zero crossover point of the AC line.
6. **Load Switch Drivers, Vehicle** (Three Per Group)—Provision for separate **Green, Yellow**, and **Red** outputs for each basic group. The three outputs shall energize the appropriate signal load switching circuit to result in a **Green, Yellow**, or **Red** indication for the duration of such required indication.
7. **Load Switch Drivers, Pedestrian** (Three Per Group)—Provision of separate **Walk, Pedestrian Clearance**, and **Dont Walk** outputs for each pedestrian movement. The three outputs shall energize the appropriate pedestrian signal load switching circuit to result in a **Walk, Pedestrian Clearance**, or **Dont Walk** indication. The **Dont Walk** output shall flash only during the **Pedestrian Clearance** interval as shown in Figure 3.5-8.
8. **Pattern Outputs**—In the applicable mode, seven outputs for master type interconnect interface drivers shall be available. The outputs shall echo the active pattern. All outputs shall be constantly **ON** when active except offset which is **OFF** for a minimum of 3 seconds or 3% of the cycle once each cycle beginning at the "0" point of the cycle.

   Pattern outputs shall be interpreted as command requests in accordance with Tables 3.4-1, 3.4-2, and 3.4-3.
9. **Signal Plan** Outputs—In the applicable mode, two outputs for master type interconnect interface drivers shall be available. The outputs shall echo the active signal plan.

   Signal Plan outputs shall be interpreted as command requests in accordance with Table 3.4-4.
10. **Coded Status Bits**—Only one of the coded status codes shall be active when the following conditions are present in the CU:

Table 3.4-4
CODED STATUS BITS
(3 PER UNIT)

Code #	Bit States A	B	C	State Names
0	OFF	OFF	OFF	Mininum
1	ON	OFF	OFF	Variable
2	OFF	ON	OFF	Not Used
3	ON	ON	OFF	Not Used
4	OFF	OFF	ON	Not Used
5	ON	OFF	ON	Not Used
6	OFF	ON	ON	Not Used
7	ON	ON	ON	Undefined

Voltage Levels: OFF= +24V; ON = 0V

Code 0—Minimum—When timing the Signal Plan Minimum portion of the Interval.

Code 1—Variable—That portion of the interval following the completion of the Signal Plan Minimum time.

Code 2 - Not Used
Code 3 - Not Used
Code 4 - Not Used
Code 5 - Not Used
Code 6 - Not Used
Code 7 - Undefined

3.4.6 Priority Of Input Functions

The priority of input functions shall be in the following order:

1. Power-Up
2. External Start
3. Preemption
4. Interval Advance
5. Stop Time
6. Automatic Flash
7. Manual Control Enable
8. Force Off

Lower priority inputs shall condition those of higher priority as defined elsewhere in this standard.

Patterns and signal plans are capable of being selected based on program entry, Interconnect Inputs, Time Base Control events, and a System Interface. The pattern and signal plan select priority shall be as follows:

1. Program Entry
2. System Interface
3. Time Base Control Event
4. Interconnect Inputs

When the Time Base Control **On-line** input is active, the Time Base Control event priority will be lower than Interconnect Inputs. Should the Sync Monitor diagnostic determine the Interconnect Offset to be invalid, a Time Base Control event may control.

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3.4.7 Indications

Indications shall be provided on the display and appropriately identified to facilitate the determination of the operation of the CU. These indications shall consist of the following as a minimum requirement:

The indications shall provide for the simultaneous (i.e., concurrent) presentation, where concurrent states exists, of the following states/functions:

Current Status

1. Running Pattern, Control Source
2. Running Pattern, Timing Plan plus Offset
3. Correction In Progress
4. System Zero
5. Cycle Counter
6. Interval In Service
7. Interval Counter
8. Presence of vehicle call
9. Presence of pedestrian call

3.5 ACTUATED CONTROL

The Standards in Clause 3.5 respond to the need for the functional interchangeability of Solid State Traffic Signal CUs, actuated Type (2 through 8 phase). Interchangeability of equipment manufactured in conformance with these standards has been promoted by connector plug compatibility.

Interchangeability of equipment can be achieved only when units are configured to produce the same functional operation utilizing exactly the same inputs and outputs.

Configurations 'A1' and 'A2' CUs (see Section 3.2) shall provide functional capability to meet the actuated control requirements contained herein.

3.5.1 DEFINITIONS

These definitions define the nomenclature frequently used in this part of the Standard Publication.

3.5.1.1 RING

A ring consists of two or more sequentially timed and individually selected conflicting phases so arranged as to occur in an established order.

3.5.1.2 BARRIER (COMPATIBILITY LINE)

A barrier (compatibility line) is a reference point in the preferred sequence of a multi-ring CU at which all rings are interlocked. Barriers assure there will be no concurrent selection and timing of conflicting phases for traffic movement in different rings. All rings cross the barrier simultaneously to select and time phases on the other side.

3.5.1.3 MULTI-RING CONTROLLER UNIT

A multi-ring CU contains two or more interlocked rings which are arranged to time in a preferred sequence and to allow concurrent timing of all rings, subject to the restraint in 3.5.1.2. A dual-ring CU is illustrated in Figure 3.5-1.

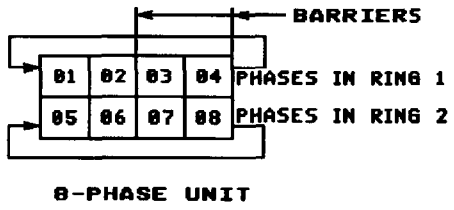

Figure 3.5-1
DUAL RING CONTROLLER UNIT

3.5.1.4 SINGLE-RING CONTROLLER UNIT

A single-ring CU contains two or more sequentially timed and individually selected conflicting phases so arranged as to occur in an established order. Single-ring CUs are illustrated in Figure 3.5-2.

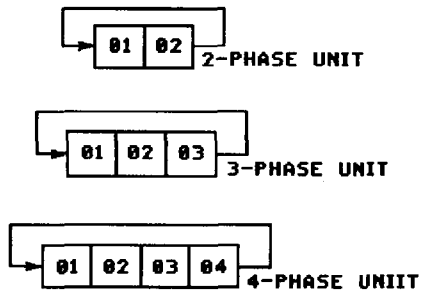

Figure 3.5-2
SINGLE RING CONTROLLER UNIT

3.5.1.5 DUAL ENTRY

Dual entry is a mode of operation (in a multi-ring CU) in which one phase in each ring must be in service. If a call does not exist in a ring when it crosses the barrier, a phase is selected in that ring to be activated by the CU in a predetermined manner.

3.5.1.6 SINGLE ENTRY

Single entry is a mode of operation (in a multi-ring CU) in which a phase in one ring can be selected and timed

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alone if there is no demand for service in a nonconflicting phase on the parallel ring(s).

3.5.1.7 PEDESTRIAN RECYCLE

Pedestrian recycle is any start of pedestrian service after the start of the associated phase **Green**.

3.5.1.8 PREFERRED SEQUENCE

Preferred sequence is the normal order of phase selection within a ring with calls on all phases.

3.5.2 General

Inputs, outputs, functions, and programming controls are separated into the following three categories:

1. Per phase (3.5.3)
2. Per ring (3.5.4)
3. Per unit (3.5.5)

3.5.2.1 PIN CONNECTIONS

A Type A2 CU shall provide input/output connector pin terminations shall be in accordance with the following:

Connector "A" Pin/Function
55 Pin (Plug) Type # -22-55P

Pin	Function	I/O
A	Fault Monitor	[O]
B	+24 VDC (External)	[O]
C	Voltage Monitor	[O]
D	Phase 1 Red	[O]
E	Phase 1 Dont Walk	[O]
F	Phase 2 Red	[O]
G	Phase 2 Dont Walk	[O]
H	Phase 2 Ped Clear	[O]
J	Phase 2 Walk	[O]
K	Vehicle Detector 2	[I]
L	Pedest Detector 2	[I]
M	Mode* Input 2	[I]
N	Stop Time (1)	[I]
P	Inhibit Max Term (1)	[I]
R	External Start	[I]
S	Interval Advance	[I]
T	Ind Lamp Control	[I]
U	AC Neutral	[I]
V	Earth Ground	[I]
W	Logic Ground	[O]
X	Flashing Logic Out	[O]
Y	Status Bit C (1)	[O]
Z	Phase 1 Yellow	[O]
a	Phase 1 Ped Clear	[O]
b	Phase 2 Yellow	[O]
c	Phase 2 Green	[O]
d	Mode* Output 18	[O]
e	Mode* Output 2	[O]
f	Vehicle Detector 1	[I]
g	Pedest Detector 1	[I]
h	Mode* Input 1	[I]
i	Force Off (1)	[I]
j	External Min Recall	[I]
k	Manual Cont Enable	[I]
m	Call To NA I	[I]
n	Test A	[I]
p	AC Line	[I]
q	I/O Mode Bit A	[I]
r	Status Bit B (1)	[O]
s	Phase 1 Green	[O]
t	Phase 1 Walk	[O]
u	Mode* Output 17	[O]
v	Mode* Input 18	[I]
w	Omit Red Clear (1)	[I]
x	Red Rest (1)	[I]
y	I/O Mode Bit B	[I]
z	Call To NA II	[I]
AA	Test B	[I]
BB	Walk Rest Modifier	[I]
CC	Status Bit A (1)	[O]
DD	Mode* Output 1	[O]
EE	Mode* Input 17	[I]
FF	Pedest Recycle (1)	[I]
GG	Max II Selection (1)	[I]
HH	I/O Mode Bit C	[I]

Connector "B" Pin/Function
55 Pin (Socket) Type # -22-55S

Pin	Function	I/O
A	Mode* Output 9	[O]
B	Preempt 2 Detector	[I]
C	Mode* Output 10	[O]
D	Phase 3 Green	[O]
E	Phase 3 Yellow	[O]
F	Phase 3 Red	[O]
G	Phase 4 Red	[O]
H	Phase 4 Ped Clear	[O]
J	Phase 4 Dont Walk	[O]
K	Mode* Output 20	[O]
L	Vehicle Detector 4	[I]
M	Pedest Detector 4	[I]
N	Vehicle Detector 3	[I]
P	Pedest Detector 3	[I]
R	Mode* Input 11	[I]
S	Mode* Input 10	[I]
T	Mode* Input 21	[I]
U	Mode* Input 9	[I]
V	Pedest Recycle (2)	[I]
W	Preempt 4 Detector	[I]
X	Preempt 5 Detector	[I]

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Pin	Function	I/O
Y	Phase 3 Walk	[O]
Z	Phase 3 Ped Clear	[O]
a	Phase 3 Dont Walk	[O]
b	Phase 4 Green	[O]
c	Phase 4 Yellow	[O]
d	Phase 4 Walk	[O]
e	Mode* Output 4	[O]
f	Mode* Output 12	[O]
g	Mode* Input 12	[I]
h	Mode* Input 4	[I]
i	Mode* Input 3	[I]
j	Mode* Input 19	[I]
k	Mode* Input 22	[I]
m	Mode* Input 23	[I]
n	Mode* Input 24	[I]
p	OL A Yellow	[O]
q	OL A Red	[O]
r	Mode* Output 19	[O]
s	Mode* Output 3	[O]
t	Mode* Output 11	[O]
u	OL D Red	[O]
v	Preempt 6 Detector	[I]
w	OL D Green	[O]
x	Mode* Input 20	[I]
y	Free (No Coord)	[I]
z	Max II Selection (2)	[I]
AA	OL A Green	[O]
BB	OL B Yellow	[O]
CC	OL B Red	[O]
DD	OL C Red	[O]
EE	OL D Yellow	[O]
FF	OL C Green	[O]
GG	OL B Green	[O]
HH	OL C Yellow	[O]

Connector "C" Pin/Function
61 Pin (Socket) Type # -24-61S

Pin	Function	I/O
A	Status Bit A (2)	[O]
B	Status Bit B (2)	[O]
C	Phase 8 Dont Walk	[O]
D	Phase 8 Red	[O]
E	Phase 7 Yellow	[O]
F	Phase 7 Red	[O]
G	Phase 6 Red	[O]
H	Phase 5 Red	[O]
J	Phase 5 Yellow	[O]
K	Phase 5 Ped Clear	[O]
L	Phase 5 Dont Walk	[O]
M	Mode* Output 13	[O]
N	Mode* Output 5	[O]
P	Vehicle Detector 5	[I]
R	Pedest Detector 5	[I]
S	Vehicle Detector 6	[I]
T	Pedest Detector 6	[I]
U	Pedest Detector 7	[I]
V	Vehicle Detector 7	[I]
W	Pedest Detector 8	[I]
X	Mode* Input 8	[I]
Y	Force Off (2)	[I]
Z	Stop Time (2)	[I]
a	Inhibit Max Term (2)	[I]
b	Test C	[I]
c	Status Bit C (2)	[O]
d	Phase 8 Walk	[O]
e	Phase 8 Yellow	[O]
f	Phase 7 Green	[O]
g	Phase 6 Green	[O]
h	Phase 6 Yellow	[O]
i	Phase 5 Green	[O]
j	Phase 5 Walk	[O]
k	Mode* Output 21	[O]
m	Mode* Input 5	[I]
n	Mode* Input 13	[I]
p	Mode* Input 6	[I]
q	Mode* Input 14	[I]
r	Mode* Input 15	[I]
s	Mode* Input 16	[I]
t	Vehicle Detector 8	[I]
u	Red Rest Mode (2)	[I]
v	Omit Red Clear (2)	[I]
w	Phase 8 Ped Clear	[O]
x	Phase 8 Green	[O]
y	Phase 7 Dont Walk	[O]
z	Phase 6 Dont Walk	[O]
AA	Phase 6 Ped Clear	[O]
BB	Mode* Output 22	[O]
CC	Mode* Output 6	[O]
DD	Mode* Output 14	[O]
EE	Mode* Input 7	[I]
FF	Mode* Output 24	[O]
GG	Mode* Output 8	[O]
HH	Mode* Output 16	[O]
JJ	Phase 7 Walk	[O]
KK	Phase 7 Ped Clear	[O]
LL	Phase 6 Walk	[O]
MM	Mode* Output 23	[O]
NN	Mode* Output 7	[O]
PP	Mode* Output 15	[O]

* Input/Output Functions are dependent on the I/O Mode Bit inputs. See 3.5.5.6(13) for a definition of the function assigned to each mode.

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3.5.3 Per Phase

The following inputs, outputs, functions, and programming controls shall be provided on a per phase basis:

3.5.3.1 TIME SETTINGS

The following functions, with the associated minimum timing ranges and maximum increments, shall be provided as a minimum when required by the application. For timing accuracy see 3.13.1.

Function	Range, Seconds	Increments, Seconds
Min Green	1–255	1
Passage Time	0–25.5	0.1
Maximum 1	1–255	1
Maximum 2	1–255	1
Yellow Change	3–25.5	0.1
Red Clearance	0–25.5	0.1
Walk	0–255	1
Ped Clearance	0–255	1
Added Initial	0–25.5	per Actuation
Time to Reduce	1–255	1
Time Before Reduction	1–255	1
Minimum Gap	0–25.5	0.1

Zero shall be satisfied by any time between zero and 100 milliseconds.

3.5.3.2 PHASE INTERVALS

1. **Green** Interval—Actuated Phase
   a. Without Volume Density—The **Green** interval is a variable interval dependent upon vehicle actuations. The **Green** interval time shall be limited by the **Maximum Green** time function which shall commence timing upon registration of a serviceable conflicting call. The **Minimum Green** time shall not be preempted by a **Maximum Green** termination.

   Three time settings shall be provided for determination of **Green** timing on an actuated phase without volume density.

   (1) **Minimum Green**—The first timed portion of the Green interval which may be set in consideration of the storage of vehicles between the zone of detection for the approach vehicle detector(s) and the stop line.

   (2) **Passage Time** (Vehicle Interval, Preset Gap)—The extensible portion of the **Green** shall be a function of vehicle actuations that occur during the **Green** interval. The phase shall remain in the extensible portion of the **Green** interval as long as the passage timer is not timed out.

   The timing of this portion of the **Green** interval shall be reset with each subsequent vehicle actuation and shall not commence to time again until the vehicle actuation is removed from the CU. The duration of the **Green** interval shall be subject to the limit of the **Maximum Green**.

   (3) **Maximum Green**—This time setting shall determine the maximum length of time this phase may be held Green in the presence of a serviceable conflicting call. In the absence of a serviceable conflicting call the **Maximum Green** timer shall be held reset.

   b. With Volume Density—In addition to **Minimum Green, Passage Time,** and **Maximum Green** timing functions, phases provided with **Volume Density** operation shall include **Variable Initial** timings and **Gap Reduction** timings. The effect on the **Initial** timing shall be to increase the timing in a manner dependent upon the number of vehicle actuations stored on this phase while its signal is displaying **Yellow** or **Red**. The effect on the extensible portion shall be to reduce the allowable gap between successive vehicle actuations by decreasing the extension time in a manner dependent upon the time waiting of vehicles on a conflicting phase.

   (1) **Variable Initial** (See Figure 3.5-3). The **Variable Initial** timing period shall be determined by an interrelationship of two time settings as described below:

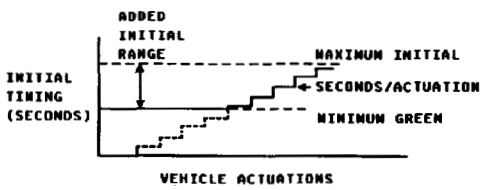

Figure 3.5-3
VARIABLE INITIAL TIMING

(a) **Minimum Green** setting shall determine the minimum **Variable Initial** time period.

(b) **Seconds/Actuation** setting shall determine the time by which the **Variable Initial** time period will be increased from zero with each vehicle actuation received during the associated phase **Yellow** and **Red** intervals.

(c) The maximum of the **Variable Initial** timing period shall be settable (on a per-phase basis) in the range of 0–255 seconds with increments of

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1 second. The maximum **Variable Initial** setting shall be subordinate to **Minimum Green** time setting.

(d) Initial timing shall equal (seconds/actuation) multiplied by (number of actuations) within the constraint of **Maximum Initial** and shall be not less than **Minimum Green.**

(2) **Gap Reduction** (See Figure 3.5-4)—The **Gap Reduction** function shall be accomplished by means of the following functional settings:

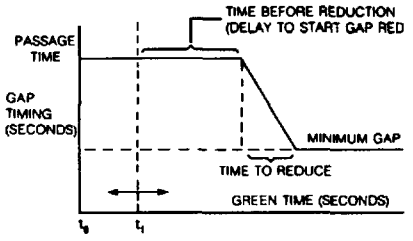

Figure 3.5-4
GAP REDUCTION

Figure 3.5-4 Notes
(1) t_0 = Start of phase **Green.**
(2) t_1 = Registration of serviceable conflicting call.
(3) **Time Before Reduction** shall not start timing before t_1.
(4) **Maximum** timer start shall be conditional upon being in the **Green** interval and registration of a serviceable conflicting call—vehicle or pedestrian.
(5) **Passage Time** portion of **Green** interval must time concurrently with **Initial** subject to vehicle actuations.

(a) **Time Before Reduction**
(b) **Passage Time**
(c) **Minimum Gap**
(d) **Time To Reduce**

The **Time Before Reduction** period shall begin when the phase is **Green** and there is a serviceable conflicting call. If the serviceable conflicting call is withdrawn while timing this period, the timer shall be reset and remain reset until the next serviceable conflicting call is received.

Upon completion of the **Time Before Reduction** period, the linear reduction of the allowable gap from the **Passage Time** level shall begin.

The rate of reduction shall be based on the setting of the **Passage Time, Minimum Gap,** and **Time To Reduce** controls. This method shall reduce the allowable gap at a rate equal to the difference between the **Passage Time** and **Minimum Gap** setting divided by the setting of the **Time To Reduce** control.

The reduction of the allowable gap shall continue until the gap reaches a value equal to or less than the minimum gap as set on the **Minimum Gap** control after which the allowable gap shall remain fixed at the values set on the **Minimum Gap** control. In the presence of a continuous vehicle actuation, the phase shall not gap out even if the gap is reduced to zero (i.e., **Minimum Gap** set at zero).

If at any time the serviceable conflicting call is withdrawn, the gap shall revert to the **Passage Time** setting value, and the **Time Before Reduction** period timer shall be reset and remain reset until the next serviceable conflicting call is received.

2. Pedestrian Timing, Concurrent

Concurrent pedestrian timing shall be permitted in association with any mode of vehicle signal timing. Two time settings shall be required:

a. **Walk**—This shall control the amount of time the **Walk** indication shall be displayed.
b. **Pedestrian Clearance**—This shall control the duration of the **Pedestrian Clearance** output and the flashing period of the **Dont Walk** output.

When a pedestrian call is stored in pedestrian memory and pedestrian indications are concurrent with an associated vehicle phase, the pedestrian sequence shall commence service when entering the vehicle **Green** of that phase unless the **Pedestrian Omit** line is activated.

During the display of the **Walk** and **Pedestrian Clearance** indications, a concurrent **Green** vehicle indication shall be shown. It shall be possible to recycle the pedestrian indications in response to succeeding pedestrian calls for service subject to absence of serviceable conflicting calls (vehicle or pedestrian) and nonactivation of the **Pedestrian Omit** line.

3. Actuated Phase Operating in the Nonactuated Mode

The actuated phases that are converted to **Nonactuated** operation by activation of either the **Call To Nonactuated Mode** inputs shall have a permanent demand placed for vehicle and pedestrian service. Each such phase shall be equipped with pedestrian timing capability.

These phases shall be considered to have the four **Green** states indicated in Figure 3.5-5.

a. State A shall be the minimum timing state. The duration of State A shall be equal to the **Walk** time setting. Signal indications for State A shall be **Green** and **Walk.**
b. State B shall be a state immediately following the minimum timing state. The CU shall dwell in this state in the presence of a **Hold** signal or when the **Walk Rest Modifier** is active and no serviceable

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STATE A - CODE 0* WALK
STATE B - CODE 1* WALK HOLD
STATE C - CODE 2* PEDESTRIAN CLEARANCE
STATE D - CODE 3* GREEN REST

* Coded Status Bits Code

Figure 3.5-5
ACTIVATED PHASE OPERATING IN THE NONACTIVATED MODE

conflicting call exists. The signal indications shall remain in **Green** and **Walk**. The CU shall leave this state when the **Hold** input is not active; or when the **Hold** input is active, a serviceable conflicting call exists, and the **Force-Off** input is activated. If the phase **Hold** is active and the **Force-Off** is activated when the phase is active and a serviceable conflicting call does not exist, the CU shall continue to dwell in State B of the phase.

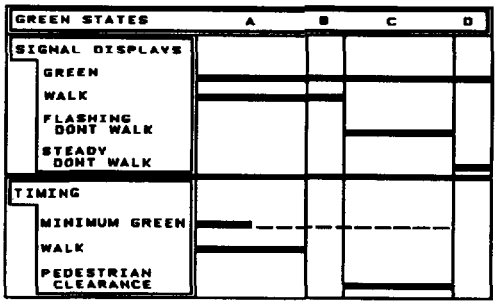
c. State C shall be the **Pedestrian Clearance** state. During State C, the phase shall activate its **Pedestrian Clearance** output and flash its **Dont Walk** output. The duration of the state shall be equal to the **Pedestrian Clearance** setting. The phase shall time the clearance and, upon completion of the timing, advance to State D.

d. State D shall be a **Green Dwell/Select** state from which the CU may select the next phases(s) to be serviced. During State D signal indications shall be **Green** and steady **Dont Walk.** When a serviceable conflicting call does not exist and the **Pedestrian Recycle** input is active, or when a serviceable conflicting call does not exist and the **Walk Rest Modifier** is active, the phase shall return to State A and retime the **Walk** interval. If the **Pedestrian Recycle** input is not active and the **Walk Rest Modifier** is not active, the pedestrian movement shall not recycle.

In the presence of external signals which may be used for coordination, the sequence of these states shall be as follows.

The **Green** interval begins with the existence of State A. Upon the completion of this state the CU exits to State B. If the **Hold** input is active at this point, the CU shall remain in this state. If **Force-off** is applied and if a serviceable conflicting call exists, the CU shall advance to State C; otherwise State B exists as long as **Hold** remains active. If **Hold** is released while the CU is in State B, the CU shall advance to State C without regard to the presence of a serviceable conflicting call. If the CU advances to State C, it shall advance to State D even in the presence of **Hold.** When in State D, the CU shall terminate the phase if a serviceable conflicting call exists. If no serviceable conflicting call exists, the CU returns to State A of this interval if **Pedestrian Recycle** is active. If **Pedestrian Recycle** is not active and no serviceable conflicting call exists, the CU rests in State D. The **Hold** function has no effect on the duration of State D.

The duration of the **Green** interval shall not be less than the setting of the **Minimum Green** control. In those instances where the sum of the **Walk** setting, the **Hold** state duration, and the **Pedestrian Clearance** setting is less than the setting on the **Minimum Green** control, the CU shall remain in State C until the phase has displayed a **Green** indication for a time equal to the **Minimum Green** time setting, and shall display a steady **Dont Walk.** Refer to Figure 3.5-6.



Note: MINIMUM GREEN time out during state A, B, or C. State D shall not be entered until MINIMUM GREEN is timed out.

Figure 3.5-6
ACTIVATED PHASE OPERATING IN THE NONACTIVATED MODE

4. Termination of **Green** Timing—**Green** timing termination shall occur in response to one of the following conditions:
   a. **Interval Advance** when timing the last portion of the **Green** interval, as described in 3.5.5.5(6).
   b. **Interval Advance** with **Manual Control Enable** activated as described in 3.5.5.5(7).
   c. Initial including variable portion completed, the pedestrian service completed, a serviceable conflicting call, and one of the following:

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(1) **Passage Time** timed out without **Hold** applied.
(2) Reduced gap timed out without **Hold** applied.
(3) **Maximum Green** termination without **Hold** applied.
(4) **Force-Off** applied.

d. Initial including the variable portion completed, the pedestrian service completed, **Red Rest** activated and **Passage Time** time out without **Hold** applied.

5. Vehicle Change and Clearance Intervals
   a. Following the **Green** interval of each phase the CU shall provide a **Yellow Change** interval which is timed according to the **Yellow Change** timing control for that phase.
   b. Following the **Yellow Change** interval for each phase, the CU shall provide a **Red Clearance** interval which is timed according to the **Red Clearance** timing control for that phase. During this **Red Clearance** interval, no Green indication shall be shown to any conflicting phase. This **Red Clearance** interval is subject to omission in response to operation of the per ring **Omit Red Clearance** input.
6. Pedestrian Timing, Exclusive—Exclusive pedestrian service shall be permitted. When servicing a pedestrian movement exclusively, no other phase shall be active. It shall not be required in a dual ring CU to provide more than two phases in the second timing ring when Exclusive Pedestrian timing is employed in the other timing ring, neither of which can be employed on the same side of the barrier with the Exclusive Pedestrian phase.

It shall not be required in a four-phase sequential CU to provide more than three phases in addition to an Exclusive Pedestrian phase.

Two time settings shall be required on the phase, **Walk** and **Pedestrian Clearance**, as described in 3.5.3.2(3).

When a pedestrian call is stored in pedestrian memory, the Exclusive Pedestrian phase shall be serviced with appropriate consideration of its order in the priority of phase sequencing.

The Exclusive Pedestrian phase shall rest with a steady **Dont Walk** indication displayed. It shall be possible to recycle the pedestrian indication in response to succeeding pedestrian calls for service, subject to absence of serviceable conflicting calls (vehicle or pedestrian) and nonactivation of the **Pedestrian Omit line.**

3.5.3.3 PHASE SELECTION POINTS

The phase next to be serviced shall be determined at the end of the **Green** interval of the terminating phase; except that if the decision cannot be made at the end of the **Green** interval, it shall not be made until after the end of all vehicle change and clearance intervals.

3.5.3.4 PROVISION FOR STORING A DEMAND

There shall be a provision for storing a call for vehicle service on each vehicle phase when that phase is not displaying a **Green** indication. The vehicle memory feature shall be capable of being disabled via program entry. There shall be a provision for storing a call for pedestrian service on phases equipped with pedestrian time setting, when that phase is not displaying a **Walk** indication.

3.5.3.5 PLACEMENT OF MAXIMUM RECALL

Means shall be provided to place a call on a phase, via program entry, such that the timing of the **Green** interval for that phase shall be extended to **Maximum Green** time.

When such a call is placed, the maximum timing shall commence to time as if there were always a serviceable conflicting call, but the phase shall not terminate unless there is an actual serviceable conflicting call.

3.5.3.6 PLACEMENT OF MINIMUM RECALL

Means shall be provided, via program entry, to place a recurring demand for vehicle service on the phase when that phase is not in its **Green** interval.

3.5.3.7 PLACEMENT OF PEDESTRIAN RECALL

Means shall be provided to place a recurring pedestrian demand, via program entry, which shall function in the same manner as an external pedestrian call except that it shall not recycle the pedestrian service until a conflicting phase is serviced.

3.5.3.8 PLACEMENT OF CALL AT PHASE TERMINATION

When a phase is terminated with time remaining in the **Passage Time**, a call shall be left on that phase. Disabling the vehicle call memory shall defeat this feature. If a phase is terminated with no passage time remaining, no call shall be left on the phase.

3.5.3.9 CONDITIONAL SERVICE

Conditional service shall provide an optional method for phase selection. When timing phases concurrently with the next serviceable call on a phase that conflicts with more than one of the phases timing (about to cross a barrier), if one of the phases is prepared to terminate due to gap out or max time out, the ring containing the timed out phase shall revert to a preceding vehicle phase if all of the following conditions apply:

1. A call exists on a preceding actuated vehicle phase. (Non-Actuated Phases shall not be conditionally re-serviced).

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2. The gapped/maxed phase is enabled for conditional service via program entry.
3. There is sufficient time remaining before max time out of the phase(s) not prepared to terminate.
4. The CU is not in coordinated mode.

3.5.3.10 AUTOMATIC PEDESTRIAN CLEARANCE

The CU design shall provide an alternate mode of operation to enable the CU timing of the Pedestrian Clearance interval when **Manual Control Enable** is active.

When enabled, via program entry, this feature shall prevent the Pedestrian Clearance interval from being terminated by the Interval Advance input.

3.5.3.11 INPUTS

1. **Hold** (In the applicable mode)—Command that retains the existing **Green** indications and has different CU responses depending upon operation in the vehicle-actuated or nonactuated mode. The operation is as follows:
   a. For a nonactuated phase, energization of the **Hold** input shall maintain the CU in the timed-out **Walk** period with a **Green** and **Walk** indication displayed. Energization of the **Hold** input while timing the **Walk** portion shall not inhibit the timing of this period. De-energization of the **Hold** input and with the **Walk** interval timed out shall cause the CU to advance into the **Pedestrian Clearance** interval. (See 3.5.3.2(3).) Reapplication of the **Hold** input while timing the **Pedestrian Clearance** portion shall neither inhibit the timing of this period nor termination of the phase.
   b. For an actuated phase, energization and de-energization of the **Hold** input shall be as follows.

      Energization of the **Hold** input shall allow the CU to time normally but shall inhibit its advance into the vehicle change interval. Energization of the **Hold** input shall inhibit the recycle of the pedestrian service unless the **Pedestrian Recycle** input is active and a serviceable pedestrian call exists on the phase. The rest state indications for that phase shall be **Green** for traffic and **Dont Walk** for pedestrians.

      De-energization of **Hold** input shall allow the CU to advance into the **Green Dwell/Select** state when all **Green** periods are timed out.

      De-energization of **Hold** input with all intervals timed out, shall allow the CU to recycle the **Walk** interval if there is no conflicting demand for service and a pedestrian call exists for that phase. However, if there is any serviceable demand on a conflicting phase with the **Hold** de-energized and with all intervals timed-out, the CU shall advance into the **Yellow Change** interval and not recycle the **Walk** on that phase until those demands have been served.
2. **Phase Omit** (In the applicable mode)—Input to cause omission of a phase, even in presence of demand, by application of an external signal. It shall affect phase selection. The omission shall continue in effect until the signal is removed. The phase to be omitted shall not present a conflicting call to any other phase, but shall accept and store calls. Activation of this input shall not affect a phase in the process of timing.
3. **Pedestrian Omit** (In the applicable mode)—Input to inhibit the selection of a phase due to a pedestrian call on that phase and to prohibit the servicing of a pedestrian call on the phase. This input when active shall prevent the starting of the pedestrian movement of that phase. After the beginning of the phase **Green**, a pedestrian call shall be serviced or recycled only in the absence of a serviceable conflicting call and with **Pedestrian Omit** on the phase nonactive. Activation of this input shall not affect a pedestrian movement in the process of timing.

3.5.3.12 Outputs

1. **Load Switch Drivers, Basic Vehicle** (Three Per Phase)—Provision for separate **Green, Yellow**, and **Red** outputs for each basic vehicle phase. A circuit closure to **Logic Ground** shall be maintained at one of these three outputs at all times. The three outputs shall energize the appropriate vehicle signal load switching circuit to result in a **Green, Yellow,** or **Red** indication for the required duration of such indication.
2. **Load Switch Drivers, Pedestrian** (Three Per Phase)—Provision of separate **Walk, Pedestrian Clearance**, and **Dont Walk** outputs for each pedestrian movement. A circuit closure to **Logic Ground** shall be maintained on at least one of these three outputs at all times. The three outputs shall energize the appropriate pedestrian signal load switching circuit to result in a **Walk, Pedestrian Clearance**, or **Dont Walk** indication. The **Dont Walk** output shall flash only during the **Pedestrian Clearance** interval as shown in Figure 3.5-7.

   The **Dont Walk** flashing shall provide an alternating **True/False** output at 1 pulse per second repetition rate with 50 + 2 percent duty cycle.
3. **Check** (In the applicable mode)—An output to indicate call status (vehicle or pedestrian, or both) of the phase, activated when the CU is not in the **Green** interval of that phase, which has a demand in that phase. Neither the **Phase Omit** nor **Pedestrian Omit** inputs shall affect the **Check** output.

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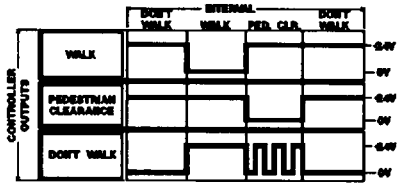

Figure 3.5-7
LOAD SWITCH DRIVERS, PEDESTRIANS

4. **Phase On** (In the applicable mode)—An output to indicate phase status. The **Phase On** output of a particular phase is activated during the **Green, Yellow**, and **Red Clearance** intervals of that phase. It shall be permissible for this output to be active during the **Red Dwell** state.
5. **Phase Next** (In the applicable mode)—An output of a particular phase activated when the phase is committed to be next in sequence and remains present until the phase becomes active. The phase next to be serviced shall be determined at the end of the **Green** interval of the terminating phase; except that if the decision cannot be made at the end of the **Green** interval, it shall not be made until after the end of all **Vehicle Change** and **Clearance** intervals.

3.5.4 Per Ring

The following inputs, outputs, functions, and programming controls shall be provided on a ring basis:

3.5.4.1 INPUTS

1. **Force Off**—Provision for termination of the **Green** timing in the actuated mode or **Walk Hold** in the nonactuated mode of the active phase in the timing ring by application of this signal, such terminating subject to presence of a serviceable conflicting call. The **Force Off** function shall not be effective during the timing of the **Initial, Walk**, or **Pedestrian Clearance**. The **Force Off** input shall be effective only as long as the input is sustained. (See 3.5.3.8.)
2. **Red Rest**—Input to require rest in **Red** of all phases in the timing ring by continuous application of an external signal. Registration of a serviceable conflicting call shall result in immediate advance from **Red Rest** to **Green** of the demanding phase. Registration of a serviceable conflicting call before entry into the **Red Rest** state, even with this signal applied, shall result in termination of the active phase and selection of the next phase in the normal manner and with appropriate change and clearance intervals. (See 3.5.5.7.)
3. **Inhibit Maximum Termination**—An input to disable the maximum termination functions of all phases in the selected timing ring. The input shall not inhibit the timing of **Maximum Green.**
4. **Omit Red Clearance**—An input to cause omission of **Red Clearance** interval timing(s).
5. **Pedestrian Recycle**—An input to control the recycling of the pedestrian movement. The recycling operation is dependent upon whether the phase is operating in the actuated or nonactuated mode:
   a. When the phase is operating in the actuated mode, if a serviceable pedestrian call exists on the phase and the **Hold** input is active, the pedestrian movement shall be recycled when the **Pedestrian Recycle** input is active, regardless of whether a serviceable conflicting call exists.
   b. When the phase is operating in the nonactuated mode, if the phase has reached State D (See 3.5.3.2(3)), the **Pedestrian Omit** is not active on the phase and a serviceable conflicting call does not exist, the pedestrian movement shall be recycled when the **Pedestrian Recycle** input is active.
6. **Stop Timing**—An input which when activated causes cessation of CU ring timing for the duration of such activation. Upon removal of activation from this input, all portions which were timing will resume timing. During stop timing, vehicle actuations on non-**Green** phases shall be recognized; vehicle actuations on **Green** phase(s) shall reset the **Passage Time** timer in the normal manner; and the CU shall not terminate any interval or interval portion or select another phase, except by activation of the **Interval Advance** input. Operation of the **Interval Advance** with **Stop Time** activated shall clear any stored calls on a phase when the CU is advanced through the **Green** interval of that phase.
7. **Maximum II Selection**—Input to allow the selection of a second maximum time setting on all phases of the timing ring.

3.5.4.2 OUTPUTS

One or more of the coded status bit states shown in Table 3.5-1 might be omitted from a normal cycle of operation. (Authorized Engineering Information). Only one of the coded status codes shall be active when the following conditions are present in the CU:

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Table 3.5-1
CODED STATUS BITS (3 PER RING)

Code #	Bit States A	B	C	State Names
0	OFF	OFF	OFF	Min Green
1	ON	OFF	OFF	Extension
2	OFF	ON	OFF	Maximum
3	ON	ON	OFF	Green Rest
4	OFF	OFF	ON	Yellow
5	ON	OFF	ON	Red Clear
6	OFF	ON	ON	Red Rest
7	ON	ON	ON	Undefined

Voltage Levels: OFF = +24V; ON = 0V

1. The active phase is in its **Green** interval and operating in the actuated mode.

Code 0 **Minimum Timing**—When timing in **Initial Walk**, or **Pedestrian Clearance** portions of the **Green** interval.

Code 1 **Extension Timing**—That portion of the **Green** interval following the completion of the minimum timings (**Initial, Walk**, and **Pedestrian Clearance**) when timing an extension(s).

Code 2 **Maximum Timing**—That portion of the **Green** interval following the completion of the minimum timings, (**Initial, Walk,** and **Pedestrian Clearance**) when not timing an extension and the **Maximum Green** is timing (e.g., when the **Hold** input is active).

Code 3 **Green Rest**—That portion of the **Green** interval when the minimum timings (**Initial, Walk**, and **Pedestrian Clearance**) are complete, **Passage Timer** is timed out and the **Maximum Green** timer is either timed out or has not started.

2. The active phase is in its **Green** interval and operating in the nonactuated mode.

Code 0 **Walk Timing**—When timing the **Walk** portion of the **Green** interval (nonactuated State A).

Code 1 **Walk Hold**—When the **Walk** output is active, **Walk** timing is complete and the **Hold** input is active (nonactuated State B).

Code 2 **Pedestrian Clearance Timing**—When timing the **Pedestrian Clearance** interval or the remaining portion of **Minimum Green** (nonactuated State C).

Code 3 **Green Rest**—When the timing of **Pedestrian** and **Minimum Green** intervals are complete (nonactuated State D).

3. The active phase is not in its **Green** interval.

Code 4 **Yellow Change**—When timing **Yellow Change.**

Code 5 **Red Clearance**—When timing **Red Clearance.**

Code 6 **Red Rest—When timing is complete and a Red** indication is displayed.

Code 7 Undefined

3.5.5 Per Unit

The following inputs, outputs, functions, and programming controls shall be provided on a per unit basis:

3.5.5.1 INITIALIZATION

Initialization shall occur under either of the following conditions:

1. Restoration of power after a defined power interruption.
2. Activation of **External Start** input.

A program entry for initialization shall be provided to cause the CU to start at the beginning of the **Green, Yellow**, or **Red** interval of any phase or nonconflicting phase pair.

As part of the initialization routine, vehicle and pedestrian calls shall be placed on all phases and retained until serviced.

3.5.5.2 SIMULTANEOUS GAP OUT

Multi-Ring CU configurations shall provide the capability of Simultaneous Gap Out when servicing cross barrier calls.

When timing phases concurrently with the next serviceable call on a phase that conflicts with more than one of the phases timing (about to cross a barrier), Simultaneous Gap Out, if enabled via program entry, shall insure that all phases which will terminate, must simultaneously reach a point of being committed to terminate before **Green** timing termination shall begin (i.e., Gap-Out, Max-Out, or Force-Off). When all phases have not yet reached such a point, any gapped out phase shall revert to the extensible portion and time passage intervals based on vehicle calls.

Under the conditions as defined above, Simultaneous Gap Out, if disabled, shall allow a phase to reach a point of being committed to terminate independently of any other phase and shall not revert to the extensible portion from a gapped out condition.

3.5.5.3 DUAL ENTRY

Dual Entry is a mode of operation (in multi-ring CUs) in which one phase in each ring must be in service, where possible subject to compatibility, at all times.

If a call does not exist in a ring when the CU is committed to cross a barrier, a phase may be selected, via program entry, in that ring to be active.

3.5.5.4 ALTERNATE SEQUENCES

The CU shall provide the capability of fifteen alternates to the standard sequence. The alternates shall be variations to the sequence based on four groups of two phases (Phase Pair) being serviced in reverse order.

As a minimum, the sixteen sequences shall provide every combination of lead-lag (phase pair reversal) for an eight phase dual ring CU configuration. For the purpose

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of this minimum requirement, the Alternate Sequences (AS) shall be capable of:

1. AS A—Phase 1 and Phase 2 Reversed
2. AS B—Phase 3 and Phase 4 Reversed
3. AS C—Phase 5 and Phase 6 Reversed
4. AS D—Phase 7 and Phase 8 Reversed

The alternate sequences may be selected by the Alternate Sequence external interface inputs (in the applicable mode) or the coordinator as a function of the pattern (Timing Plan/Offset) in effect. When the internal coordinator is running, the external interface inputs for alternate sequences shall be ignored.

Alternate Sequence inputs shall be interpreted as command requests in accordance with Table 3.5-2.

Table 3.5-2
ALTERNATE SEQUENCE

Command Request	AS A Input	AS B Input	AS C Input	AS D Input
Seq 00	OFF	OFF	OFF	OFF
Seq 01	ON	OFF	OFF	OFF
Seq 02	OFF	ON	OFF	OFF
Seq 03	ON	ON	OFF	OFF
Seq 04	OFF	OFF	ON	OFF
Seq 05	ON	OFF	ON	OFF
Seq 06	OFF	ON	ON	OFF
Seq 07	ON	ON	ON	OFF
Seq 08	OFF	OFF	OFF	ON
Seq 09	ON	OFF	OFF	ON
Seq 10	OFF	ON	OFF	ON
Seq 11	ON	ON	OFF	ON
Seq 12	OFF	OFF	ON	ON
Seq 13	ON	OFF	ON	ON
Seq 14	OFF	ON	ON	ON
Seq 15	ON	ON	ON	ON

Voltage Levels: OFF = +24V; ON = 0V

Connector Pins—In the applicable mode, input pin terminations shall be provided in accordance with the following:

1. Alternate Sequence A
2. Alternate Sequence B
3. Alternate Sequence C
4. Alternate Sequence D

3.5.5.5 INPUTS

1. **AC Line**—Current protected side of 120 VAC 60 Hertz power source within the CU.

   The CU shall have a front panel mounted over-current protection device in the 120 VAC input to the unit.
2. **AC Neutral**—Unfused and unswitched side of 120 VAC 60 Hertz power source taken from neutral output of ac power source.

   This input must not be connected to **Logic Ground** or **Earth Ground** within the CU.
3. **Earth Ground**—Terminal for connection to the chassis of the unit. **Earth Ground** shall be electrically connected to the shell of the connector(s) where applicable. This input shall not be connected to **Logic Ground** or AC **Neutral** within the CU.
4. **Vehicle Detector**—Provision to enter a vehicle call into the CU.

Vehicle Detector inputs shall be provided as follows:

(a) Type A1 CU - 32

(b) Type A2 CU - 8 (20 in the applicable mode—See 3.5.5.5(15))

As a minimum, each Vehicle Detector input shall be enabled by assignment to any one phase, via program entry. Each shall be capable of Delay, Extension, and Switching as follows:

a. Delay—The vehicle detector actuation (input recognition) shall be capable of being delayed, by an adjustable program entered time (0–255 seconds in increments of 1 second), when the phase is not **Green**. Once the actuation has been present for the delay time it shall be continued for as long as it is present. If an actuation is removed prior to delay timing out, no call is placed.

b. Extension—The vehicle detector actuation (input duration) shall be capable of being extended from the point of termination by an adjustable program entered time (0–25.5 seconds in increments of 0.1 second), when the phase is **Green.**

c. Switch—The vehicle detector actuation shall be capable of being switched to another phase when the assigned phase is **Yellow** or **Red** and the program entered phase is **Green**. Detector Switching provides a per detector entry identifying the program entered phase that will receive the switched actuations.

The special vehicle detector functions shall be capable of being used in any combination.

As a minimum, eight Vehicle Detector inputs shall be capable of assignment to a System Detector function, via program entry.

5. **Pedestrian Detector Call** (8 per unit)—Provision to enter a pedestrian demand for service into the appropriate phase of the CU.

As a minimum, each Pedestrian Detector Call input shall be enabled by assignment to any one phase, via program entry.

6. **Interval Advance**—A complete **On-Off** operation of this input shall cause immediate termination of the interval in process of timing. Where concurrent interval timing exists, use of this input shall cause immediate termination of the interval which would terminate next without such actuation.

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Phases without stored vehicle or pedestrian calls shall be omitted from the resultant phase sequencing of the CU unless **External Min. Recall To All Vehicle Phases** or **Manual Control Enable** inputs are activated.

The CU shall select the next phase to service based on its normal sequence control method. If **Interval Advance** is activated during the **Green** interval and no serviceable call exists, the CU shall not advance beyond the **Green Dwell/Select** state, except when **Red Rest** is active.

If **Interval Advance** is applied when the CU is displaying **Green** and **Walk** indications, the unit shall advance to the state of displaying **Green** and **Pedestrian Clearance**. If **Interval Advance** is applied when the unit is displaying **Green** and **Pedestrian Clearance,** the unit shall display a steady **Dont Walk** indication and advance to the **Green Dwell/Select** state, from which it shall immediately select a phase next and advance to the **Yellow** subject to the presence of a serviceable conflicting call and the constraints of concurrent timing.

If no pedestrian provisions exist, application of the **Interval Advance** signal at any point in the **Green** interval shall cause the unit to advance to the **Green Dwell/Select** state from which it shall immediately select a phase next and advance to the **Yellow** subject to the presence of a serviceable conflicting call and the constraints of concurrent timing.

Interval Advance may be used in conjunction with **Manual Control Enable** to produce manual control of the CU with timed vehicle change and clearance intervals.

Interval Advance shall be used in conjunction with **Stop Time** to advance through all serviceable intervals except that the CU shall not advance beyond the **Green Dwell/Select** state without a serviceable conflicting call, except when **Red Rest** is active.

7. **Manual Control Enable**—An input to place vehicle and pedestrian calls on all phases, stop CU timing in all intervals except vehicle change and clearance intervals, and inhibit the operation of **Interval Advance** during vehicle change and clearance intervals. When this function is used in conjunction with **Interval Advance**, the operation of the CU shall be as follows:
   a. When concurrent pedestrian service is not provided, an activation of the **Interval Advance** shall advance the CU to **Green Dwell/Select,** from which it shall immediately select a phase next and advance to the **Yellow**, subject to the constraints of concurrent timing.
   b. When concurrent pedestrian service is provided, an activation of the **Interval Advance** input shall terminate the **Walk** interval. When **Automatic Pedestrian Clearance** is enabled, the **Pedestrian Clearance** interval is timed internally by the CU (see 3.5.3.10). When **Automatic Pedestrian Clearance** is not enabled, a second activation of the **Interval Advance** input is required to terminate the **Green** interval, including the **Pedestrian Clearance** interval.
   c. All vehicle change and clearance intervals are timed internally by the CU. Actuations of the **Interval Advance** input during vehicle change and clearance intervals shall have no effect on the CU.
8. **Call To Nonactuated Mode** (Two per Unit)—Two inputs shall be provided which when activated shall cause any phases(s) appropriately programmed to operate in the **Nonactuated Mode.**

The two inputs shall be designated **Call To Nonactuated Mode I** and **Call To Nonactuated Mode II.** When both inputs are active, all phases programmed for **Nonactuated Mode** shall operate in the **Nonactuated Mode** as described in 3.5.3.2(3).

Only phases equipped for pedestrian service shall be used for **Nonactuated Mode** operation.

9. **External Minimum Recall To All Vehicle Phases**—Input to place a recurring demand on all vehicle phases for a minimum vehicle service.
10. **Indicator Lamp Control**—Input to disable CU indicators.

The CU might not employ this input. (Authorized Engineering Information)

11. **Test Input** (Two or three per Unit)—Test input, two or three per CU, for manufacturer's use only.
12. **External Start**—An input to cause the CU to revert to its programmed initialization phase(s) and interval(s) upon application. Upon removal of this input the CU shall commence normal timing.
13. **Walk Rest Modifier**—This input when true shall modify nonactuated operation only. With this input active, nonactuated phase(s) shall remain in the timed-out **Walk** state (rest in **Walk**) in the absence of a serviceable conflicting call without regard to the **Hold** input status. With this input nonactive, nonactuated phase(s) shall not remain in the timed-out **Walk** state unless the **Hold** input is active.

    The CU shall recycle the pedestrian movement when reaching State D in the absence of a serviceable conflicting call. See 3.5.3.2(3d).
14. **System Address Bits**—Five System Address inputs shall be provided. The CU shall respond to the system address defined by the binary decoding of these five inputs.
15. **Input/Output Mode** (Three per Unit)—The Type A2 CU shall select the input/output function of specific hardware I/O based on the current status of these three inputs.

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I/O Mode Bits (3 per Unit)

Mode #	Bit States A	B	C	State Names
0	OFF	OFF	OFF	TS 1 Compatible
1	ON	OFF	OFF	Hardwire Interconnect
2	OFF	ON	OFF	System Interface
3	ON	ON	OFF	Reserved
4	OFF	OFF	ON	Reserved
5	ON	OFF	ON	Reserved
6	OFF	ON	ON	Manufacturer Specific
7	ON	ON	ON	Manufactured Specific

Voltage Levels: OFF = +24; ON = 0V

a. Mode 0 Input/Output Functions

Inputs:

Pin	Function
A-h	Phase 1 Hold
A-M	Phase 2 Hold
B-i	Phase 3 Hold
B-h	Phase 4 Hold
C-m	Phase 5 Hold
C-p	Phase 6 Hold
C-EE	Phase 7 Hold
C-X	Phase 8 Hold
B-U	Phase 1 Phase Omit
B-S	Phase 2 Phase Omit
B-R	Phase 3 Phase Omit
B-g	Phase 4 Phase Omit
C-n	Phase 5 Phase Omit
C-q	Phase 6 Phase Omit
C-r	Phase 7 Phase Omit
C-s	Phase 8 Phase Omit
A-EE	Phase 1 Ped Omit
A-v	Phase 2 Ped Omit
B-j	Phase 3 Ped Omit
B-x	Phase 4 Ped Omit
B-T	Phase 5 Ped Omit
B-k	Phase 6 Ped Omit
B-m	Phase 7 Ped Omit
B-n	Phase 8 Ped Omit

Outputs:

Pin	Function
A-DD	Phase 1 Phase On
A-e	Phase 2 Phase On
B-s	Phase 3 Phase On
B-e	Phase 4 Phase On
C-N	Phase 5 Phase On
C-CC	Phase 6 Phase On
C-NN	Phase 7 Phase On
C-GG	Phase 8 Phase On
B-A	Phase 1 Phase Next
B-C	Phase 2 Phase Next
B-t	Phase 3 Phase Next
B-f	Phase 4 Phase Next
C-M	Phase 5 Phase Next
C-DD	Phase 6 Phase Next
C-PP	Phase 7 Phase Next
C-HH	Phase 8 Phase Next
A-u	Phase 1 Check
A-d	Phase 2 Check
B-r	Phase 3 Check
B-K	Phase 4 Check
C-k	Phase 5 Check
C-BB	Phase 6 Check
C-MM	Phase 7 Check
C-FF	Phase 8 Check

b. Mode 1 Input/Output Functions

Inputs:

Pin	Function
A-h	Preempt 1
A-M	Preempt 3
B-i	Vehicle Detector 9
B-h	Vehicle Detector 10
C-m	Vehicle Detector 13
C-p	Vehicle Detector 14
C-EE	Vehicle Detector 15
C-X	Vehicle Detector 16
B-U	Vehicle Detector 11
B-S	Vehicle Detector 12
B-R	Timing Plan C
B-g	Timing Plan D
C-n	Alternate Sequence A
C-q	Alternate Sequence B
C-r	Alternate Sequence C
C-s	Alternate Sequence D
A-EE	Dimming Enable
A-v	Automatic Flash
B-j	Timing Plan A
B-x	Timing Plan B
B-T	Offset 1
B-k	Offset 2
B-m	Offset 3
B-n	TBC On Line

Outputs:

Pin	Function
A-DD	Preempt 1 Status
A-e	Preempt 3 Status
B-s	TBC Auxiliary 1
B-e	TBC Auxiliary 2

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Pin	Function
C-N	Timing Plan A
C-CC	Timing Plan B
C-NN	Offset 1
C-GG	Offset 2
B-A	Preempt 2 Status
B-C	Preempt 4 Status
B-t	Preempt 5 Status
B-f	Preempt 6 Status
C-M	Offset 3
C-DD	Timing Plan C
C-PP	Timing Plan D
C-HH	Reserved
A-u	Free/Coord Status
A-d	Automatic Flash
B-r	TBC Auxiliary 3
B-K	Reserved
C-k	Reserved
C-BB	Reserved
C-MM	Reserved
C-FF	Reserved

c. Mode 2 Input/Output Functions

Inputs:

Pin	Function
A-h	Preempt 1
A-M	Preempt 3
B-i	Vehicle Detector 9
B-h	Vehicle Detector 10
C-m	Vehicle Detector 13
C-p	Vehicle Detector 14
C-EE	Vehicle Detector 15
C-X	Vehicle Detector 16
B-U	Vehicle Detector 11
B-S	Vehicle Detector 12
B-R	Vehicle Detector 17
B-g	Vehicle Detector 18
C-n	Vehicle Detector 19
C-q	Vehicle Detector 20
C-r	Alarm 1
C-s	Alarm 2
A-EE	Dimming Enable
A-v	Local Flash Status
B-j	Address Bit 0
B-x	Address Bit 1
B-T	Address Bit 2
B-k	Address Bit 3
B-m	Address Bit 4
B-n	MMU Flash Status

Outputs:

Pin	Function
A-DD	Preempt 1 Status
A-e	Preempt 3 Status
B-s	TBC Auxiliary 1
B-e	TBC Auxiliary 2
C-N	Timing Plan A
C-CC	Timing Plan B
C-NN	Offset 1
C-GG	Offset 2
B-A	Preempt 2 Status
B-C	Preempt 4 Status
B-t	Preempt 5 Status
B-f	Preempt 6 Status
C-M	Offset 3
C-DD	Timing Plan C
C-PP	Timing Plan D
C-HH	Reserved
A-u	Free / Coord Status
A-d	Automatic Flash
B-r	TBC Auxiliary 3
B-K	Reserved
C-k	System Special Function 1
C-BB	System Special Function 2
C-MM	System Special Function 3
C-FF	System Special Function 4

d. Mode 3, 4, and 5 Input/Output Functions

Mode 3, 4, and 5 are reserved for future definition and use by NEMA. The CU shall not recognize any mode dependent input as valid nor shall it provide a valid output on any mode dependent output when this Input/Output Mode is active.

e. Mode 6 and 7 Input/Output Functions

Mode 6 and 7 are for manufacturer specific applications.

A Terminal and Facilities wired to utilize Mode 6 or Mode 7 may not be compatible with other manufacturer's CUs. (Authorized Engineering Information)

3.5.5.6 OUTPUTS

1. **Logic Ground**—Voltage reference point and current return for CU input and output logic circuits. This output must not be connected to AC **Neutral** or **Earth Ground** within the CU.
2. **Fault Monitor**—An open collector output which is maintained **True** (low state) as long as the voltages within the CU do not drop below predetermined levels required to provide normal operation.

   The output will also be **False** (hi state) during CU generated flash modes as defined elsewhere in this section.
3. **Controller Unit Voltage Monitor** (Type A2 Only) - An open collector output which is maintained **True**

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(low state) as long as the voltages within the CU do not drop below predetermined levels required to provide normal operation.

The output will also be **False** (hi state) during CU generated flash modes as defined elsewhere in this section.

This output operates concurrently with Fault Monitor output except during periods of No Fault Flash (i.e., Startup Flash, Automatic Flash, and Preempt Flash).

4. **Regulated 24 Volts DC For External Use** (Type A2 Only)—Positive 24 ± 2 volts DC shall be regulated over an AC line voltage variation from 89 to 135 volts from no-load to full-load. Current capability shall be 500 milliamperes continuous with less than 0.5 volt peak-to-peak ripple.
5. **Flashing Logic Output** (Type A2 Only)—Alternating **True/False** logic output at 1 pulse per second repetition rate with 50 ± 2 percent duty cycle. In its **False** state, this output shall be capable of providing 50 milliamperes of current. In its **True** state, this output shall be capable of sinking 200 milliamperes. This output shall switch within 5 degrees of the zero crossover point of the AC line.
6. **Load Switch Drivers, Vehicle Overlap** (Three per Overlap—Provision of separate **Green, Yellow,** and **Red** outputs for each overlap when determined internal to the CU, four overlaps maximum. A circuit closure to **Logic Ground** shall be maintained at one of these three outputs at all times. The three outputs shall energize the appropriate overlap signal load switching circuit to result in a **Green, Yellow,** or **Red** indication for the duration of such required indication.

3.5.5.7 RED REVERT

A provision within the CU whereby an adjustable (2–6 seconds)* minimum **Red** indication will be timed following the **Yellow Change** interval and prior to the next display of **Green** on the same phase.

* Not less than 2 seconds and in increments not greater than 1 second.

3.5.6 Priority of Input Functions

The priority of input functions shall be in the following order:

a. Power-Up
b. External Start
c. Preemption
d. Phase Omit
e. Pedestrian Omit
f. Interval Advance
g. Stop Time
h. Automatic Flash
i. Manual Control Enable
j. Ring Force Off
k. Phase Hold
l. Pedestrian Recycle

Lower priority inputs shall condition those of higher priority as defined elsewhere in this standard.

3.5.7 Indications

Indications shall be provided on the display and appropriately identified to facilitate the determination of the operation of the CU. These indications shall consist of the following as a minimum requirement:

The indications shall provide for the simultaneous (i.e., concurrent) presentation, where concurrent states exists, of the following states/functions:

Phase Information:

1. Phase or phases in service
2. Phase or phases next to be serviced
3. Presence of vehicle call
4. Presence of pedestrian call

The above information shall be displayed simultaneously for all phases.

Status of Active Phase in the Ring:

1. Initial
2. Extension
3. Yellow change
4. Red clearance
5. Walk
6. Pedestrian clearance
7. Reason for **Green** termination
   a. Gap-out
   b. Maximum time-out
   c. Force-off
8. Rest state (dwell).

The above information shall be presented simultaneously for two rings in a multi-ring CU.

3.5.8 Overlaps

All CUs shall include internally generated overlaps.

Overlaps are designated alphabetically A, B, C, and D. The generation of control for overlap signal indications shall be programmable and shall provide **Green, Yellow,** and **Red** load switch drivers for each of four overlap signals. Change and Clearance Timing—The timing for **Yellow Change** and **Red Clearance** overlap signals shall be determined by either:

a. The phase terminating the overlap, or
b. An independent adjustment for each overlap signal.

3.6 ACTUATED COORDINATION

The CU shall include provisions for an internal coordinator. The coordinator shall accept Timing Plan (Dial/Split) and Offset commands from traditional

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(pretimed) interconnect systems, from a companion Time Base program, and/or an Internal System Interface.

3.6.1 Definitions

These definitions define the nomenclature frequently used in this part of the Standard Publication.

3.6.1.1 PERMISSIVE

A time period, during which the CU is allowed to leave the coordinated phase(s) under coordination control to go to other phases.

3.6.2 Operation

Coordination shall be implemented by holding the CU in the programmed coordinated phase(s) until a specific point in the cycle, and forcing-off non-coordinated phase(s) at predetermined points within the cycle.

Coordination controls shall be internally applied (i.e., Hold, Omit, Force Ring 1, etc.) while the CU inputs for these same functions remain active and may impact coordinator operation.

Coordination shall be capable of implementing alternate sequence operations. It shall be possible to transfer from one sequence to another based on a change in pattern (Timing Plan plus Offset). When the internal coordinator is running, external selection of alternate sequences shall be ignored.

3.6.2.1 TIMING PLANS

The coordinator shall provide control for a minimum of 16 timing plans. The Coordinator shall select the timing plan to be used, according to the current status of the Timing Plan request.

3.6.2.1.1 Cycles

The coordinator shall be capable of providing a minimum of 1 cycle length for each timing plan. Each cycle shall be adjustable over a range of 30 to 255 seconds in 1-second increments.

3.6.2.1.2 Splits

A minimum of 1 set of splits shall be provided for each timing plan. Each split shall provide an adjustable time for each phase, each adjustable from 0 to 100 percent in 1-percent increments or from 0 to 255 seconds in 1-second increments.

3.6.2.2 OFFSET

Coordination shall include a minimum of three offsets per timing plan, each adjustable from 0 to 100 percent in 1 percent increments or from 0 to 254 seconds in 1 second increments.

The values shall determine the latest time that the starting point of the coordinated phase **Green**, local time zero, shall lag the Synchronization pulse, system time zero.

The Coordinator shall recognize when the sync reference and local offset in control indicate local zero is not correct. When establishing its offset based on the sync pulse, the coordinator shall reference only the leading edge, regardless of the width of the sync pulse. The pulse width shall be a minimum of 3 seconds or 3 percent of the cycle.

It shall be possible to enact Free Mode as a function of the Timing Plan plus Offset in effect. This shall be accomplished via program entry.

3.6.2.3 SYNC MONITOR

The coordinator shall monitor the Offset command requests for validity of the imposed sync reference.

The coordinator shall cause the CU to revert to Free mode when:

1. No sync pulse is received for three consecutive cycles
2. No offset line is active for 15 seconds
3. More than one offset line is active for 15 seconds

During Sync Monitor Free mode, the Offset command requests shall continue to be monitored and should the command request return to valid operation, the coordinator shall implement the pattern commanded.

The Sync Monitor Free mode may be replaced by a TBC event. See the **On-Line** definition in the Time Base section.

3.6.2.4 MANUAL CONTROL

The coordinator shall be capable of being set to manually operate in any pattern (Timing Plan plus Offset) via program entry. A manual selection of pattern overrides all other pattern interface commands.

3.6.2.5 FREE MODE

The coordinator shall be capable of Free mode of operation. During this mode all coordinator control of the CU operation shall be removed.

The coordinator shall be capable of being set to the Free mode defined under Sync Monitor and via program entry.

The coordinator shall recognize input requests that conflict with the internal coordination operation and automatically revert to Free mode while the inputs are active. The inputs that conflict with internal coordination are:

1. **Manual Control Enable**
2. Any **Stop Time**
3. **Automatic Flash**
4. Any **Preemption**

3.6.3 Command Priority

The coordination patterns are capable of being selected based on program entry, Interconnect Inputs, Time Base

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Control events, and a System Interface. The pattern select priority shall be as follows:

1. Program Entry
2. System Interface
3. Time Base Control Event
4. Interconnect Inputs

3.6.4 External Interface

The coordinator external interface for Type A1 CUs shall be via Port 1 (See 3.3.1). The external interface for Type A2 CUs shall be via Connectors A, B, and C (see 3.3.5).

The coordinator shall operate with an external interface as follows:

1. Coord Inputs: The Coordinator shall select the pattern to be used, according to the current status of the Timing Plan and Offset requests. In the applicable mode, seven inputs for a hardwire type interconnect interface shall be available.
2. Coord Outputs: Seven outputs for master type interconnect interface drivers shall be available. The coord outputs shall echo the active pattern. All outputs shall be constantly "**On**" when active except offset which is "**Off**" for a minimum of 3 seconds or 3 percent of the cycle once each cycle beginning at the "0" point of the cycle.
3. Levels: All logic signals shall be low state (nominal 0 volts dc) for the operate condition of all coord inputs and outputs.
4. Connector Pins: Input/Output pin terminations shall be provided in accordance with the following table:

Coordination Inputs	Coordination Outputs
Timing Plan A Input	Timing Plan A Output
Timing Plan B Input	Timing Plan B Output
Timing Plan C Input	Timing Plan C Output
Timing Plan D Input	Timing Plan D Output
Offset 1 Input	Offset 1 Output
Offset 2 Input	Offset 2 Output
Offset 3 Input	Offset 3 Output

5. Input/Output Command Association: Coord inputs and outputs shall be interpreted as command requests in accordance with Tables 3.6-1 and 3.6-2.

For the purpose of utilization in an existing traditional interconnect system, a Reference with Dial and Split numbers is provided.

3.6.5 Indications

Indications shall be provided on the display and appropriately identified to facilitate the determination of coord operation.

Coordinator settings and activity shall be capable of being monitored on the display (i.e., Hold, Omit, and Force Off indication shall denote when these functions are used).

Table 3.6-1
TIMING PLAN

Command	TP A	TP B	TP C	TP D	Reference,
TP 00	OFF	OFF	OFF	OFF	Dial 1 Split 1
TP 01	OFF	OFF	ON	OFF	Dial 1 Split 2
TP 02	OFF	OFF	OFF	ON	Dial 1 Split 3
TP 03	OFF	OFF	ON	ON	Dial 1 Split 4
TP 04	ON	OFF	OFF	OFF	Dial 2 Split 1
TP 05	ON	OFF	ON	OFF	Dial 2 Split 2
TP 06	ON	OFF	OFF	ON	Dial 2 Split 3
TP 07	ON	OFF	ON	ON	Dial 2 Split 4
TP 08	OFF	ON	OFF	OFF	Dial 3 Split 1
TP 09	OFF	ON	ON	OFF	Dial 3 Split 2
TP 10	OFF	ON	OFF	ON	Dial 3 Split 3
TP 11	OFF	ON	ON	ON	Dial 3 Split 4
TP 12	ON	ON	OFF	OFF	Dial 4 Split 1
TP 13	ON	ON	ON	OFF	Dial 4 Split 2
TP 14	ON	ON	OFF	ON	Dial 4 Split 3
TP 15	ON	ON	ON	ON	Dial 4 Split 4

Table 3.6-2
OFFSET

Command	Off 1	Off 2	Off 3
Offset 1	ON	OFF	OFF
Offset 2	OFF	ON	OFF
Offset 3	OFF	OFF	ON
Sync	OFF	OFF	OFF

Voltage Levels: OFF = +24V; ON = 0

As a minimum, the indications shall provide the following:

Current Status

1. Running Pattern, Control Source
2. Running Pattern, Timing Plan plus Offset
3. Correction In Progress
4. System Zero
5. Cycle Counter

3.7 PREEMPTION

The CU shall include provisions for an internal preemptor with the capability of 6 unique preempt sequences.

3.7.1 Definitions

These definitions define the nomenclature frequently used in this part of the Standard Publication.

3.7.2 Operation

Internal Preemption shall be a special program operating within the CU. The preemption program shall accept com-

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mands from 6 preempt inputs and provide the timing and signal display programmed to occur in response to each.

Preemption controls shall be internally applied. Internally applied preempt controls shall have priority as defined in Section 3.5.6.

The preemption program shall recognize the current signal display at the time of preempt and shall provide transition timing and signal display to a programmed preempt condition. Once the preempt has been satisfied, the preemption program shall provide an exit transition timing and signal display to a programmed (one for each of the six preempt inputs) return-to-normal condition.

3.7.2.1 INPUT PRIORITY

The Preemption program shall provide for setting priorities of the preemption inputs with respect one to the other and to other inputs. The priorities shall be as follows:

1. Preempt 1 shall normally have priority over Preempt 2. If Preempt 1 becomes active while the Preemption program is in the Preempt 2 routine, the CU shall immediately terminate the Preempt 2 routine and enter the Preempt 1 routine. When Preempt 2 has been terminated by Preempt 1, control shall not return to Preempt 2 at the end of Preempt 1 except when Preempt 2 demand is still present at the end of Preempt 1.

   The priority of Preempt 1 over Preempt 2 shall be capable of being canceled via program entry. If the priority has been canceled and the Preempt 1 becomes active while the preemption program is in the Preempt 2 routine, the Preempt 2 routine shall complete normally. After Preempt 2 is complete, the CU shall enter the Preempt 1 routine only if the Preempt 1 demand is still present.

   When Preempt 2 becomes active while the preemption program is in the Preempt 1 routine, the Preempt 1 routine shall complete normally regardless of the priority of Preempt 1 versus Preempt 2. After Preempt 1 is complete, the CU shall enter the Preempt 2 routine only if the Preempt 2 demand is still present. Whenever both inputs become active at the same time, Preempt 1 shall occur first.

   Preempt 2 shall normally have priority over Preempt 3. The priority of Preempt 2 over Preempt 3 shall be capable of being cancelled via program entry.

   Preempt 3, 4, 5, and 6 shall normally have equal status (priority canceled). A priority of Preempt 3 over Preempt 4, Preempt 4 over Preempt 5, and Preempt 5 over Preempt 6 shall be capable of being established via program entry.

   Operation capability as described above for Preempt 1 and 2 shall be provided for Preempt 2 and 3, 3 and 4, 4 and 5, and 5 and 6.

   The default priorities above were established assuming PE1 and PE2 as railroad and PE3 to PE6 as emergency vehicle (Authorized Engineering Information).
2. All Preempt routines shall normally have priority over Automatic Flash. If any Preempt becomes active while the CU is in Automatic Flash, Automatic Flash shall terminate normally and the CU shall enter the Preempt routine.

   The priority of Preempt over Automatic Flash shall be capable of being canceled via program entry. If the priority of Preempt over Automatic Flash has been canceled and a Preempt input becomes active while the CU is in Automatic Flash, the CU shall remain in Automatic Flash until the demand (Both Automatic Flash and Preempt) is terminated.
3. Start-Up Flash shall always have priority over all Preempt routines. If a Preempt input becomes active or is active during Start-Up Flash, the CU shall maintain the Start-Up Flash condition for the duration of the both Preempt demand and Start-Up Flash time.
4. External Start shall always have priority over all Preempt routines. If External Start becomes active during a Preempt routine, the CU shall revert to Start-Up Flash rather than the Initialization condition. The CU shall maintain the Start-Up Flash condition for the duration of the External Start, Preempt demand, and Start-Up Flash time.

3.7.2.2 MEMORY

The premption program shall provide input memory which shall be capable of being set to locking or non-locking via program entry.

When input memory is set for non-locking, termination of the input prior to implementation of the routine shall not initiate preempt operation.

3.7.3 External Interface

The preemptor external interface for Type A1 and P1 CUs shall be via Port 1 (see 3.3.1). The external interface for Type A2 and P2 CUs shall be via Connectors A, B, and C (see 3.3.5).

The preemptor shall operate with an external interface as follows:

1. Preempt Inputs: The Preemptor shall select the preempt routine to be active, according to the current status of the inputs and the preempt priority entries. In the applicable mode, six inputs for preempt actuation shall be available.
2. Preempt Outputs: Six outputs, one for each preempt routine shall be available. The outputs shall be "on" when their respective preempt is in control.
3. Input Levels: All logic signals shall be low state (nominal 0 volts DC) for the operate condition of all preempt inputs.

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4. Connector Pins: Input pin terminations shall be provided in accordance with the following table:

Preemption Inputs	Preemption Outputs
Preempt 1 Input	Preempt 1 Output
Preempt 2 Input	Preempt 2 Output
Preempt 3 Input	Preempt 3 Output
Preempt 4 Input	Preempt 4 Output
Preempt 5 Input	Preempt 5 Output
Preempt 6 Input	Preempt 6 Output

3.7.4 Indications

Indications shall be provided on the display and appropriately identified to facilitate the determination of preempt operation.

As a minimum, the indications shall provide the following:

Current Status

1. Preempt Call
2. Preempt In Control
3. Preempt Interval
4. Preempt Interval Counter

3.8 TIME BASE

The CU shall include provisions for internal Time Base Control.

3.8.1 Definitions

These definitions define the nomenclature frequently used in this part of the Standard Publication.

3.8.1.1 COORDINATED UNIVERSAL TIME

The National Institute of Standards and Technology operates standard frequency and time stations at Fort Collins, Colorado. The broadcasts of WWV may be heard via telephone by dialing (303) 499-7111, Boulder, Colorado. (Not a toll-free number).

3.8.2 Operation

The internal Time Base Control shall be a special program operating within the CU. A minimum of 48 different Time Base Control events shall be capable of being programmed over a one year time frame.

The Time Base calendar shall provide automatic compensation for leap years.

The Time Base Control shall provide for Daylight Savings Time to be programmed to occur automatically as defined by law in most states or not to occur.

The Time Base clock shall be maintained to within ± 0.005 % at 20°C (68°F) and to within ± 0.02% over the specified operating temperature range as compared to Coordinated Universal Time (WWV) standard for a period of thirty days during periods when AC power is not applied.

The Time Base Control program shall output Timing Plan plus Offset commands to the coordination program. It shall be possible to perform functions not necessarily traffic related within the Time Base Control program by programming and use of three auxiliary outputs.

The Time Base coordination pattern sync (Cycle Zero) shall be user programmable to be referenced to any hour/minute or the event time.

3.8.3 External Interface

The Time Base Control external interface for Type A1 and P1 CUs shall be via Port 1 (see 3.3.1). The external interface for Type A2 and P2 CUs shall be via Connectors A, B, and C (see 3.3.5).

The Time Base Control shall operate with an external interface as follows:

1. Time Base Inputs: One input for Time Base control shall be available. The Time Base On Line input, when active, shall disable the Time Base pattern outputs to the internal coordination program.
2. Time Base Outputs: Three outputs for Time Base Auxillary shall be available. The outputs shall be "on" when their respective auxillary is part of the current time base event.
3. Output Levels: All logic signals shall be low state (nominal 0 volts DC) for the operate condition.
4. Connector Pins: Input/Output pin terminations shall be provided in accordance with the following table:

Time Base Inputs	Time Base Outputs
On Line	Aux # 1 Output
	Aux # 2 Output
	Aux # 3 Output

3.8.4 Indications

Indications shall be provided on the display and appropriately identified to facilitate the determination of time base operation.

As a minimum, the indications shall provide the following:

Current Status

1. Date, Time, Day-Of-Week
2. Current Event Pattern
3. Current Event Auxillary Functions

3.9 MISCELLANEOUS

3.9.1 Flash

3.9.1.1 START-UP FLASH

The CU shall have provisions whereby an adjustable time period/state (Start-Up Flash—0 to 255 seconds in

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increments of 1 second) shall occur prior to the Initialization routine.

During the Start-Up Flash state, the **Fault Monitor** and **Voltage Monitor** outputs shall be inactive.

When power is restored following a defined power interruption, the Start-Up Flash state shall become operational. No input, other than the lack of AC power, shall prevent this state from the completion and/or exit to the Initialization routine except as noted in this standard.

If a Preempt Input is active during Start-Up Flash timing, the CU shall maintain the Start-Up Flash state for the duration of the Preempt demand and/or Start-Up Flash time.

3.9.1.2 AUTOMATIC FLASH

The activation of this input shall cause the following operation to occur:

1. Actuated CUs

   The CU shall assure the completion of the **Minimum Green** or **Walk** plus **PED Clearance** time on the current phase(s). Thereafter, if necessary, it shall proceed to the vehicle clearance intervals followed by the programmed Entry Phase(s). After the Entry Phase(s) **Minimum Green** or **Walk** plus **PED Clearance**, the CU shall proceed to the vehicle clearance intervals. Upon completion of the vehicle **Red Clearance** interval, the CU shall initiate flashing operation. The CU shall maintain this condition as long as the Automatic Flash input is active.

   When the input becomes inactive, the CU shall move immediately to the beginning of the phase(s) programmed as the Exit Phase(s), with a Green/Walk display, calls on all phase vehicle and pedestrian, and shall cease flashing operation.

2. Pretimed CUs

   The CU shall cycle normally to the programmed Entry Interval. Upon completion of the interval, the CU shall initiate flashing operation. The CU shall maintain this condition as long as the Automatic Flash input is active.

   When the input becomes inactive, the CU shall move immediately to the beginning of the programmed Exit Interval, with calls on all actuated vehicle and pedestrian movements, and shall cease flashing operation.

3. Method

   The method by which flashing operation is accomplished shall be determined via program entry and shall be either:

   a. **Voltage Monitor** Output inactive, or

   b. Load Switch Driver Output Flashing

   Load Switch Driver Output Flashing shall provide an alternating **True/False** logic output at 1 pulse per second repetition rate with 50 ± 2 percent duty cycle. The selection, via program entry, of Yellow flashing, Red flashing, or Dark for each vehicle load switch driver group (G/Y/R) shall be provided. All pedestrian load switch driver groups (W/PC/D) shall be inactive (DARK) in flash.

3.9.2 Dimming

The CU shall be programmed to provide output dimming based on a Time Base Auxiliary Event and Dimming Enable input (both must be active to enable). The dimming function shall be accomplished by controlling the load switch driver outputs with respect to the AC line voltage.

For a Type A1 and P1 CU, the dimming function shall be accomplished within the TF.

For a Type A2 and P2 CU, the dimming function shall be integral to the CU.

The dimming function shall be accomplished by the elimination of alternate one-half wave segments from the AC sinusoid applied to the field indications. When "**Dimmed**" by this method, the control transition from the **On** (low state) to **Off** (high state) and vice versa should not occur within 20° of AC line zero crossing.

Dimming control shall provide selection, via program entry (individual Green, Yellow, Red, Walk, Ped Clear, and Dont Walk output), of which load switch driver shall have a "Dimmed" output and which half cycle (+ or -) shall be eliminated.

When the Type A2 and P2 CU is used in a cabinet that employs Absence of Red Monitoring with a NEMA TS 1 Monitor, the user may be required to make a choice between:

1. Absence of Red Monitoring.
2. Dimming the Red Display.

For additional information about this subject, reference is made to Federal Highway Administration Report No. FHWA-TS-85-213 entitled "Traffic Signal Brightness: An Examination of Nighttime Dimming." (Authorized Engineering Information.)

Some types of signals may not operate properly or may be damaged if dimmed. (Authorized Engineering Information.)

3.9.3 Diagnostics

The CU shall be provided with a resident series of diagnostic capabilities describing its own internal state. It shall not require internal access or changes to the CU to initiate diagnostic programs.

3.9.3.1 AUTOMATIC DIAGNOSTICS

The CU shall perform diagnostics automatically (i.e., without operator request) to verify essential elements are operating properly and take the action defined herein based on those diagnostics.

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3.9.3.1.1 Memory

The CU shall contain provisions to verify all memory elements on power up. When a fault is detected, an appropriate Message shall be displayed and the unit shall maintain the Start-Up Flash state.

As a minimum, the following memory diagnostics shall be performed:

1. RAM Diagnostic: This test shall verify that all RAM is operating correctly. Patterns shall be automatically written to RAM. Each Write shall be followed by a read and compare to verify that it contains the pattern.
2. ROM Diagnostic: This test shall verify that the Operating System ROM contains the proper program. The routine shall perform a check on ROM and make a comparison with a pre-programmed value.
3. Non-Volatile Memory Diagnostic: This test shall verify whether the Non-Volatile Memory contain data and that data has not changed since the last write. The routine shall perform a check on Non-Volatile Memory and make a comparison with a preprogrammed value.

   The CU shall continue to verify ROM and Non-Volatile Memory during normal operation at a minimum rate of 1024 bytes per second. When a fault is detected, the unit shall initiate and maintain the Start-Up Flash state.

3.9.3.1.2 Processor Monitor

The CU shall contain provisions to monitor the operation of the microprocessor. The monitor shall receive signals, at least, once every 100 milliseconds from the microprocessor. When the signal is not received for 1 second maximum, the processor monitor shall initiate flashing operation (**Fault Monitor** and **Voltage Monitor** output inactive).

3.9.3.1.3 Port 1

When AC power is present and the Port 1 **Disable** Input is not **True**, the CU shall transmit Command Frames and expect Response Frames in accordance with 3.3.1.4 and as defined here.

The CU shall log Response Frame Faults in non-volatile memory event history. Each logged event shall denote the date, time, and Response Frame Number.

1. MMU Compatibility Programming

Command Frame ..: 3

Response Frame .: 131

The CU shall transmit the Command Frame in accordance with 3.3.1.4.

A Response Frame Fault shall be logged in event history when more than 5 out of the most recent 10 Response Frame transfers are not received.

Actuated CUs shall verify the MMU Channel to Signal Driver Group Utilization (See 3.3.1.4-1.a) with the phase sequence.

Following a power interruption, when the compatibility defined in the Response Frame does not compare to the resident channel utilization or a Response Frame Fault occurs, the CU shall not exit the Start-Up Flash state.

Otherwise (actuated CUs only), when the program entry definition is not compatible with the sequence, the compatibility defined in the Response Frame does not compare to the resident channel utilization, or a Response Frame Fault occurs, the CU shall initiate flashing operation (**Fault Monitor** and **Voltage Monitor** Output inactive and Load Switch Driver Red Output Flashing).

2. MMU Field Status

Command Frame ..: 1

Response Frame .: 129

The CU shall transmit the Command Frame in accordance with 3.3.1.4.

A Response Frame Fault shall be logged in event history when more than 5 out of the most recent 10 response Frame transfers are not received.

The CU shall evaluate the Response Frame with the MMU Channel to Signal Driver Group Utilization (See 3.3.1.4 1.a) and determine if incompatible channels are active.

When the above conditions have been true for 10 consecutive Response Frame transfers and the Response Frame indicates the MMU has not transferred to the Fail State or a Response Frame Fault occurs, the CU shall initiate flashing operation (**Fault Monitor** and **Voltage Monitor** Output inactive and Load Switch Driver Red Output Flashing).

3. Signal Control Output Status

Command Frame ..: 0

Response Frame .: 128

The CU shall transmit the Command Frame in accordance with 3.3.1.4.

A Response Frame Fault shall be logged in event history when more than 5 out of the most recent 10 Response Frame transfers are not received.

When a Response Frame Fault occurs, the CU shall initiate flashing operation (**Fault Monitor** and **Voltage Monitor** Output inactive and Load Switch Driver Red Output Flashing).

4. Terminal & Facilities (Type A1 and P1 CU)

Command Frame ..: 10–13

Response Frame .: 138–141

The CU shall transmit each Command Frame in accordance with 3.3.1.4.

A Response Frame Fault shall be logged in event history when more than 5 out of the most recent 10 Response Frame transfers (138–141 exclusive) are not received.

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When a Response Frame Fault occurs, the CU shall initiate flashing operation (**Fault Monitor** and **Voltage Monitor** Output inactive and Load Switch Driver Red Output Flashing).

5. Detector Racks

Command Frame ..: 20–23

Response Frame .: 148–151

The CU shall transmit the Command Frame in accordance with 3.3.1.4.

A Response Frame Fault shall be logged in event history when more than 5 out of the most recent 10 Response Frame transfers (148–151 exclusive) are not received.

When a Response Frame Fault occurs, the CU shall operate as though a continuous call is present on all enabled respective detectors.

6. Detector Racks

Command Frame ..: 24–27

Response Frame .: 152–155

The CU shall transmit the Command Frame in accordance with 3.3.1.4.

A Response Frame Fault shall be logged in event history when more than 5 out of the most recent 10 Response Frame transfers (152–155 exclusive) are not received.

7. Auxilliary Input/Output (Type A1 and P1 CU)

Command Frame ..: 30

Response Frame .: 158

The CU shall transmit the Command Frame in accordance with 3.3.1.4.

A Response Frame Fault shall be logged in event history when more than 5 out of the most recent 10 Response Frame transfers are not received.

8. Transfer Outputs Frame (Type A1 and P1 CU)

Command Frame ..: 18

The CU shall transmit the Command Frame in accordance with 3.3.1.4.

A Transfer Outputs Frame Fault shall be logged in event history when the Transfer Outputs Frame has not been transmitted for 500 milleseconds.

When a Transfer Outputs Frame Fault occurs, the CU shall initiate flashing operation (**Fault Monitor** Output inactive and Load Switch Driver Red Output Flashing).

3.9.3.1.4 Detector Diagnostics

Each active detector (Vehicle and Pedestrain enabled by assignment) shall be capable of being tested by diagnostics for conformance to specified parameters. The detector diagnostics shall monitor activity on each active detector for constant calls, absence of calls, or erratic output.

An active detector is classified as "On-Line" when the results of the Diagnostic procedures indicate that data from the detector is within the allowable range of values.

An active detector is classified as "Failed" when the results the Diagnostic procedures indicate that data from the detector is not within the allowable range of values.

1. **No Activity:** If an active detector does not exhibit an actuation during a program entered period (00–255 minutes in one minute increments), it is considered a fault by the diagnostics and the detector is classified as "Failed."
2. **Maximum Presence:** If an active detector exhibits continuous detection for a program entered period (00–255 minutes in one minute increments), it is considered a fault by the diagnostics and the detector is classified as "Failed."
3. **Erratic Output:** If an active detector exhibits excessive actuations (program entered maximum counts per minute 00–255 in increments of one), it is considered a fault by the diagnostics and the detector is classified as "Failed."
4. **Fault Status:** When a Fault status defined in the respective Response Frame 152 to 155 is **True** for an active detector, it is considered a fault by the diagnostics and the detector is classified as:
   a. "Failed - Watchdog," or
   b. "Failed - Open Loop," or
   c. "Failed - Shorted Loop," or
   d. "Failed - Excess Change,"

Indications shall be provided to facilitate the determination of current diagnostic status of each detector.

The CU shall include a program entry for No Activity, Maximum Presence, and Erratic Output for each detector. The respective diagnostic shall be disabled when the program entry is "00."

When a detector is classified as "Failed" by these diagnostics, the CU shall operate as though a continuous call is present until such time as the detector is classified as "On-Line."

The CU shall log detector diagnostic status (i.e., On-Line or Failed) in non-volatile memory event history. Each logged event shall denote the date and time of occurrence.

The Detector Report shall have the capacity to store a minimum of 50 events. The events once logged shall remain until the report capacity is exceeded at which time the oldest event shall be deleted and the new one shall be added.

3.9.3.1.5 Events Report

The CU shall monitor activity and log status in non-volatile memory event history. Events to be logged shall be selected via program entry. Each logged event shall denote the date and time of occurrence.

The following events shall be monitored and the status of each selected event shall be logged in the Events Report:

1. **Cycle Fault:** When the local CU is operating in the coordinated mode and cycling diagnostics indicate

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that a serviceable call exists that has not been serviced for two cycles, the Status shall be logged as a **Cycle Fault.** The local intersection shall automatically revert to Free.

2. **Coord Fault:** When a Cycle Fault is in effect and the serviceable call has been serviced within two cycles after the Cycle Fault, the Intersection Status shall be logged as a **Coord Fault.** A coordination retry shall be attempted. If a Cycle Fault does not occur again within two cycles, the Status shall be logged as **Coord Active,** if no other failure or coord fault condition exists.
3. **Coord Failure**: When a Coord Fault is in effect and a Cycle Fault occurs again within two cycles of the coordination retry, the Status shall be logged as a **Coord Failure** and shall not attempt another coordination retry prior to entry of phase, unit, or coord data or the AC power being recycled to the CU.
4. **Cycle Failure**: When a local CU is operating in the non-coordinated mode, whether the result of a Cycle Fault or Free being the current normal mode, and cycling diagnostics indicate that a serviceable call exists that has not been serviced for two cycles, the Status shall be logged as a **Cycle Failure**. The intersection shall automatically and immediately revert to Flash (**Fault Monitor** and **Voltage Monitor** Inactive). The CU shall not exit this state prior to the entry of phase or unit data or AC power being removed and reapplied.

The cycling diagnostic shall be a phase by phase test. For the purpose of this test, the following definitions are included:

Not Serviced—A phase does not go green.

Serviceable Call—A phase has a call and can be serviced normally.

Serviced Normally—The following conditions are true:

a. The Phase Is Active
b. The Phase Omit Is Not Active
c. No Phase Hold Is Active
d. External Start Is Not Active
e. No Stop Time Is Active
f. Manual Control Enable Is Not Active
g. Programmed Flash Is Not Active

Two Cycles—When running coordinated, two times the pattern cycle length. When running non-coordinated, two times the longest path between barriers (Maximum Green, Yellow, and Red times sum).

5. **MMU Flash:** Should the CU MMU Flash input remain active for a period of time exceeding the Start-Up Flash time, the Status is logged as a **MMU Flash.** If subsequent to a MMU Flash logging the MMU Flash input is removed, the Status shall be logged as ON-LINE if no other failure is present.
6. **Local Flash**: Should the CU Local Flash input become active, MMU Flash input is not active, and Flash is not commanded by the Master, the Status shall be logged as a **Local Flash.** If subsequent to a Local Flash logging the Local Flash input is removed, the Status shall be logged as **On-Line** if no other failure is present.
7. **Preempt**: Should any of the CU Preempt inputs become active, the Status shall be logged as a **Preempt #.** If subsequent to a Preempt logging the Preempt input is removed, the Status shall be logged as **On-Line** if no other failure is present.
8. **Local Free:** Should any of the CU inputs and/or programming cause it to not respond to coordination control, the Status shall be logged as **Local Free.** If subsequent to a Local Free logging the CU becomes able to respond to coordination control, the Status shall be logged as **Coord Active** if no other failure is present.
9. **Power On/Off**: Should a power interruption occur, the Status shall be logged as **Power Off.** When power returns the Status shall be logged as **Power On.**
10. **Low Battery**: Should any battery voltage fall below the required level, the Status shall be logged as **Low Battery.**
11. **Response Fault**: Should a response fault occur (3.9.3.1.3 Port 1), the Status shall be logged as **Response Fault** along with the Response Frame number which caused the fault.
12. **Alarm 1** and **Alarm 2**: Should any of the CU Alarm inputs become active, the Status shall be logged as an **Alarm #.**

The Events Report shall have the capacity to store a minimum of 100 alarms. The alarms once logged shall remain until the report capacity is exceeded at which time the oldest alarm shall be deleted and the new one shall be added.

3.9.3.2 OPERATOR INITIATED DIAGNOSTICS

The CU shall perform diagnostics enabling operator verification of properly operating inputs, outputs, keypad, and display.

The "operator initiated" diagnostics shall be performed only after an operator request through the CU keypad. The intersection shall automatically and immediately revert to Flash (**Fault Monitor** and **Voltage Monitor** Inactive) during this diagnostic. The diagnostics evaluation shall be displayed on the CU front panel display and/or indications on a Controller Test Set as an operator interface.

This diagnostic is not intended for use while the CU is in control of intersection operation. (Authorized Engineering Information).

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3.9.3.2.1 Inputs

The CU shall provide test routines to enable operator verification that input functions are proper. This test shall determine whether the input buffers are operating correctly. The user shall activate each input. The routine shall identify each input by an indication on the front panel.

The user shall observe the front panel display and determine correct operation.

3.9.3.2.2 Outputs

The CU shall provide test routines to enable operator verification that output functions are proper. This test shall determine whether the output drivers are operating correctly. Each output shall be actuated in a fixed sequence. The user shall observe the output sequence and determine correct operation.

3.9.3.2.3 Integral Display

The CU shall provide test routines to enable operator verification that display functions are proper. This test shall determine whether front panel drivers and decoders are operating properly. All the indicators shall be activated. The user shall observe the front panel display and determine correct operation.

3.9.3.2.4 Integral Keypad

The CU shall provide test routines to enable operator verification that keypad functions are proper. This test shall determine whether the keypad is operating correctly. The operator shall test each of the CU keys. The display shall indicate the key pressed. The user shall observe the front panel display and determine correct operation.

3.10 FUTURE

The CUs defined by this standard includes provision for future addition and/or modification that shall not be deemed to be impossible due to Input-Output Interface limitations.

Future functional capabilities may be limited to Type A1 and P1 CUs (Authorized Engineering Information).

3.11 PROGRAMMING

The CU shall provide means to enter and view variable data, view current status, and view the event report.

3.11.1 Entry

The method of entering CU variables shall be by:

1. An integral keypad on the face of the unit, and
2. Via Port 2 RS-232C Interface and a Personal Computer

3.11.2 Display

The method provided to view CU variables, current status, and the event report shall be by:

1. Integral Indication on the face of the unit
   and
2. Via Port 2 RS-232C Interface and a Personal Computer

The method provided shall include a simultaneous display of a minimum of two lines, 16 characters per line of ASCII text (HEX 20 through HEX 7A).

3.11.3 Security

The CU shall maintain user programmable variables in non-volatile memory to assure continued proper CU operation with return of power after power loss.

3.11.4 Backup

The CU shall contain a reserve data base of all CU variables stored in Non-Volatile Memory. The reserve data base may be manually copied into active memory by the user.

3.12 POWER INTERRUPTION

A power interruption is defined as 0 volts AC.

Two or more power interruptions which are separated by power restorations of 1500 or more milliseconds shall be considered as separate interruptions.

Three interruptions of 300 milliseconds or less which are separated by power restorations of 300 milliseconds or more shall not cause the CU to revert to its start-up state.

The CU shall react to a power interruption, upon restoring power, as follows:

1. Interruption of 500 Milliseconds or Less: Shall continue to operate as though the power interruption had not occurred.
2. Interruption of More Than 500 Milliseconds and Less than 1000 Milliseconds: Shall either continue to operate (3.12(1)) or shall revert to its start-up state (3.12(3)).
3. Interruption of 1000 Milliseconds or More: Shall revert to its start-up state.

3.13 TEST

The CU shall perform its specified functions under the conditions set forth in Section 2, Environmental Requirements. Clause 3.13 defines the test procedures required to demonstrate the conformance of a CU type with the provisions of the standards.

In the interest of ensuring safe and reliable operation of the CU covered by these standards, the stress levels which the tests encompass are nominal "Worse-Case" conditions the units experience in operation. These tests are intended for type acceptance testing not a production testing. (Authorized Engineering Information)

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3.13.1 Timing Accuracy

3.13.1.1 DEVIATION

The CU shall maintain all of the programmed functions within the maximum timing deviation.

3.13.1.2 SETABILITY AND REPEATABILITY

The accuracy of the timing of any interval portion is limited by the setability and repeatability error of that interval portion's readout and setting device.

1. Setability is the difference between the indication and the actual timings obtained.

2. Repeatability is the measure of the duplicating capability for repetitive timings of a given setting. (Authorized Engineering Information)

3.13.2 Timing

Timing shall be accomplished by digital methods. The setability shall be in discrete increments. The timing shall relate to the power line frequency so that no cumulative or drift errors shall occur in timing intervals. Any interval timed shall not deviate by more than 100 milliseconds from its set value at a power source frequency of 60 hertz.

3.13.3 Vibration

The CU shall maintain the programmed functions and physical integrity when subjected to a vibration of 5 to 30 cycles per second up to 0.5 gravity applied in each of three mutually perpendicular planes.

3.13.4 Shock

The CU shall suffer neither permanent mechanical deformation nor any damage that renders the unit inoperable, when subjected to a shock of 10G applied in each of three mutually perpendicular planes.

3.13.5 Test Facilities

All instrumentation required in the test procedures, such as voltmeters, ammeters, thermocouples, pulse timers, etc. shall be selected in accordance with good engineering practice. In all cases where time limit tests are required, the allowance for any instrumentation errors shall be included in the limit test.

1. Variable Voltage Source: A variable source capable of supplying 10 amperes from 89 to 135 volts AC.

2. Environmental Chamber: An environmental chamber capable of attaining temperatures of -34°C (-30°F) to +74°C (+165°F) and relative humidities given in Table 2-1.

3. Transient Generator(s): Transient generator(s) capable of supplying the transients outlined in 2.1.6 through 2.1.8.

3.13.6 Test Unit

The test unit shall consist of one CU.

3.13.7 Test Procedure: Transients, Temperature, Voltage, and Humidity

3.13.7.1 TEST A: PLACEMENT IN ENVIRONMENTAL CHAMBER AND CHECK-OUT OF HOOK-UP

1. Place the test unit in the environmental chamber. Connect the test unit AC input circuit to a variable voltage power transformer, voltmeter, and transient generator. The transient generator shall be connected to the AC input circuit at a point at least 4.6 meters (15 feet) from the AC power source and not over 3 meters (10 feet) from the input to the test unit.
2. Connect test switches to the appropriate terminals to simulate the various features incorporated into the test unit. Place these switches in the proper position for desired operation.
3. Verify the test hook-up. Adjust the variable-voltage power transformer to 120 volts AC and apply power to the test unit. Verify that the test unit goes through its prescribed start-up sequence and cycles properly in accordance with the operation determined by the positioning of test switches in item 2.

Upon the satisfactory completion and verification of the test hook-up, proceed with Test B.

3.13.7.2 TEST B: TRANSIENT TESTS (POWER SERVICE)

1. Program the test unit to dwell. Verify the input voltage is 120 volts AC.
2. Set the transient generator to provide high-repetition noise transients as follows:
   a. Amplitude: 300 volts ± 5 percent, both positive and negative polarity.
   b. Peak Power: 2500 watts.
   c. Repetition Rate: one pulse every other cycle moving uniformly over the full wave in order to sweep once every 3 seconds across 360 degrees of line cycle.
   d. Pulse Rise Time: 1 microsecond.
   e. Pulse Width: 10 microseconds.
3. Apply the transient generator output to the AC voltage input for at least 5 minutes. Repeat this test for at least two conditions of dwell for the test unit. The test unit must continue to dwell without malfunction.
4. Program the test unit to cycle. Turn on the transient generator (output in accordance with item 2) for 10 minutes, during which time the test unit shall continue to cycle without malfunction.
5. Set a transient generator to provide high-repetition noise transients as follows:

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a. Amplitude: 300 volts ±5 percent, both positive and negative polarity.
b. Source Impedance: not less than 1000 ohms nominal impedance.
c. Repetition: one pulse per second for a minimum of five pulses per selected terminal.
d. Pulse Rise Time: 1 microsecond.
e. Pulse Width: 10 microseconds.

Program the test unit to dwell. Verify the input voltage is 120 volts AC.

6. Apply the transient generator (output in accordance with item 5) between logic ground and the connecting cable termination of selected Connector A, B, or C input/output terminals of the test unit.

   A representative sampling of selected input/output terminations shall be tested. The test unit shall continue to dwell without malfunction.

7. Program the test unit to cycle. Turn on the transient generator (output in accordance with item 5) and apply its output to the selected Connector A, B, or C input/output terminations. The test unit shall continue to cycle without malfunction.

8. Set a transient generator to provide low-repetition high-energy transients as follows:
   a. Amplitude: 600 volts ±5 percent, both positive and negative polarity.
   b. Energy Discharge Source: capacitor, oil-filled, 10 microfarads.
   c. Repetition Rate: one discharge each 10 seconds.
   d. Pulse Position: random across 360 degrees of line cycle.

9. Program the test unit to dwell. Verify the input voltage is 120 volts AC.

10. Discharge the oil-filled 10-microfarad capacitor ten times for each polarity across the AC voltage input. Repeat this test for at least two conditions of dwell. The test unit shall continue to dwell without malfunction.

11. Program the test unit to cycle. Discharge the capacitor ten times for each polarity while the test unit is cycling, during which time the test unit shall continue to cycle without malfunction.

12. During the preceding transient tests (item 3 through 11), the test unit must continue its programmed functions.

    The test unit shall not skip intervals or interval portions when cycling; place false calls or produce false indications while in dwell; disrupt normal sequences in any manner; or change timings.

13. Non-destruct Transient Immunity:
    a. Turn off the AC power input to the test unit from the variable-voltage power source.
    b. Apply the following high-energy transient to the AC voltage input terminals of the test unit (no other power connected to terminals):
       (1) Amplitude: 1000 volts, both positive and negative polarity.
       (2) Peak Power Discharge: capacitor, oil-filled, 15 microfarads.
       (3) Maximum Repetition Rate: applied to the CA once every 2 seconds for a maximum of three applications for each polarity.
    c. Upon completion of the foregoing, apply 120 volts AC to the test unit and verify that the test unit goes through its prescribed start-up sequence and cycles properly in accordance with the programmed functions. The first operation of the over-current protective device during this test shall not be considered a failure of the test unit.

NOTE - Test C through G follow the profile indicated in Figure 3.13-1 to demonstrate the ability of the test unit to function reliably under stated conditions of temperature, voltage and humidity.

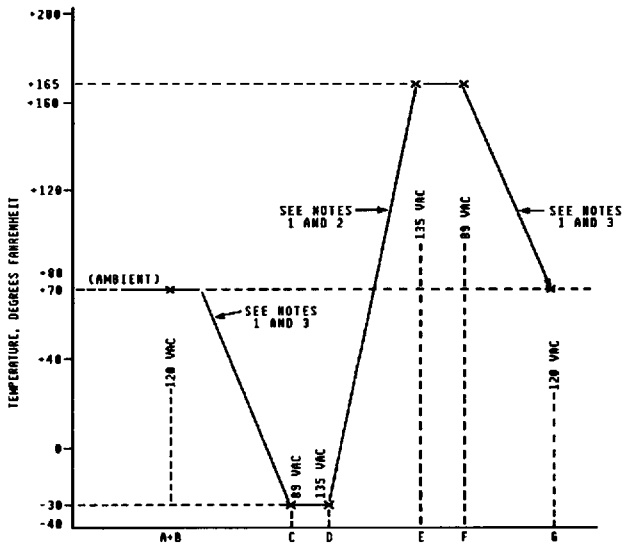

Figure 3.13-1
TEST PROFILE

Figure 3.13.-1 Notes:

Note 1 - The rate of change in temperature shall not exceed 17°C (30oF) per hour.

Note 2 - Humidity controls shall be set in conformance with the humidities given in Table 2-1 during the temperature change between Test D and Test E.

Note 3 - If a change in both voltage and temperature are required for the next test, the voltage shall be selected prior to the temperature change.

3.13.7.3 TEST C—LOW-TEMPERATURE LOW-VOLTAGE TESTS

1. Definition of Test Conditions
   a. Environmental Chamber Door: closed.
   b. Temperature: -34°C (-30°F).
   c. Low Voltage: 89 volts AC.

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d. Humidity Control: off.

2. Test Procedure: While at room temperature, adjust the input voltage to 89 volts AC and verify that the test unit is still operable.

a. With the test unit cycling, lower the test chamber to -34°C (-30°F) at a rate not exceeding 17°C (30°F) per hour. Allow the test unit to cycle for a minimum of 5 hours at -34°C (-30°F) with the humidity controls in the off position. Then operate the test switches as necessary to determine that all functions are operable.

b. Power shall then be removed from the test unit for a minimum period of 5 hours. Upon restoration of power, the test unit shall go through its prescribed start-up sequence and then resume cycling.

c. With the test unit at -34°C (-30°F) and the input voltage at 89 volts AC, the following items shall be evaluated against their respective standards:

3.13.10 Power Interruption Tests
3.13.11 Timing Accuracy Tests
3.13.11.2 Repeatability

On satisficatory completion of this test, proceed with test D.

3.13.7.4 TEST D—LOW-TEMPERATURE HIGH-VOLTAGE TESTS

1. Definition of Test Conditions

a. Environmental Chamber Door: closed.
b. Low Temperature: -34°C (-30°F)
c. High Voltage: 135 volts AC.
d. Humidity Controls: off.

2. Test Procedure: While at -34°C (-30°F) and with humidity controls off, adjust the input voltage to 135 volts AC and allow the test unit to cycle for 1 hour. Then operate the test switches as necessary to determine that all functions are operable.

3. With the test unit at -34°C (-30°F) and the input voltage at 135 volts AC (humidity controls off), the following items shall be evaluated against their respective standards:

3.13.10 Power Interruption Tests
3.13.11 Timing Accuracy Tests
3.13.11.2 Repeatability

On satisfactory completion of this test, proceed to Test E.

3.13.7.5 TEST E—HIGH-TEMPERATURE HIGH-VOLTAGE TESTS

1. Definition of Test Conditions

a. Environmental Chamber Door: closed.
b. High Temperature: 74°C (+165°F).
c. High Voltage: 135 volts AC.
d. Humidity Controls: in accordance with the humidities given in Table 2-1.

2. Test Procedure—With the test unit cycling, raise the test chamber to +74°C (+165°F) at a rate not to exceed 17°C (30°F) per hour. Verify the input voltage is 135 volts AC.

Set the humidity controls to not exceed 95 percent relative humidity over the temperature range of 4.4°C (40°F) to 43.3°C (110°F). When the temperature reaches 43°C (109°F), readjust the humidity control to maintain constant absolute humidity; 43°C (109°F) wet bulb which results in the relative humidities shown in Table 2-1. Verify that the test unit continues to cycle satisfactory during the period of temperature increase and at established levels of relative humidity.

a. Allow the test unit to cycle for a minimum of 15 hours at 74°C (165°F) and 18 percent relative humidity. Then operate the test switches as necessary to determine that all functions are operable.

b. With the test unit at 74°C (165°F) and 18 percent relative humidity and the input voltage at 135 volts AC, the following items shall be evaluated against their respective standards:

3.13.10 Power Interruption Tests
3.13.11 Timing Accuracy Tests
3.13.11.2 Repeatability

On satisfactory completion of this test, proceed to Test F.

3.13.7.6 TEST F—HIGH-TEMPERATURE LOW-VOLTAGE TESTS

1. Definition of Test Conditions

a. Environmental Chamber Door: closed.
b. High Temperature: 74°C (165°F).
c. Low Voltage: 89 volts AC.
d. Humidity Controls: 18 percent relative humidity and 43°C (109°F) wet bulb.

2. Test Procedure: Adjust the input voltage to 89 volts AC and proceed to operate the test switches to determine that all functions are operable. With the test unit at 74°C (165°F) and 18 percent relative humidity, 43°C (109°F) wet bulb, and the input voltage at 89 volts AC, the following items shall be evaluated against their respective standards:

3.13.10 Power Interruption Tests
3.13.11 Timing Accuracy Tests
3.13.11.2 Repeatability

On satisfactory completion of this test, proceed to Test G.

3.13.7.7 TEST G—TEST TERMINATION

1. Program the test unit to cycle.
2. Adjust the input voltage to 120 volts AC.
3. Set the controls on the environmental chamber to return to room temperature, 15°C (60°F) to 27°C (80°F), with the humidity controls in the off position. The rate of temperature change shall not exceed 17°C (30°F) per hour.
4. Verify the test unit continues to cycle properly.

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5. Allow the test unit to stabilize at room temperature for 1 hour. Proceed to operate the test switches to determine that all functions are operable.

3.13.7.8 TEST H—APPRAISAL OF EQUIPMENT UNDER TEST

1. A failure shall be defined as any occurrence which results in other than normal operation of the equipment. (See item 2 for details.) If a failure occurs, the test unit shall be repaired or components replaced, and the test during which failure occurred shall be restarted from its beginning.
2. The test unit is considered to have failed if any of the following occur:
   a. If the test unit skips intervals or interval portions, places false calls, presents false indications, exhibits disruption of normal sequence, or produces changes in timing beyond specified tolerances, or
   b. If the test unit fails to satisfy the requirements of 3.13.7 Tests A to G, inclusive.
3. An analysis of the failure shall be performed and corrective action taken before the test unit is retested in accordance with this standard. The analysis must outline what action was taken to preclude additional failures during the tests.
4. When the number of failures exceeds two, it shall be considered that the test unit fails to meet these standards. The test unit may be completely retested after analysis of the failure and necessary repairs have been made in accordance with item 3.
5. Upon completion of the tests, the test unit shall be visually inspected. If material changes are observed which will adversely affect the life of the test unit, the cause and conditions shall be corrected before making further tests.
6. Upon satisfactory completion of all of the tests described in 3.13.7.1 through 3.13.7.7, the test unit shall be tested in accordance with 3.13.8.

3.13.8 Vibration Test

3.13.8.1 PURPOSE OF TEST

This test is intended to duplicate vibrations encountered by the test unit when installed at its "street-corner" location.

The test unit shall be fastened securely to the vibration test table prior to the start of the test.

3.13.8.2 TEST EQUIPMENT REQUIREMENTS

1. Vibration table with adequate table surface area to permit placement of the test unit.
2. Vibration test shall consist of:
   a. Vibration in each of three mutually perpendicular planes.
   b. Adjustment of frequency of vibration over the range from 5 to 30 hertz.
   c. Adjustment of test table excursion (double amplitude displacement) to maintain a G value, measured at the test table, of 0.5G; as determined by the following formula:

$$G = 0.0511df^2$$

Where-
d = excursion in inches
f = frequency in cycles per second

3.13.8.3 RESONANT SEARCH

1. With the test unit securely fastened to the test table, set the test table for a double amplitude displacement of 0.015 inch.
2. Cycle the test table over a search range from 5 to 30 cycles per second and back within a period of 12-1/2 minutes.
3. Conduct the resonant frequency search in each of the three mutually perpendicular planes.
4. Note and record the resonant frequency determined from each plane.
   a. In the event of more than on resonant frequency in a given plane, record the most severe resonance.
   b. If resonant frequencies appear equally severe, record each resonant frequency.
   c. If no resonant frequency occurs for a given plane within the prescribed range, 30 cycles per second shall be recorded.

3.13.8.4 ENDURANCE TEST

1. Vibrate the test unit in each plane at its resonant frequency for a period of 1 hour at an amplitude resulting in 0.5G acceleration.
2. When more than one resonant frequency has been recorded in accordance with 3.13.8.3(4), the test period of 1 hour shall be divided equally between the resonant frequencies.
3. The total time of the endurance test shall be limited to 3 hours, 1 hour in each of three mutually perpendicular planes.

3.13.8.5 DISPOSITION OF EQUIPMENT UNDER TEST

1. The test unit shall be examined carefully to determine that no physical damage has resulted from the vibration tests.
2. The test unit shall be carefully checked to determine that it is functionally operable in all modes of its prescribed operation.
3. The test unit may be removed from the test table. Upon satisfactory completion of the vibration test, proceed with the shock (impact) test described in 3.13.9.

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3.13.9 Shock (Impact) Test

3.13.9.1 PURPOSE OF TEST

The purpose of this test is to determine that the test unit is capable of withstanding the shock (impact) to which it may reasonably be subjected during handling and transportation in the process of installation, repair, and replacement. It is to be noted that the test unit is not, at this time, in its shipping carton.

The test unit shall be firmly fastened to the specimen table. In each of its three planes the test unit shall be dropped from a calibrated height to result in a shock force of 10G's.

3.13.9.2 TEST EQUIPMENT REQUIREMENTS

1. Shock (impact) test fixture equivalent to that suggested by the simplified sketch shown in Figure 3.13-2.

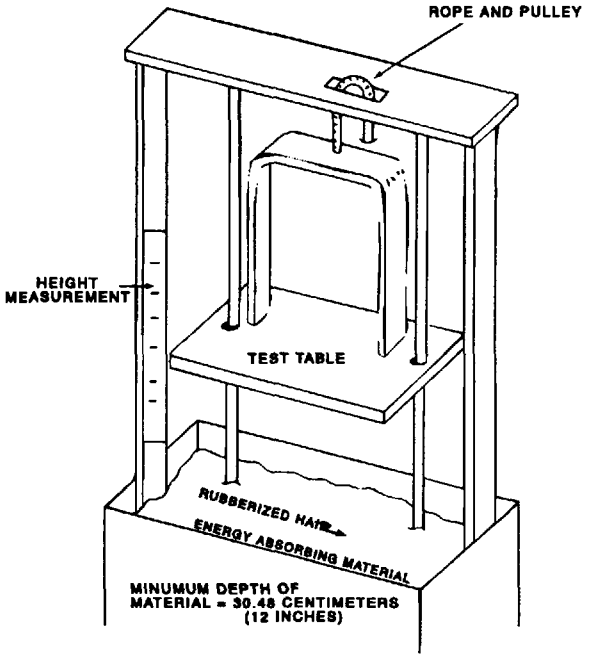

Figure 3.13-2
SHOCK TEST FIXTURE

2. The test table shall have a surface area sufficient to accommodate the test unit.
3. The test table shall be calibrated and the items tested as indicated. This shock test defines the test shock to be 10G +1G.
   a. Calibration of the test equipment for these shock tests shall be measured by three accelerometers having fixed shock settings of 9G, 10G, and 11G. They shall be Inertia Switch Incorporated's ST-355, or the equivalent. These devices shall be rigidly attached to the test table.
   b. Calibration of the fixture for each item to be tested shall be as follows:
      (1) Place a dummy load weighing within 10 percent of the test unit on the table.
      (2) Reset the three accelerometers and drop the test table from a measured height.
      (3) Observe that the accelerometers indicate the following:
         (a) The 9G accelerometer shall be activated.
         (b) The 10G unit may or may not be actuated.
         (c) The 11G unit shall not be actuated.
   c. Repeat calibration test (a) and (b) adjusting the height of the drop until, on ten successive drops, the following occurs:
      (1) The 9G unit is actuated ten times.
      (2) The 10G unit is actuated between four to eight times.
      (3) The 11G unit is not actuated on any of the ten drops.

3.13.9.3 TEST PROCEDURE

1. The calibration height of the drop for the particular item under test as determined in 3.13.9.2 shall be used in this procedure.
2. Secure the test unit to the test table surface so that the test unit rests on one of its three mutually perpendicular planes.
3. Raise the test table to the calibrated height.
4. Release the test table from the calibrated height, allowing a free fall into the box of energy absorbing material below.
5. Repeat the drop test for each of the remaining two mutually perpendicular planes, using the same calibrated height for each drop test of the same test unit.
6. The observations of the accelerometer for the three tests of the test item shall be:
   a. The 9G unit is actuated for all three tests. (Repeat the calibration if the unit is not actuated.)
   b. The 10G unit may or may not be actuated in these tests.
   c. The 11G unit is not actuated on any drop. (If the unit is actuated, repeat the calibration only if the test unit has suffered damage.)

3.13.9.4 DISPOSITION OF TEST UNIT

1. Check the test unit for any physical damage resulting from the drop tests.
2. Check the test unit carefully to determine that it is functionally operable in all modes of its prescribed operation.
3. Satisfactory completion of all environmental tests, including the shock (impact) is required.

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3.13.10 Power Interruption Tests

The following power interruption tests shall be conducted at low input voltage (89 volts AC and high input voltage (135 volts AC) at -34°C (-30°F), and +74°C (+165°F).

3.13.10.1 500-MILLISECOND POWER INTERRUPTION

While the test unit is cycling, remove the input voltage for a period of 500 milliseconds. Upon restoration of the input voltage, check to insure that the test unit continues normal operation as though no power interruption has occurred. Repeat this test three times.

3.13.10.2 1000-MILLISECOND POWER INTERRUPTION

While the test unit is cycling, remove the input voltage for a period of 1000 milliseconds. Upon restoration of the input voltage, check to insure that the test unit reverts to its start-up sequence. Repeat this test three times.

3.13.11 Timing Accuracy Tests

A sampling of at least four intervals (or interval portions) shall be timed as specified in the following procedure.

3.13.11.1 SETABILITY

The range of timing shall, as a minimum requirement, be as shown in 3.4.2.1 or 3.5.3.1.

The range of timing and setability requirements shall be in accordance with the functional standards given in this publication.

Determine that the setting of the interval time has been provided in positive discrete increments in accordance with the functional standards given in this publication for the specific test unit.

3.13.11.2 REPEATABILITY

At all stabilized temperatures specified in 3.13.7.2 through 3.13.7.7, each interval shall be timed with the digital time indicator for ten consecutive cycles for one given setting for each interval.

Any interval timed shall not deviate by more than ±100 milliseconds from its set value.

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SECTION 4
MALFUNCTION MANAGEMENT UNIT

4.1 OVERVIEW

The standards in Section 4 respond to the need for a **Malfunction Management Unit** (MMU) to accomplish the detection of, and response to, improper and conflicting signals and improper operating voltages in a CA. This standard provides interchangeability between units of different manufacturers and downward compatibility to NEMA Standards Publication TS 1-1989.

The MMU shall detect the presence of voltage on conflicting field connection terminals, the absence of proper voltages on all of the signal field connection terminals of a channel, and shall be capable of monitoring for the presence of satisfactory operating voltages within the CU and the MMU itself.

The MMU upon sensing any of these conditions, shall cause the transfer of the traffic signals to **Flashing Operation**, and the CA shall be wired in such a manner as to provide **Flash Transfer** if the MMU is removed from service (refer to Section 5.5.3).

The standards in Section 4 describe an MMU for 12 or 16 channels. The MMU shall operate in two modes determined by the signal level on the **Type Select** input. If the **Type Select** input is at Logic Ground potential then the MMU will operate as a Type 16 with sixteen channels, otherwise it will operate as a Type 12 with twelve channels.

Type 16—Each of the sixteen channels consists of three 120 volt AC inputs: **Green/Walk; Yellow; Red/Dont Walk.**

Type 12—Each of the twelve channels consists of four 120 volt AC inputs: **Green; Yellow; Walk**; and **Red.**

The Type 16 MMU is intended for those applications in which there are three circuits per channel and the MMU channels have been wired in a one-to-one correspondence with the load switches, as defined in section 5.5.3 paragraph 9 of this standard. The Type 12 MMU is intended to provide downward compatibility with conflict monitors conforming to TS 1-1989. (Authorized Engineering Information)

4.1.1 Basic Capability

The **Signal Monitor** portion of the MMU shall be capable of monitoring for the presence of voltage on conflicting field connection terminals in the CA. For the purpose of conflict determination, a signal on any of the **Green, Yellow,** or **Walk** inputs associated with a channel shall be considered as that channel being active.

The **Signal Monitor** portion of the MMU shall also detect the absence of any required signal voltage on each channel at the field connection terminals in the CA. For this purpose a signal on the **Green, Yellow, Walk,** or **Red/Dont Walk** inputs associated with a channel shall be considered as that channel being active.

The **Voltage Monitor** portion of the MMU shall be capable of monitoring the **Controller Unit Voltage Monitor** output which indicates satisfactory operating voltage in the CU and the +24 volt direct current inputs.

4.1.2 TS 1-1989 Compatibility

The MMU shall be capable of operation in a cabinet designed to TS 1 specification with no loss of TS 1 functionality. Some area of TS 1 functionality will be superseded by this specification. Unless noted otherwise all functions of TS 1-1989, Part 6, shall be complied with by an MMU when it is installed in a CA wired to the requirements of TS 1.

4.2 PHYSICAL

4.2.1 Accessibility

All operating circuitry and components within the MMU shall be readily accessible for maintenance.

4.2.2 Material and Construction of Printed Circuit Assemblies

All printed circuit boards shall meet all requirements as outlined in Section 3.2.3.

4.2.3 Environmental Requirements

The MMU shall perform its specified functions under the conditions set forth in Section 2, Environmental Requirements.

4.2.4 Size

The overall dimensions of the MMU, including mating connector(s) and harness, shall not exceed 11.43 centimeters (4.5 inches) width, 26.67 centimeters (10.5 inches) height, and 27.94 centimeters (11 inches) depth.

4.3 INTERFACE STANDARDS

The MMU shall use an Input/Output Interface conforming to Section 3.3.1 for input/output functions with the CU and Section 4.3.2 for input/output functions with the TF.

If additional input/output terminations are required to allow for the inclusion of additional functional capabilities, such terminations shall be provided on an additional connector which shall not be interchangeable with other connectors on the face of the MMU. The provision of these additional capabilities shall not modify the operating capabilities of the unit when the additional input/output connector is disconnected.

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4.3.1 Port 1 Connector

The Port 1 connector shall be a 15 pin metal shell D subminiature type. The connector shall utilize female contacts with 15 millionths of an inch minimum gold plating in the mating area. The connector shall be equipped with latching blocks. The connector shall intermate with a 15 pin D type connector, AMP Incorporated part number 205206-1 or equivalent, which is equipped with spring latches, AMP Incorporated part number 745012-1, or equivalent. Pin connections shall be as follows:

4.3.1.1 PORT 1 CONNECTOR PIN ASSIGNMENTS

Pin	Function
1	Rx Data+
2	Logic Ground
3	Rx Clock+
4	Logic Ground
5	Tx Data+
6	Logic Ground
7	Tx Clock+
8	Logic Ground
9	Rx Data-
10	Port 1 Disable (0 VDC=disable)
11	Rx Clock-
12	Earth Ground
13	Tx Data-
14	Reserved
15	Tx Clock-

NOTE: Tx pins at the MMU are connected to Rx pins at the CU. Rx pins at the MMU are connected to Tx pins at the CU.

4.3.2 Pin Connections

The MMU shall provide input/output interface pin connections per 4.3.2.1 and 4.3.2.2.

4.3.2.1 CONNECTORS

The connectors on the MMU shall have a metallic shell. The connectors shall be connected to the chassis internally. The connectors shall be mounted on the front of the unit in accordance with the following:

1. Connector A shall intermate with a MS 3116 22-55 SZ
2. Connector B shall intermate with a MS 3116 16-26 S

4.3.2.2 PIN ASSIGNMENTS

Input/output pin terminations shall conform with the following tabulations:

Type 16 Connector-A Pin Terminations

A.	AC Line
B.	Output Relay 1 Open (closes when fault occurs)
C.	Output Relay 2 Closed (opens when fault occurs)
D.	Channel 12 Green
E.	Channel 11 Green
F.	Channel 10 Green
G.	Channel 9 Green
H.	Channel 8 Green
J.	Channel 7 Green
K.	Channel 6 Green
L.	Channel 5 Green
M.	Channel 4 Green
N.	Channel 3 Green
P.	Channel 2 Green
R.	Channel 1 Green
S.	+24 Monitor I
T.	Logic Ground
U.	Earth Ground
V.	AC Neutral
W.	Output Relay 1 Common
X.	Output Relay 2 Common
Y.	Channel 12 Yellow
Z.	Channel 11 Yellow
a.	Channel 10 Walk (Type 12 only)
b.	Channel 10 Yellow
c.	Channel 9 Yellow
d.	Channel 8 Yellow
e.	Channel 7 Yellow
f.	Channel 6 Yellow
g.	Channel 5 Yellow
h.	Channel 3 Yellow
i.	Channel 15 Green
j.	Channel 2 Yellow
k.	Channel 1 Yellow
m.	Controller Voltage Monitor
n.	+24V Monitor Inhibit
p.	Output Relay 1 Closed (opens when fault occurs)
q.	Output Relay 2 Open (closes when fault occurs)
r.	Channel 12 Walk (Type 12 only)
s.	Channel 11 Walk (Type 12 only)
t.	Channel 9 Walk (Type 12 only)
u.	Channel 16 Yellow
v.	Channel 15 Yellow
w.	Channel 13 Yellow
x.	Channel 4 Yellow
y.	Channel 14 Green
z.	Channel 13 Green
AA.	Spare 1
BB.	Reset
CC.	Cabinet Interlock A

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DD.	Cabinet Interlock B
EE.	Channel 14 Yellow
FF.	Channel 16 Green
GG.	Spare 2
HH.	Type Select

Type 16 Connector-B Pin Termination

A.	AC Line
B.	Start-delay Relay Common
C.	Start-delay Relay Open (closes during start delay period)
D.	Channel 12 Red
E.	Channel 11 Red
F.	Channel 9 Red
G.	Channel 8 Red
H.	Channel 7 Red
J.	Channel 6 Red
K.	Channel 5 Red
L.	Channel 4 Red
M.	Channel 2 Red
N.	Channel 1 Red
P.	Spare 1
R.	+24V Monitor II
S.	Spare 2
T.	Channel 13 Red
U.	Start-delay Relay Closed (open during start delay period)
V.	Channel 10 Red
W.	Channel 14 Red
X.	Channel 15 Red
Y.	Channel 16 Red
Z.	Channel 3 Red
a.	Red Enable
b.	Spare 3
c.	Spare 4

Type 12 Connector-A Pin Terminations

A.	AC Line
B.	Output Relay 1 Open (closes when fault occurs)
C.	Output Relay 2 Closed (opens when fault occurs)
D.	Channel 12 Green
E.	Channel 11 Green
F.	Channel 10 Green
G.	Channel 9 Green
H.	Channel 8 Green
J.	Channel 7 Green
K.	Channel 6 Green
L.	Channel 5 Green
M.	Channel 4 Green
N.	Channel 3 Green
P.	Channel 2 Green
R.	Channel 1 Green
S.	+24 Monitor I
T.	Logic Ground
U.	Earth Ground
V.	AC Neutral
W.	Output Relay 1 Common
X.	Output Relay 2 Common
Y.	Channel 12 Yellow
Z.	Channel 11 Yellow
a.	Channel 10 Walk
b.	Channel 10 Yellow
c.	Channel 9 Yellow
d.	Channel 8 Yellow
e.	Channel 7 Yellow
f.	Channel 6 Yellow
g.	Channel 5 Yellow
h.	Channel 3 Yellow
i.	Channel 3 Walk
j.	Channel 2 Yellow
k.	Channel 1 Yellow
m.	Controller Voltage Monitor
n.	+24V Monitor Inhibit
p.	Output Relay 1 Closed (opens when fault occurs)
q.	Output Relay 2 Open (closes when fault occurs)
r.	Channel 12 Walk
s.	Channel 11 Walk
t.	Channel 9 Walk
u.	Channel 8 Walk
v.	Channel 7 Walk
w.	Channel 5 Walk
x.	Channel 4 Yellow
y.	Channel 2 Walk
z.	Channel 1 Walk
AA.	Spare 1
BB.	Reset
CC.	Cabinet Interlock A
DD.	Cabinet Interlock B
EE.	Channel 6 Walk
FF.	Channel 4 Walk
GG.	Spare 2
HH.	Type Select

Type 12 Connector-B Pin Terminations

A.	AC Line
B	Start-delay Relay Common
C.	Start-delay Relay Open (closes during start delay period)
D.	Channel 12 Red
E.	Channel 11 Red
F.	Channel 9 Red
G.	Channel 8 Red
H.	Channel 7 Red
J.	Channel 6 Red
K.	Channel 5 Red
L.	Channel 4 Red
M.	Channel 2 Red

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N.	Channel 1 Red
P.	Spare 1
R.	+24V Monitor II
S.	Spare 2
T.	Channel 13 Red (Type 16 only)
U.	Start-delay Relay Closed (open during start delay period)
V.	Channel 10 Red
W.	Channel 14 Red (Type 16 only)
X.	Channel 15 Red (Type 16 only)
Y.	Channel 16 Red (Type 16 only)
Z.	Channel 3 Red
a.	Red Enable
b.	Spare 3
c.	Spare 4

Connector-B pins: T, W, X, Y are called out as spare pins in TS 1-1989. (Authorized Engineering Information)

Open contacts of the **Output** relay are the contacts which are open when the MMU is in the no conflict state and all voltages are sufficient for proper operation of the CA. (Authorized Engineering Information)

4.3.3 Inputs

4.3.3.1 AC LINE

The over-current protected side of 120 volt AC 60 hertz source. This input shall be employed to generate the voltages required to operate the monitoring logic.

The MMU shall have a front panel mounted over-current protection device in the 120 volt AC input to the unit.

4.3.3.2 AC NEUTRAL

The unfused and unswitched return side of 120 volt AC 60 hertz power source taken from the neutral output of AC power source. This input shall be the reference signal for all field terminal voltage sensing inputs. This input shall not be connected to **Logic Ground** or **Earth Ground** within the unit.

4.3.3.3 EARTH GROUND

The MMU shall have an input terminal providing an independent connection to the chassis of the unit. This input shall not be connected to the **Logic Ground** or **AC Neutral** within the unit.

4.3.3.4 LOGIC GROUND

A voltage reference point and current return for the **Reset** input, **Controller Voltage Monitor** input, **+24V Monitor I** input, **+24V Monitor II** input, **Type Select** input, **+24V Monitor Inhibit** input and **Port 1 Disable** input logic circuits. This termination shall not be connected to either the **AC Neutral** or **Earth Ground** within the unit.

4.3.3.5 +24V MONITOR DC INPUTS

Two +24 volt DC inputs are monitored to assure proper +24 volt DC levels.

4.3.3.6 CONTROL INPUTS

The **Reset** input, **Controller Voltage Monitor** input, **+24V Monitor Inhibit** input, **Type Select** input and **Port 1 Disable** input are logic level inputs and shall conform to the requirements of Section 3.3.5.1. The MMU shall respond to these inputs as indicated in Sections 4.4.9, 4.4.8, 4.4.7, 4.3.3.10, and 4.4.6.

4.3.3.7 CABINET INTERLOCK

The MMU shall have two terminals internally connected (#22AWG minimum jumper) to indicate the presence of the unit to the external circuitry. These terminals shall be identified as **Cabinet Interlock A** and **Cabinet Interlock B.**

4.3.3.8 FIELD TERMINALS

Type 16: Three inputs shall be provided for each channel to permit the monitoring of voltages at the **Green/Walk, Yellow**, and **Red/Dont Walk** signal field terminals. The unit shall be designed so that it shall not be necessary to terminate unused **Green, Yellow,** or **Walk** signal sensing inputs when the impedance to AC Line of each of these inputs is less than the equivalent of 1500 picofarads (pF) between the input and AC Line as measured at the input of the unit.

Type 12: Four inputs shall be provided for each channel to permit the monitoring of voltages at the **Green, Yellow, Red,** and **Walk** signal field terminals. The unit shall be designed so that it shall not be necessary to terminate unused **Green, Yellow,** or **Walk** signal sensing inputs when the impedance to AC Line of each of these inputs is less than the equivalent of 1500 picofarads (pF) between the input and AC Line as measured at the input of the unit.

A **Green, Yellow,** or **Walk** signal input shall be sensed when it exceeds 25 volts RMS AC and a signal input shall not be sensed when it is less than 15 volts RMS AC. Signals between 15 and 25 volts RMS AC may or may not be sensed. Both positive and negative half wave rectified signals shall be sensed. The RMS measurement shall be made over a minimum period of at least two cycles.

A **Red/Dont Walk** signal input shall require the presence of 60 ± 10 volts RMS AC at the field terminal to satisfy the requirements of a **Red/Dont Walk** signal indication. Both positive and negative half wave rectified signals shall be sensed. The RMS measurement shall be made over a minimum period of at least two cycles.

A half wave rectified 60 Hz sinusoid of 50 volts peak or more on a **Green, Yellow,** or **Walk** input is equivalent to 25 volts RMS AC or more. A half wave rectified 60 Hz sinusoid of 30 volts peak or less on a **Green, Yellow,** or

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Walk input is equivalent to 15 volts RMS AC or less. A half wave rectified 60 Hz sinusoid of 140 volts peak or more on a **Red/Dont Walk** input is equivalent to 70 volts RMS AC or more. A half wave rectified 60 Hz sinusoid of 100 volts peak or less on a **Red/Dont Walk** input is equivalent to 50 volts RMS AC or less. (Authorized Engineering Information)

When the circuit connected to the sensing input of the unit exhibits high impedance characteristics such as caused by dimmers or burned out lamps, it may be necessary to place a low impedance device external to the unit between the unit input and **AC Neutral**. See section 6.2.4. (Authorized Engineering Information)

All unused **Red/Dont Walk** signal inputs shall be terminated to AC Line. (Authorized Engineering Information)

4.3.3.9 RED ENABLE

The presence of the proper voltage at this terminal enables the MMU to detect the absence of voltage on all field signal inputs of a channel. The absence of the proper voltage inhibits the detection of the absence of voltage on all field signal inputs of a channel. This input shall be considered enabled when the input voltage exceeds 89 volts RMS AC at the **Red Enable** input. This function shall not be considered enabled when the input voltage is less than 70 volts RMS AC at the **Red Enable** input. Signals between 70 and 89 volts RMS AC may or may not enable the detection of the absence of voltage on all field signal inputs of a channel.

The presence of the proper voltage at this terminal also enables Minimum Yellow Change/Red Clearance Interval Monitoring (4.4.5). The absence of the proper voltage at this terminal shall inhibit Minimum Yellow/Red Clearance Interval Monitoring.

4.3.3.10 TYPE SELECT INPUT

The MMU shall operate as a Type 16 with sixteen channels when the **Type Select** input is at logic **True** (low) state, otherwise it shall operate as a Type 12 with twelve channels.

Type 16—Each of the sixteen channels consists of three 120 volt AC inputs: **Green/Walk; Yellow; Red/Dont Walk.**

Type 12—Each of the twelve channels consists of four 120 volt AC inputs: **Green; Yellow; Walk;** and **Red.**

All Port 1 communications activity shall be disabled when the MMU is selected to operate as a Type 12.

4.3.4 Outputs

4.3.4.1 OUTPUT RELAY

The **Output** relay of the MMU shall have two sets of isolated Form C contacts. These relay contacts shall be capable of switching all loads in the range from 2 milliamperes at 18 volts direct current to 3 amperes at 135 volts RMS AC.

The open circuit of the **Output** relay shall be the circuits which are open when the unit is in the "no conflict" state and all voltages are sufficient for proper operation of the CA. The relay coil shall be energized in the "no conflict" state.

4.3.4.2 START-DELAY CONTROL

The MMU shall include a means of detecting an MMU Power Failure (4.4.1). Upon restoration of AC Line following an MMU Power Failure, the **Start-delay** relay shall maintain continuity between its common and open contacts for a period of 2.0 ± 0.5 seconds. Following this 2.0 second period of time, the **Start-delay** relay shall cause continuity to occur between its common and closed contacts.

The **Start-delay** relay shall have a Form C relay output contact. These relay contacts shall be capable of switching all loads in the range from 2 milliamperes at 18 volts direct current to 3 amperes at 135 volts RMS AC.

The operation of the **Start-delay** relay normally results in initiating a start-up sequence within the CU by interrupting the AC Line input to the CU.

4.3.5 Display

The minimum indication shall be as follows:

1. Triggering of the Conflict monitoring portion of the unit.
2. Triggering of the Voltage monitoring portion of the unit.
3. Triggering of the Red monitoring portion of the unit.
4. Triggering of the Minimum Yellow Change/Red Clearance monitoring portion of the unit.
5. Timeout failure on Port 1.
6. Triggering of the microprocessor or memory monitoring portion of the unit.
7. One per channel which indicates the presence of an active **Green**, **Yellow**, or **Walk** field input on that channel during non-fault conditions. The channel indicator display shall latch when the Conflict monitor portion of the unit triggers. The channel indicator display shall show the channels which caused the Red monitoring or Minimum Yellow Change / Red Clearance monitoring portion of the unit to trigger.

The displays specified in 1, 2, 3, 4, 5, 6, and 7 shall not be reset by an MMU Power Failure and shall be retained in their latched state until the unit is reset by the activation of the front panel control or the activation of the **Reset** input. If a voltage monitor fault is non-latching, the display specified in 2 shall indicate the state of the Voltage monitoring portion of the MMU.

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4.3.6 Control and Programming

The MMU shall have a front panel control for manual reset.

Programming the Minimum Flash time, **Minimum Yellow Change** channel disable inputs, **+24 Volt Latch** input, and **CVM Latch** input shall be accomplished through the use of soldered wire jumpers on an interchangeable **Programming Card** (Figure 4.3.6-1).

4.3.6.1 MINIMUM FLASH PROGRAMMING

The **Programming Card** shall have four pairs of 1.09 mm (0.043 inch) diameter holes for programming jumpers. One hole of each pair shall be connected to the common pin #32 on rows A and B and C on each connector. The four jumper hole pairs shall be logically labeled for easy identification of the jumper holes in binary weighted fashion. A soldered wire jumper in a jumper hole pair shall add that designated input value to the binary weighted sum plus one.

4.3.6.2 MINIMUM YELLOW CHANGE CHANNEL DISABLE PROGRAMMING

The **Programming Card** shall have 16 pairs of 1.09 mm (0.043 inch) diameter holes for programming jumpers. One hole of each pair shall be connected to the common pin #32 on rows A and B and C on each connector. The 16 jumper hole pairs shall be logically labeled for easy identification of the channel numbers. A soldered wire jumper in a jumper hole pair shall disable Minimum Yellow Change monitoring for that channel.

4.3.6.3 VOLTAGE MONITOR LATCH PROGRAMMING

The **Programming Card** shall have two pairs of 1.09 mm (0.043 inch) diameter holes for programming jumpers. One hole of each pair shall be connected to the common pin #32 on rows A and B and C on each connector. The two jumper hole pairs shall be logically labeled for easy identification of the **+24 Volt Latch** input and **CVM Latch** input. A soldered wire jumper in a jumper hole pair shall cause these fault conditions to be latched.

4.3.7 Compatibility Programming

The MMU is fully programmable and shall require programming action to provide compatibility between channels.

Programming is accomplished through the use of soldered wire jumpers on an interchangeable **Programming Card** (Figure 4.3.6-1). The interchangeable **Programming Card** may be used with an MMU operating in either Type 16 or Type 12 mode.

The **Programming Card** shall plug into the MMU through a slot in the front panel. The MMU shall provide card guides to ease the insertion of the **Programming Card**. The **Programming Card** shall be provided with card ejectors, Stanford Applied Engineering part number 6100 or equivalent, to ease the removal of the **Programming Card**.

The edge of the **Programming Card** shall be flush with the surface of the front panel when it is properly seated in the program card slot of the MMU.

The **Programming Card** shall meet the requirements for all printed circuit boards described in Section 3.2.3. The **Programming Card** shall be provided with two male connectors with the following requirements:

1. Each connector having 96 positions in a 3-row contact arrangement with 32 contacts per row on a 2.54 millimeter (0.1 inch) contact grid.
2. Each connector shall conform to DIN 41612, series C.
3. Each connector shall be positioned with pin 1 located at the top.

The **Programming Card** shall have 120 pairs of 1.09 mm (0.043 inch) diameter holes for programming jumpers. One hole of each pair shall be connected to the common pin #32 on rows A, B, and C on each connector. The 120 jumper hole pairs shall be logically labeled for easy identification of the jumper holes by channel pairs. A soldered wire jumper in a jumper hole pair shall define a pair of channels as permissive or compatible.

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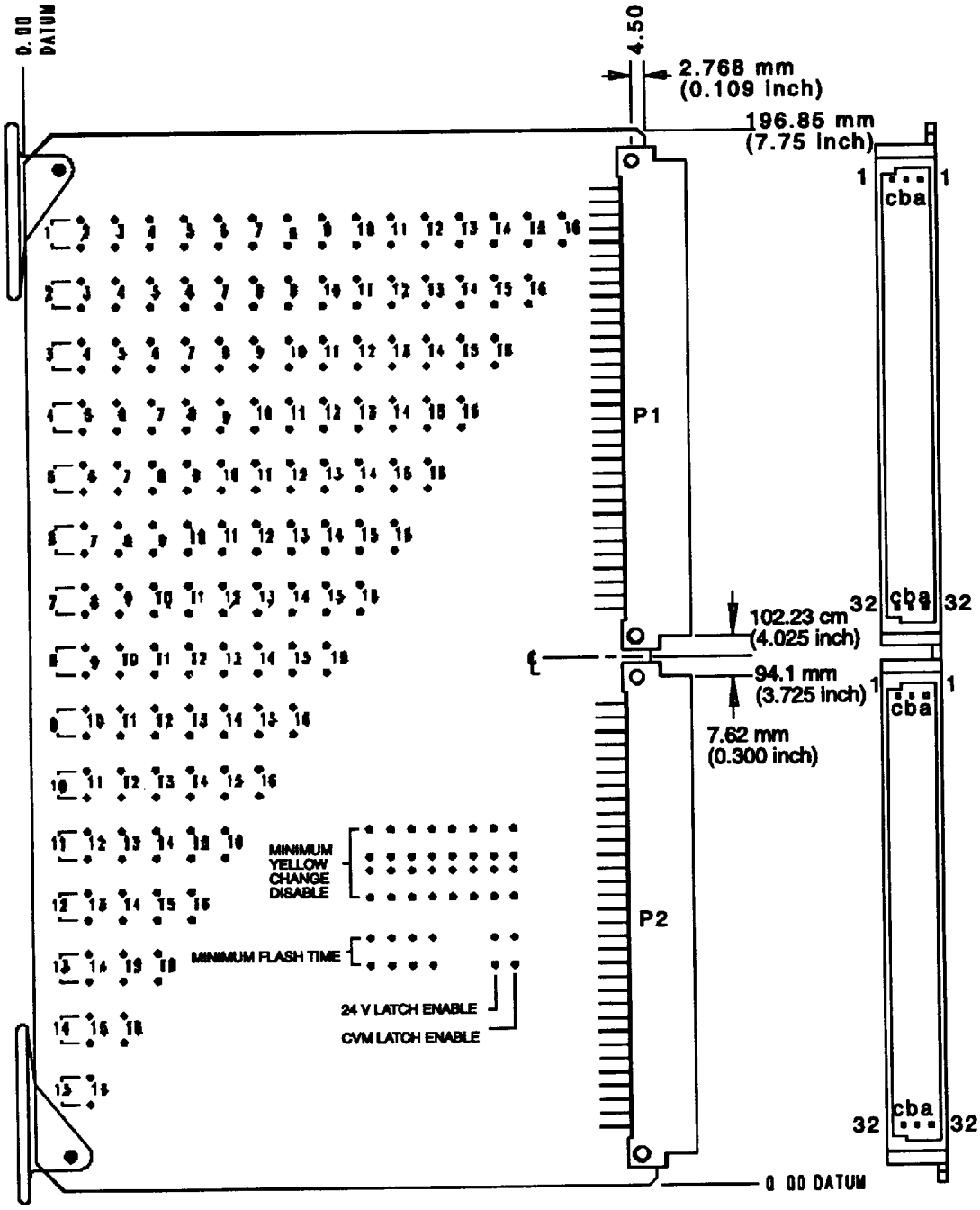

Figure 4.3.6-1
PROGRAMMING CARD

NOTES: 1. All dimensions are in metric.
2. Tolerances: x.xx = ± 0.0254 cm; x.xxx = ± 0.0127 cm
3. Printed Circuit Board thickness: 1.60 mm

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4.3.7.1 CONNECTOR P1 PROGRAMMING CARD PIN CONNECTIONS

Connector P1 Row A

Pin #	Channel Pair
1	1-2
2	1-5
3	1-8
4	1-11
5	1-14
6	2-3
7	2-6
8	2-9
9	2-12
10	2-15
11	3-5
12	3-8
13	3-11
14	3-14
15	4-5
16	4-8
17	4-11
18	4-14
19	5-6
20	5-9
21	5-12
22	5-15
23	6-8
24	6-11
25	6-14
26	7-8
27	7-11
28	7-14
29	8-9
30	8-12
31	8-15
32	Common

Connector P1 Row B

Pin #	Channel Pair
1	1-3
2	1-6
3	1-9
4	1-12
5	1-15
6	2-4
7	2-7
8	2-10
9	2-13
10	2-16
11	3-6
12	3-9
13	3-12
14	3-15
15	4-6
16	4-9
17	4-12
18	4-15
19	5-7
20	5-10
21	5-13
22	5-16
23	6-9
24	6-12
25	6-15
26	7-9
27	7-12
28	7-15
29	8-10
30	8-13
31	8-16
32	Common

Connector P1 Row C

Pin #	Channel Pair
1	1-4
2	1-7
3	1-10
4	1-13
5	1-16
6	2-5
7	2-8
8	2-11
9	2-14
10	3-4
11	3-7
12	3-10
13	3-13
14	3-16
15	4-7
16	4-10
17	4-13
18	4-16
19	5-8
20	5-11
21	5-14
22	6-7
23	6-10
24	6-13
25	6-16
26	7-10
27	7-13
28	7-16
29	8-11
30	8-14
31	9-10
32	Common

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4.3.7.2 CONNECTOR P2 PROGRAMMING CARD PIN CONNECTIONS

Connector P2 Row A

Pin #	Channel Pair
1	9-11
2	9-14
3	10-11
4	10-14
5	11-12
6	11-15
7	12-14
8	13-14
9	14-15

Connector P2 Row B

Pin #	Channel Pair
1	9-12
2	9-15
3	10-12
4	10-15
5	11-13
6	11-16
7	12-15
8	13-15
9	14-16

Connector P2 Row C

Pin #	Channel Pair
1	9-13
2	9-16
3	10-13
4	10-16
5	11-14
6	12-13
7	12-16
8	13-16
9	15-16

Connector P2 Row A

Pin #	Function
10	MYCD-1
11	MYCD-4
12	MYCD-7
13	MYCD-10
14	MYCD-13
15	MYCD-16
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Minimum Flash b8
22	Minimum Flash b1
23	Reserved
24	Reserved
25	Reserved

Connector P2 Row A

Pin #	Function
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved
32	Common

Connector P2 Row B

Pin #	Function
10	MYCD-2
11	MYCD-5
12	MYCD-8
13	MYCD-11
14	MYCD-14
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Minimum Flash b4
22	24V Latch Enable
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved
30	Reserved
31	Reserved
32	Common

Connector P2 Row C

Pin #	Function
10	MYCD-3
11	MYCD-6
12	MYCD-9
13	MYCD-12
14	MYCD-15
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Minimum Flash b2
22	CVM Latch Enable
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved

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Pin #	Function
28	Reserved
29	Reserved
30	Reserved
31	Reserved
32	Common

Notes:
MYCD-n refers to Minimum Yellow Change Disable input for channel n

4.4 FUNCTIONS

4.4.1 MMU Power Failure

The MMU shall respond to a **Power Failure** by entering into a non-latching flash state. The MMU shall respond to a **Power Failure** whether it is the result of overcurrent protection device operation, failure of the MMU power supply, or absence of proper operating AC Line as defined below.

A proper operating AC Line input shall be considered to be **On** if the voltage level is greater than 98 volts RMS AC and it shall be considered to be **Off** if the voltage level is less than 89 volts RMS AC. The hysteresis from the **Off** state to the **On** state or vice versa shall be at least 3 volts RMS AC.

The MMU shall respond to a **Power Failure** as follows:

1. If the AC Line input is **Off** for 450 milliseconds or less, the MMU shall continue to operate as though the AC Line had remained **On**. The **Output Relay** contacts shall not transfer to the fault condition during this interval. The **Start-Delay** relay contacts shall maintain continuity between its common and closed contacts.
2. If the AC Line input is **Off** for 500 milliseconds or more, the MMU shall transfer the **Output** relay contacts to the fault condition. The **Start-Delay** relay contacts shall cause continuity to occur between its common and open contacts. The time interval from the start of the AC Line input being **Off** and the transfer of both relays to these states shall not exceed 525 milliseconds. Both relays shall maintain these states for the duration of the **Power Failure.**
3. If the AC Line input is **Off** for more than 450 milliseconds and less than 500 milliseconds, the MMU shall either continue to operate (4.4.1 (1)) or shall cause a non-latching flash state (4.4.1 (2)).

4.4.2 Minimum Flashing Indication

The MMU shall include a means of detecting an MMU **Power Failure** (4.4.1). The detection of an MMU **Power Failure** shall transfer the **Output** relay contacts to the fault condition. The state of the **Output** relay contacts shall be maintained for a timed interval following restoration of power to the AC Line input. This timed interval shall be the Minimum Flash time. The duration of the Minimum Flash time shall be adjustable between the limits of 6 seconds and 16 seconds and with a maximum incremental adjustment of 1 second.

All MMU initiated flash conditions will last for the programmed Minimum Flash time unless terminated by the front panel reset or **Reset** input command.

4.4.3 Conflict Monitoring

When voltages on any conflicting channels are detected as concurrently active for less than 200 milliseconds, the MMU shall not transfer the **Output** relay contacts to the fault condition. When voltages on any conflicting channels are detected as concurrently active for 450 milliseconds or more, the MMU shall transfer the **Output** relay contacts to the fault condition. When voltages on any conflicting channels are detected as concurrently active for more than 200 milliseconds but less than 450 milliseconds, the MMU may or may not transfer the **Output** relay contacts to the fault condition. The time interval between the beginning of the concurrently conflicting channels and the transfer of the **Output** relay contacts to the fault condition shall not exceed 450 milliseconds. A status bit shall be set in the Type 129 Response frame (Section 3.3.1.4) and transmitted to the CU through Port 1.

When the MMU transfers the **Output** relay contacts to the fault condition it shall cause continuity between the open (see Section 4.3.2.2) and common contacts of the **Output** relay. These contacts shall remain in this fault condition until the unit is reset by the activation of a front panel control or the activation of the **Reset** input.

An MMU **Power Failure** shall not reset the MMU when it has been triggered by a conflict prior to the MMU **Power Failure**.

4.4.4 Red Monitoring

The MMU shall be capable of monitoring for the absence of voltage on all of the inputs of a channel. When an absence of all signal voltage to a channel is detected for less than 700 milliseconds, the MMU shall not transfer the **Output** relay contacts to the fault condition. When an absence of all signal voltage to a channel is detected for 1000 milliseconds or more, the MMU shall transfer the **Output** relay contacts to the fault condition. When an absence of all signal voltage to a channel is detected for more than 700 milliseconds but less than 1000 milliseconds, the MMU may or may not transfer the **Output** relay contacts to the fault condition. The time interval between the beginning of the absence of signal voltage on a channel and the transfer of the **Output** relay contacts to the fault condition shall not exceed 1000 milliseconds. A status bit shall be set in the Type 129 Response frame (Section 3.3.1.4) and transmitted to the CU through Port 1.

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Red Monitoring shall be disabled when the **Red Enable** input is not active or if the **Load Switch Flash** bit is set to "1" in the Type 0 command frame from the CU.

When the MMU transfers the **Output** relay contacts to the fault condition it shall cause continuity between the open (see Section 4.3.2.2) and common contacts of the **Output** relay. These contacts shall remain in this fault condition until the unit is reset by the activation of a front panel control or the activation of the **Reset** input.

An MMU **Power Failure** shall not reset the MMU when it has been triggered by detection of absence of signal voltage on a channel prior to the MMU **Power Failure**.

4.4.5 Minimum Yellow Change / Red Clearance Interval Monitoring

4.4.5.1 YELLOW PLUS RED INTERVAL

The MMU shall verify that the Yellow Change plus Red Clearance interval between the end of an active **Green** signal and the beginning of the next conflicting **Green** signal is at least 2.7 ± 0.1 seconds. When the minimum Yellow Change plus Red Clearance interval is not satisfied, the MMU shall transfer the **Output** relay contacts to the fault condition. A status bit shall be set in the Type 129 Response frame (Section 3.3.1.4) and transmitted to the CU through Port 1.

4.4.5.2 YELLOW CHANGE INTERVAL

The MMU shall verify that the Yellow Change interval is at least 2.7 ± 0.1 seconds. The Yellow Change interval consists of the duration of time in which the yellow field terminal input is active. When the minimum Yellow Change interval is not satisfied, the MMU shall transfer the **Output** relay contacts to the fault condition. A programming means shall be provided on the programming card to disable Minimum Yellow Change interval monitoring on a per channel basis.

Minimum Yellow Change/Red Clearance Interval (4.4.5.1 and 4.4.5.2) monitoring shall be disabled when the **Red Enable** input is not active or if the **Load Switch Flash** bit is set to "1" in the Type 0 command frame from the CU.

When the MMU transfers the **Output** relay contacts to the fault condition it shall cause continuity between the open (see Section 4.3.2.2) and common contacts of the **Output** relay. These contacts shall remain in this fault condition until the unit is reset by the activation of a front panel control or the activation of the **Reset** input.

An MMU **Power Failure** shall not reset the MMU when it has been triggered by detection of fault prior to the MMU **Power Failure**.

4.4.6 Port 1 Timeout

The MMU will transfer the **Output** relay contacts to the fault condition if it does not receive a Type 0 command frame (see Section 3.3.1.4) from the CU for 300 milliseconds. These contacts shall remain in this state until the unit is reset by the activation of the front panel control or the activation of the **Reset** input. A status bit shall be set in the Type 129 Response frame (TS2 Section 3.3.1.4) and transmitted to the CU through Port 1.

A Port 1 Timeout failure during the programmed Minimum Flash time or during an MMU **Power Failure** shall not cause a latched fault condition. The Port 1 Timeout function shall be disabled if the **Port 1 Disable** input is at a **True** (low) state or the MMU is selected to operate as a Type 12. (See 4.3.3.10.)

4.4.7 Voltage Monitoring

The MMU shall include the capability of monitoring two +24 volt direct current sources applied to its **+24 Volt Monitor** inputs. Absence of the proper voltage level at either of the inputs shall cause the unit to transfer the **Output** relay contacts to the fault condition. Restoration of all proper voltage levels shall reset the **Voltage Monitoring** portion of the MMU. A +24 volt DC failure during the programmed Minimum Flash time or during an MMU **Power Failure** shall not cause a fault condition.

A programming means shall be provided on the programming card to cause +24 volt failures to latch in the fault condition until the unit is reset by the activation of the front panel control or the activation of the **Reset** input. A latched +24 volt DC failure shall not be reset by an MMU **Power Failure**.

4.4.7.1 +24 VOLT DIRECT CURRENT SUPPLY MONITOR

A voltage greater than +22 volts DC applied to both of the **+24 Volt Monitor** inputs shall be recognized by the MMU as adequate for proper operation of the CA. A voltage less than +18 volts DC applied to either of the **+24 Volt Monitor** inputs shall be recognized by the MMU as inadequate for proper operation of the CA. Voltages between +22 volts DC and +18 volts DC may or may not be considered inadequate for proper operation of the CA.

When a **+24 Volt Monitor** input is detected as inadequate for less than 125 milliseconds, the MMU shall not transfer the **Output** relay contacts to the fault condition. When a **+24 Volt Monitor** input is detected as inadequate for more than 175 milliseconds, the MMU shall transfer the **Output** relay contacts to the fault condition. When a **+24 Volt Monitor** input is detected as inadequate for more than 125 milliseconds but less than 175 milliseconds, the MMU may or may not transfer the **Output** relay contacts to the fault condition. The time interval between the beginning of the inadequate voltage level and the transfer of

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the **Output** relay contacts to the fault condition shall not exceed 450 milliseconds. A status bit shall be set in the Type 129 Response frame (Section 3.3.1.4) and transmitted to the CU through Port 1.

If only one +24 volt direct current supply is monitored, the two **+24 Volt Monitor** inputs should be jumpered and connected to that +24 volt direct current supply. Over the voltage range of 0 to +30 volts direct current the maximum current "in" or "out" of the **+24 Volt Monitor Input** terminals shall be less than 10 milliamperes. The input impedance of these terminals shall not exceed 11K ohms to **Logic Ground**. The surge impedance shall not be less than 100 ohms.

4.4.7.2 +24 VOLT MONITOR INHIBIT INPUT

Application of a **TRUE** (low) state to this input shall inhibit the operation of the +24 Volt Monitor.

4.4.8 Controller Voltage/Fault Monitor Input

The MMU shall include an input from the CU (**Controller Unit Voltage Monitor (CVM) or Fault Monitor** output). When a **TRUE** (low) state is absent for less than 125 milliseconds, the MMU shall not transfer the **Output** relay contacts to the fault condition. When a **TRUE** (low) state is absent for more than 175 milliseconds, the MMU shall transfer the **Output** relay contacts to the fault condition. When a **TRUE** (low) state is absent for more than 125 milliseconds but less than 175 milliseconds, the MMU may or may not transfer the **Output** relay contacts to the fault condition. The time interval between the beginning of the absence of a **TRUE** (low) state and the transfer of the **Output** relay contacts to the fault condition shall not exceed 450 milliseconds. A status bit shall be set in the Type 129 Response frame (Section 3.3.1.4) and transmitted to the CU through Port 1. A CVM failure during the programmed Minimum Flash time or during an MMU **Power Failure** shall not cause a fault condition.

A programming means shall be provided on the programming card to cause CVM failures to latch in the fault condition until the unit is reset by the activation of the front panel control or the activation of the **Reset** input. A latched CVM failure shall not be reset by an MMU **Power Failure**.

4.4.9 Reset

Activation of the front panel control for manual reset or the **Reset** input shall cause the two Form C **Output** relay contacts to transfer to the no-fault condition. The MMU shall remain in the no-fault condition only if there are no existing faults and all input voltages are at proper operating levels.

Each activation of the front panel control for manual reset or the **Reset** input shall cause a one time reset input to the MMU. A continuously activated front panel manual reset or **Reset** input shall not prevent the MMU from monitoring any fault conditions and/or transferring the **Output** relay contacts to the fault condition. The front panel manual reset or **Reset** input must be removed and reapplied to activate a new reset input to the MMU.

The only intended purpose for the **Reset** input is to facilitate bench testing of the MMU. (Authorized Engineering Information)

4.5 DIAGNOSTICS

The MMU shall be provided with a resident series of self-check diagnostic capabilities.

4.5.1 Memory

The MMU shall contain provisions to verify all memory elements on power up. When a fault is detected, the **Output** relay contacts shall remain in the fault condition. Failure of any of these diagnostics may result in a status bit being set in the Type 129 Response frame (Section 3.3.1.4) and transmitted to the CU through Port 1.

As a minimum, the following memory diagnostics shall be performed:

1. RAM Diagnostic—This test shall verify that all RAM elements are operating correctly. Patterns shall be written to RAM. Each Write shall be followed by a Read to verify that it contains the pattern.
2. ROM Diagnostic—This test shall verify that the Operating System ROM(s) contain the proper program. The routine shall perform a check on each ROM and make a comparison with a preprogrammed value.
3. Non-Volatile Memory Diagnostic—This test shall verify whether the Non-Volatile Memory contains valid data and that the data has not changed since the last write. The routine shall perform a check on each Non-Volatile Memory Element and make a comparison with a preprogrammed value.

The MMU shall continue to verify ROM and Non-Volatile Memory during normal operation at a minimum rate of 1024 bytes per second. When a fault is detected, the unit shall transfer the Output relay contacts to the fault condition.

4.5.2 Microprocessor Monitor

The MMU shall monitor the operation of its microprocessor. As a minimum, the monitoring circuit shall receive signals or logic state transitions at least once every 50 milliseconds from the microprocessor. When the signal or logic state transition is not received for 200 milliseconds, maximum, the monitor circuit shall transfer the **Output** relay to the fault condition.

4.6 MALFUNCTION MANAGEMENT UNIT TESTS

The MMU shall perform its specified functions under the conditions set forth in Section 2, Environmental Re-

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quirements. Clause 4.6 defines the test procedures required to demonstrate the conformance of an MMU with the provisions of the standards.

In the interest of ensuring safe and reliable operation of the MMU covered by these standards, the stress levels which the tests encompass are nominal "Worst Case" conditions the units may experience in operation. These tests are intended for type acceptance testing and not production testing. (Authorized Engineering Information)

4.6.1 Test Facilities

1. A variable AC voltage source capable of providing AC test voltages from 0 to 135 volts RMS AC, 5 amperes minimum capacity.
2. Test probe or test fixture to provide a means of applying the test voltage specified in item #1 to selected field terminal inputs of the MMU.
3. A true RMS responding voltmeter to provide means of detecting a test voltage of 0 to 150 volts RMS AC. The voltmeter shall display actual RMS voltages without additional computation required. The true RMS meter shall measure a 60 Hz half wave sinusoidal signal with a peak voltage of 50 volts as 25 volts RMS.
4. A digital time indicator with sufficient scale to cover the range and resolution of timings to be taken and with a readout capability of at least 0.01 seconds.
5. Milliamp meter.
6. A variable direct current voltage source capable of providing 0.5 amperes from 0 to 30 VDC.
7. Test probe or test fixture to provide a means of applying the test voltage in item #6 to selected inputs (see 4.3.3.5 and 4.3.3.6) of the MMU.
8. A transient generator capable of supplying the transients outlined in 2.1.6 through 2.1.8.
9. Test fixture capable of providing Port 1 communications with the MMU as outlined in 3.3.1 (Port 1 Physical and Protocol).

4.6.2 Standard Setup

Unless otherwise specified the MMU shall be set up as follows:

1. No fault state at the beginning of each test.
2. All **Green, Yellow,** and **Walk** inputs shall be zero volts.
3. All **Red** inputs shall be connected to AC Line.
4. **Red Enable** shall be zero volts AC.
5. The two **+24 Volt Monitor** inputs shall be connected to 24 volts DC.
6. **+24 Volt Monitor Inhibit** input and **CVM** input shall be zero volts DC.
7. MMU set up for non-latching voltage monitoring faults.
8. Program card programmed for no compatible channels.
9. MMU set up to operate as a type 12, without Port 1 communications.

Where AC Line is specified it is meant to mean any voltage from 89 volts RMS AC to 135 volts RMS AC.

4.6.3 Ground Isolation Test

Measure resistance between **AC Neutral** and **Logic Ground** to verify that it exceeds 10 megohms.

4.6.4 1500 pF Input Test

With AC Line applied to any **Green, Yellow,** or **Walk** input apply 135 volts RMS AC through a 1500 pF capacitor to each of the other **Green, Yellow,** and **Walk** inputs one at a time for 1 second. Verify that no conflicts are recognized. Repeat test with AC Line applied to a different **Green, Yellow,** or **Walk** input and verify that the input used for the first part of the test also does not cause a conflict to a 135 volts RMS AC signal applied through 1500 pF.

4.6.5 Conflict Low Voltage Test

4.6.5.1 Apply AC Line to one conflicting input and apply 15 volts RMS AC full wave signal to all other **Green, Yellow,** and **Walk** inputs for one second. Verify that no conflict is recognized within that interval. Repeat with AC Line on a different channel.

4.6.5.2 Same as 4.6.5.1 with 15 volts RMS AC (30 V peak 60 Hz) positive half wave signal.

4.6.5.3 Same as 4.6.5.1 with 15 volts RMS AC (30 V peak 60 Hz) negative half wave signal.

4.6.6 Conflict High Voltage Test

4.6.6.1 Apply AC Line to one conflicting input and apply 25 volts RMS AC full wave signal to each of the other **Green, Yellow,** or **Walk** inputs. Verify that a conflict is recognized and the **Output** relay contacts transfer to the fault condition within the time parameters specified in section 4.4.3. Repeat with AC Line on a different conflicting input to verify that the first input also responds correctly to 25 volts RMS AC input.

4.6.6.2 Same as 4.6.6.1 with 25 volts RMS AC (50 V peak 60 Hz) positive half wave signal.

4.6.6.3 Same as 4.6.6.1 with 25 volts RMS AC (50 V peak 60 Hz) negative half wave signal.

4.6.6.4 With the MMU in a Conflict fault state, verify that the MMU remains in the Conflict fault state after the removal of the conflicting signals. Remove AC power

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from the MMU, allow enough time for the internal power supplies to "bleed" down to 0 VDC before restoring AC power to the MMU. Verify that the AC power interruption does not cause reset of the fault or alter any fault data display indications.

4.6.7 Red Input Test

4.6.7.1 Apply 89 volts RMS AC to the **Red Enable** input. With all other **Red** inputs at AC Line, apply 50 volts RMS AC to each **Red** input and verify that a Red Failure is recognized and the **Output** relay contacts transfer to the fault condition within the time parameters specified in Section 4.4.4.

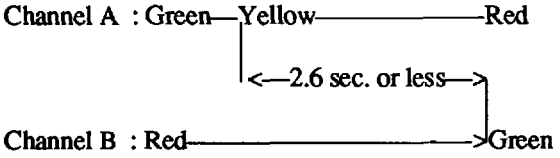
4.6.7.2 With the MMU in the Red Failure state, verify that the MMU remains in the Red Failure state after the removal of the Red Failure. Remove AC power from the MMU, allow enough time for the internal power supplies to "bleed" down to 0 VDC before restoring AC power to the MMU. Verify that the AC power interruption does not cause reset of the fault or alter any fault data display indications.

4.6.7.3 Apply 89 volts RMS AC to the **Red Enable** input. Apply 70 volts RMS AC to all **Red** inputs for at least 2 seconds and verify that no faults are recognized within that interval.

4.6.7.4 With **Red Enable** input at 70 volts RMS AC and **Red** inputs at zero volts for at least 2 seconds, verify that no faults are recognized within that interval.

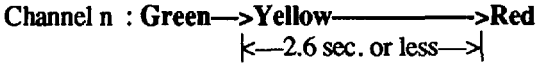
4.6.8 Minimum Yellow Change/Red Clearance Interval

4.6.8.1 With **Red Enable** signal connected to AC Line, apply the following sequence to any conflicting channels:



Verify that the MMU recognizes that a 2.6 second or less clearance time **(Yellow + Red)** as a Minimum Yellow Change / Red Clearance failure. Verify that all other pairs of conflicting channels respond correctly to a Minimum Yellow Change / Red Clearance failure.

4.6.8.2 With **Red Enable** signal connected to AC Line, apply the following sequence to any channel enabled to monitor minimum Yellow Change interval:



Verify that a 2.6 second or less Yellow Change interval is detected as a Minimum Yellow Change / Red Clearance failure.

4.6.8.3 With the MMU in the Minimum Yellow Change/Red Clearance fault state, remove AC power from the MMU, allow enough time for the internal power supplies to "bleed" down to 0 VDC before restoring AC power to the MMU. Verify that the AC power interruption does not cause reset of the fault or alter any fault data display indications.

4.6.9 Port 1 Timeout

With the MMU setup with Port 1 communications and the **Type Select** input set **True** (low), verify that the **Output** relay contacts transfer to the fault condition after 300 milliseconds but before 400 milliseconds if a Type 0 frame is not received within this interval. Verify that no timeout occurs if the **Port 1 Disable** input is a **True** (low) state.

4.6.10 DC Voltage Monitoring

For tests 4.6.10.1 to 4.6.10.6 apply 24 VDC to the **+24 Volt Inhibit** input.

4.6.10.1 Apply 22 VDC to both **+24 Volt Monitor** inputs. Verify that the MMU is in the no fault condition.

4.6.10.2 Apply 18 VDC to each **+24 Volt Monitor** input with the other input at 22 volts. Verify that applying the 18 VDC to either input is recognized as a +24 Volt Failure and the Output relay contacts transfer to the fault condition within the time parameter specified in Section 4.4.7.1. Verify that reapplying 22 VDC to the input(s) being tested restores the MMU to the no fault condition.

4.6.10.3 With the MMU in the no fault condition, verify that applying 16 VDC to the **Controller Voltage Monitor (CVM)** input is recognized as a CVM failure and the **Output** relay contacts transfer within the time parameter specified in Section 4.4.8. Verify that applying 8 VDC to the CVM input restores the MMU to the no fault condition.

For tests 4.6.10.4 to 4.6.10.5 enable latching 24 volt failures.

4.6.10.4 Apply 18 VDC to either **+24 Volt Monitor** input and verify that a +24 Volt Failure is recognized and the **Output** relay contacts transfer within the time parameter specified in section 4.4.7.1. Verify that reapplying 22 VDC to the input(s) being tested does not restore the MMU to the no fault condition or line feed alter the fault data display indications.

4.6.10.5 With the MMU in the latched +24 Volt failure state, remove AC power from the MMU, allow enough time for the internal power supplies to "bleed" down to 0

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VDC before restoring AC power to the MMU. Verify that the AC power interruption does not cause reset of the fault or alter any fault data display indications.

For tests 4.6.10.6 to 4.6.10.7 enable latching CVM failures.

4.6.10.6 Apply 16 VDC to the **Controller Voltage Monitor (CVM)** input and verify that a CVM failure is recognized and the **Output** relay contacts transfer within the time parameter specified in Section 4.4.8. Verify that reapplying 8 VDC to the **CVM** input does not restore the MMU to the no-fault condition or alter the fault data display indications.

4.6.10.7 With the MMU in the latched CVM failure state, remove AC power from the MMU, allow enough time for the internal power supplies to "bleed" down to 0 VDC before restoring AC power to the MMU. Verify that the AC power interruption does not cause reset of the fault or alter any fault data display indications.

4.6.10.8 Over the voltage range of 0 to +30 volts DC, verify that the maximum current into or out of the **+24 Volt Monitor** inputs is less than 10 milliamps.

4.6.11 MMU Power Failure

4.6.11.1 Remove AC power for 450 milliseconds and verify that both the **Start-Delay** and **Output** relays remain in the no fault condition for at least 100 milliseconds beyond the end of this interval.

4.6.11.2 Remove AC power for 500 milliseconds and verify that the MMU recognizes the 500 millisecond MMU **Power Failure**. Verify that both the **Start-Delay** and Fault **Output** relays transfer to the fault condition within 525 milliseconds following the start of the power failure interval. Verify that the MMU executes a Start-Delay and Minimum Flash time power-up sequence as specified in Sections 4.3.4.2 and 4.4.2 upon restoration of AC power.

4.6.11.3 Slowly lower the AC Line input voltage level until the MMU recognizes an MMU **Power Failure**. Slowly raise the AC Line input voltage level until the MMU recognizes power restoration. Verify that the **Off** voltage level occurs above 89 volts RMS AC and that the **On** voltage level occurs below 98 volts RMS AC. Also verify that the hysteresis from **Off** to **On**, or **On** to **Off** is at least 3 volts.

4.6.12 Permissive Programming

With a program card programmed for all channels to be permissive, apply AC Line to all channels. Verify that no conflicts are recognized.

4.6.13 Continuous Reset

Create a conflict on at least two channels. Activate the front panel manual reset or **Reset** input. While the reset input is maintained, verify that the **Output** relay contacts transfer to the no fault condition and that a Conflict failure is again recognized.

4.6.14 Transient Tests

The MMU shall maintain all defined functions while the independent test pulse levels specified in Sections 2.1.6.1 and 2.1.6.2 are applied to the AC field inputs and AC Line input of the MMU.

The MMU shall be capable of withstanding a high energy transient specified in Section 2.1.8 applied to the AC field inputs and AC Line input (no other power connected to these inputs) of the MMU without failure of the unit under test. The MMU shall perform all defined functions upon application of power to the AC Line input of the MMU.

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SECTION 5
TERMINALS AND FACILITIES

These standards define the minimum requirements for terminals and facilities within the cabinet. Specific construction and performance standards are established for the purpose of achieving greater utility and safety.

These standards define the performance and construction requirements of cabinet terminals and facilities that are considered to be of the attached or nonplug-in type. The emphasis is placed upon electrical requirements, cabling, supporting terminal facilities, and labeling.

Any tests or procedures referenced in this section of the standards publication are intended to facilitate type testing of equipment designs and are not intended to be performed on all production units.

5.1 DEFINITIONS

5.1.1 Cabinet

An outdoor enclosure designed for base, pedestal or pole mounting providing protection, support, ventilation and security for the enclosed facilities and equipment.

5.1.2 Flash Bus

A flash bus is an **AC line** feed supplying flashing power to the flash-transfer device(s) from an output of a flasher.

5.1.3 Earth Ground

An electrical connection between a circuit or piece of equipment and the earth.

5.1.4 Logic Ground

Voltage reference point and current return for DC logic circuits.

5.1.5 Primary Feed

The primary feed is the 120 VAC single phase input to the cabinet from the local power distribution system. The primary feed includes the neutral conductor.

5.1.6 Signal Bus

The signal bus is the **AC line** feed supplying power to the signal load switches from the output of the signal bus relay.

5.1.7 Terminal(s)

A terminal is an electrically conductive member serving as a junction to electrically connect two or more conductors and to also provide a means to individually connect or disconnect conductors. No more than three conductors are permitted to be connected to a terminal.

5.2 PHYSICAL

5.2.1 Material

All ferrous metal parts shall be protected against corrosion. All materials shall be moisture and fungus resistant.

5.2.2 Terminal Identification

Each electrical terminal within the facilities shall be uniquely identified and shall be referenced by the cabinet wiring diagram.

Terminal(s) nomenclature shall be adjacent to the terminal(s). The nomenclature for terminals accessible from the front of a panel shall be visible from the front of the panel. Nomenclature shall be permanent and legible.

5.2.3 Component Identification

All load switches, relays, flasher(s), circuit breakers, fuses, and switches within the facilities shall be uniquely identified, and shall be referenced on the cabinet diagram. Component nomenclature on nonplug-in devices shall be on or adjacent to the component. Component nomenclature for plug-in devices shall be adjacent to the receptacle for the device. Nomenclature shall be permanent and legible.

5.2.4 Printed Circuits

Printed circuits shall meet the requirements of Section 3.2.3.

Each AC circuit shall have sufficient current carrying capacity to enable the device protecting the circuit to trip in a direct short circuit condition before the track is damaged in any manner.

If a plug-in base for a load switch, flasher, or flash relay is connected directly to a printed circuit board, the base shall be rigidly connected to another facility surface so that no mechanical strain is placed on the printed circuit solder connections when the plug-in device is inserted or removed.

Connectors used for BIUs and Detectors attached directly to a printed circuit board shall be secured to the printed circuit board by means other than the solder connections.

5.2.5 Wire

1. All wire used in controller cabinets shall be copper. All wire #14 to 30 AWG shall be stranded. Wires shall be sized per the ampacity ratings of Table 5.2.5-1.

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Table 5.2.5-1
AMPACITY

AWG Wire Size	Ampacity Rating
30–24	0.25
22	2
20	4
18	5
16	10
14	15
12	20
10	30
8	50
6	70

2. Conductors shall conform to military specification MIL-W-16878D, Electrical Insulated High Temperature Wire, type B. Conductors #14 AWG or larger shall be permitted to be UL type THHN.
3. Conductors shall not be spliced between terminations.
4. Cable may be used in lieu of individual conductors to interconnect equipment or panels within the controller cabinet. The cable shall be constructed of #28 AWG or larger conductors. Insulation shall have a voltage rating of 300 volts minimum and shall be rated for use at 105°C. Cables shall be provided with strain relief.

5.2.6 Wiring

All terminals and facilities wiring shall be neatly arranged and made secure by the use of wiring harnesses, cable sheaths, cable wraps, or raceways. All wires in a harness shall be laced or bound together.

Cabling shall be routed to prevent conductors from being in contact with metal edges. Cabling shall be arranged so that any removable assembly may be removed without disturbing conductors not associated with that assembly.

5.2.7 Layout

The terminals and facilities layout shall be arranged in a manner that allow all equipment to be readily accessible.

Terminals and facilities shall be located within the cabinet as follows:

1. Terminals for CU inputs and outputs together with load switch and flasher supports shall be located on the rear portion of the cabinet.
2. Power distribution components as required by Section 5.4.2 shall be located on the lower right portion of the cabinet.
3. Terminals for auxiliary functions and detector loop field terminal connections shall be located on the left portion of the cabinet.
4. Load Switch Field Terminals shall be located on the lower half of the back or side of the cabinet. Terminals shall be mounted not less than 152.4 mm (6.0 inches) from the bottom of the cabinet in ground or foundation mounted cabinets. This distance shall be not less than 76.2 mm (3.0 inches) in cabinets mounted in other configurations. These terminals shall be readily accessible from the front of the cabinet.

All shelf mounted equipment shall be arranged to allow removal and replacement without the removal of adjacent equipment.

5.2.8 Load Switch and Flasher Support

At least one point of support shall be provided to the load switch or flasher within the area designated as the area of required support as shown in Figure 5.2.8-1. The load switch or flasher handle or gripping device shall be readily accessible to allow installation or removal. Flasher and load switch bases shall be mounted so that they are oriented in the manner shown in Figure 5.2.8-2 or 5.2.8-3.

At least 50% of the area above and beneath the load switch or flasher, between 12.7 and 38.1 mm (0.5 and 1.5 inches) either side of the centerline of the device, shall be open to allow for the free flow of air across the load switches or flashers. There shall be no obstruction within 24.4 mm (1.0 inches) above and below the units within the open area.

5.3 INTERFACE

This standard defines TF interfaces for both Type 1 and Type 2 CUs as defined in Section 3.

5.3.1 Type 1 Controller Interface

The Type 1 TF shall utilize a Bus Interface Unit (BIU) conforming to the requirements of Section 8.0 for all controller input/output functions except controller fault monitor output.

5.3.1.1 LOAD SWITCH AND FLASHER POSITIONS

Wired sockets and BIUs shall be provided as a minimum in the quantities listed in Table 5.3.1-1 for the configuration selected.

It shall be possible to flash either the Yellow or Red indication on any load switch output assigned to a vehicle movement and to change from one color indication to the other by use of simple tools without the need to unsolder or resolder connections. All flash change means shall be readily accessible from the cabinet door opening.

5.3.1.2 INPUT/OUTPUT TERMINALS

As a minimum terminals shall be provided for the input/output signals listed in Table 5.3.1-2 for the TF configurations indicated.

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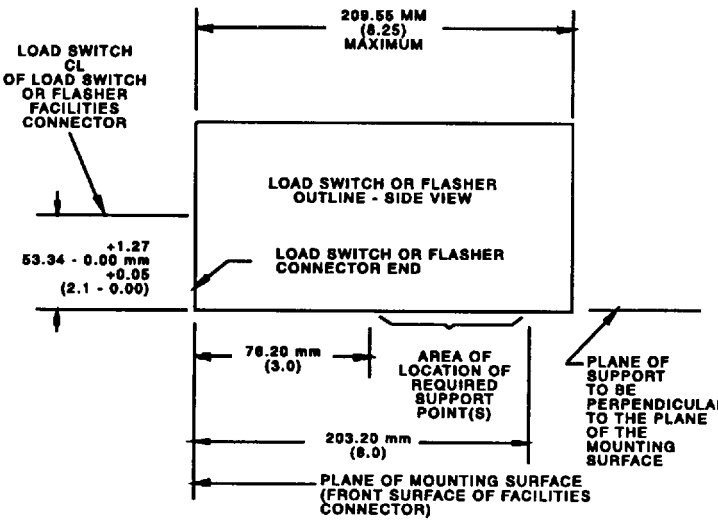
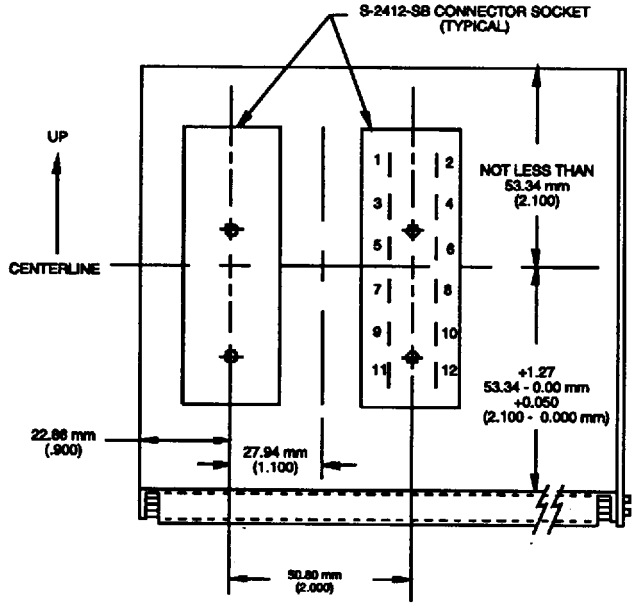


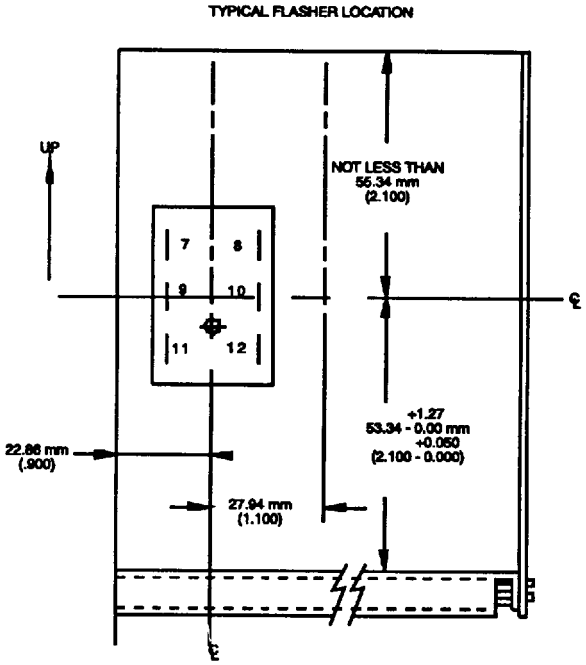
NOTE: All dimensions in parenthesis are in inches

Figure 5.2.8-1
LOAD SWITCH OR FLASHER SUPPORT



NOTE: All dimensions in parenthesis are in inches.

Figure 5.2.8-2
FRONT VIEW-LOAD SWITCH SUPPORT DIMENSIONS



NOTE: All dimension in parenthesis are in inches.

Figure 5.2.8-3
FRONT VIEW-FLASHER SUPPORT DIMENSIONS

5.3.1.3 POWER AND CONTROL TERMINALS

Terminals shall be provided for each of the following functions:

AC Line
AC Neutral
Earth Ground
Controller Power
Power Supply Power
Logic Ground
+12 VDC
+24 VDC
12 VAC
Line Frequency Reference

Table 5.3.1-1
TYPE 1 CONFIGURATIONS

Config	Load Sw. Sockets	Flash Relay Sockets	Flasher Sockets	BIUs Required	Detector Rack Type	MMU Type
1	4	2	1	1	1	16
2	8	4	1	1	1	16
3	12	6	1	2	2	16

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Table 5.3.1-2
INPUT/OUTPUT TERMINALS

	Input Functions	Terminals and Facilities Configurations 1	2	3	4
1.	Stop Time Ring 1	X	X	X	X
2.	Stop Time Ring 2			X	X
3.	Call To Nonactuated I	X	X	X	X
4.	Walk Rest Modifier	X	X	X	X
5.	Manual Control Enable	X	X	X	X
6.	Interval Advance	X	X	X	X
7.	External Minimum Recall	X	X	X	X,
8.	External Start	X	X	X	X
9.	Test Input A	X	X	X	X
10.	Test Input B	X	X	X	X
11.	Preempt 1 Input	X	X	X	X
12.	Preempt 2 Input	X	X	X	X
13.	Preempt 3 Input			X	X
14.	Preempt 4 Input			X	X
15.	Automatic Flash	X	X	X	X
16.	Dimming Enable	X	X	X	X
17.	TBC ON Line	X	X	X	X
	Output Functions				
1.	TBC Aux # 1 Output	X	X	X	X
2.	TBC Aux # 2 Output	X	X	X	X
3.	TBC Aux # 3 Output			X	X
4.	Preempt 1 Output	X	X	X	X
5.	Preempt 2 Output	X	X	X	X
6.	Preempt 3 Output			X	X
7.	Preempt 4 Output			X	X
8.	Fault Monitor	X	X	X	X

5.3.1.4 BIU INTERFACE

5.3.1.4.1 BIU Rack

BIU rack(s) shall be provided to accommodate at a minimum the number of BIU's listed in Table 5.3.1-1 for the configuration selected.

The BIU rack design shall accommodate BIU units as defined in Section 8.0. A dual row 64 pin female DIN 41612 Type B connector shall be provided for each BIU rack position. Card guides shall be provided for both edges of the BIU (reference Figure 8.2-1). Each BIU rack position shall be labeled with the BIU number corresponding to the associated BIU functions. The BIU address pins for each BIU rack position connector shall be connected to correspond to the BIU number as shown in Table 5.3.1-3.

At least 30% of the area above and beneath each BIU shall be open to allow for the free flow of air through the BIU rack. There shall be no obstruction within 25.4 mm (1.0 inches) above and below the BIU rack within the open area.

Table 5.3.1-3
BIU ADDRESS ASSIGNMENT

BIU Number	Function Table	BIU Address Bit 0	Bit 1	Bit 2	Bit 3
1	5.3.1-4	OFF	OFF	OFF	OFF
2	5.3.1-5	ON	OFF	OFF	OFF
3	5.3.1-6	OFF	ON	OFF	OFF
4	5.3.1-7	ON	ON	OFF	OFF
5	Reserved	OFF	OFF	ON	OFF
6	Reserved	ON	OFF	ON	OFF
7	Spare	OFF	ON	ON	OFF
8	Spare	ON	ON	ON	OFF

5.3.1.4.2 BIU Input/Output Functions

The TF BIU address inputs shall control the assignment of input/output functions to the various BIUs as shown in Tables 5.3.1-3 through 5.3.1-7. Signal assignments shown correspond to the requirements of both actuated and pretimed controllers. Signals not required by a pretimed controller shall be considered as reserved.

Table 5.3.1-4
BIU 1 SIGNAL ASSIGNMENT

Signal	Function
Output 1	Load Switch 1 Red Driver
Output 2	Load Switch 1 Yellow Driver
Output 3	Load Switch 1 Green Driver
Output 4	Load Switch 2 Red Driver
Output 5	Load Switch 2 Yellow Driver
Output 6	Load Switch 2 Green Driver
Output 7	Load Switch 3 Red Driver
Output 8	Load Switch 3 Yellow Driver
Output 9	Load Switch 3 Green Driver
Output 10	Load Switch 4 Red Driver
Output 11	Load Switch 4 Yellow Driver
Output 12	Load Switch 4 Green Driver
Output 13	Load Switch 5 Red Driver
Output 14	Load Switch 5 Yellow Driver
Output 15	Load Switch 5 Green Driver
Input/Output 1	Load Switch 6 Red Driver [O]
Input/Output 2	Load Switch 6 Yellow Driver [O]

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Table 5.3.1-4(Continued)
BIU 1 SIGNAL ASSIGNMENT

Signal	Function
Input/Output 3	Load Switch 6 Green Driver [O]
Input/Output 4	Load Switch 7 Red Driver [O]
Input/Output 5	Load Switch 7 Yellow Driver [O]
Input/Output 6	Load Switch 7 Green Driver [O]
Input/Output 7	Load Switch 8 Red Driver [O]
Input/Output 8	Load Switch 8 Yellow Driver [O]
Input/Output 9	Load Switch 8 Green Driver [O]
Input/Output 10	TBC Aux # 1 Output [O]
Input/Output 11	TBC Aux # 2 Output [O]
Input/Output 12	Preempt 1 Output [O]
Input/Output 13	Preempt 2 Output [O]
Input/Output 14	Preempt 1 Input [I]
Input/Output 15	Preempt 2 Input [I]
Input/Output 16	Test Input A [I]
Input/Output 17	Test Input B [I]
Input/Output 18	Automatic Flash [I]
Input/Output 19	Dimming Enable [I]
Input/Output 20	Manual Control Enable [I]
Input/Output 21	Interval Advance [I]
Input/Output 22	External Minimum Recall [I]
Input/Output 23	External Start [I]
Input/Output 24	TBC ON Line [I]
Input 1	Stop Time Ring 1 (Stop Time)
Input 2	Stop Time Ring 2
Input 3	Max II Selection Ring 1
Input 4	Max II Selection Ring 2
Input 5	Force Off Ring 1 (Force Off)
Input 6	Force Off Ring 2
Input 7	Call To Non Act I
Input 8	Walk Rest Modifier
Opto Input 1	Phase 1 Ped Call
Opto Input 2	Phase 2 Ped Call
Opto Input 3	Phase 3 Ped Call
Opto Input 4	Phase 4 Ped Call
Opto Common	12 VAC
Data Transmit	Reserved
Data Receive	Reserved
Address Bit 0	Reference Table 5.3.1-3
Bit 1	
Bit 2	
Bit 3	
+24 VDC	Power Supply Interface
Logic Ground	
Earth Ground	
Line Freq. Ref.	

Reference Section 8.0 for BIU signal pin assignment.
Signals shown in parenthesis ( ) apply only to a pretimed controller.

Table 5.3.1-5
BIU 2 SIGNAL ASSIGNMENT

Signal	Function
Output 1	Load Switch 9 Red Driver
Output 2	Load Switch 9 Yellow Driver
Output 3	Load Switch 9 Green Driver
Output 4	Load Switch 10 Red Driver
Output 5	Load Switch 10 Yellow Driver
Output 6	Load Switch 10 Green Driver
Output 7	Load Switch 11 Red Driver
Output 8	Load Switch 11 Yellow Driver
Output 9	Load Switch 11 Green Driver
Output 10	Load Switch 12 Red Driver
Output 11	Load Switch 12 Yellow Driver
Output 12	Load Switch 12 Green Driver
Output 13	Load Switch 13 Red Driver
Output 14	Load Switch 13 Yellow Driver
Output 15	Load Switch 13 Green Driver
Input/Output 1	Load Switch 14 Red Driver [O]
Input/Output 2	Load Switch 14 Yellow Driver [O]
Input/Output 3	Load Switch 14 Green Driver [O]
Input/Output 4	Load Switch 15 Red Driver [O]
Input/Output 5	Load Switch 15 Yellow Driver [O]
Input/Output 6	Load Switch 15 Green Driver [O]
Input/Output 7	Load Switch 16 Red Driver [O]
Input/Output 8	Load Switch 16 Yellow Driver [O]
Input/Output 9	Load Switch 16 Green Driver [O]
Input/Output 10	TBC Aux # 3 Output[O]
Input/Output 11	Free/Coord Status [O]
Input/Output 12	Preempt 3 Output [O]
Input/Output 13	Preempt 4 Output [O]
Input/Output 14	Preempt 5 Output [O]
Input/Output 15	Preempt 6 Output [O]
Input/Output 16	Preempt 3 Input [I]
Input/Output 17	Preempt 4 Input [I]
Input/Output 18	Preempt 5 Input [I]
Input/Output 19	Preempt 6 Input [I]
Input/Output 20	Call To Nonactuated II [I]
Input/Output 21	Spare
Input/Output 22	Spare
Input/Output 23	Spare
Input/Output 24	Spare
Input 1	Inhibit Max Ring 1
Input 2	Inhibit Max Ring 2
Input 3	Local Flash
Input 4	MMU Flash
Input 5	Alarm 1
Input 6	Alarm 2
Input 7	Free (No Coord)

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Table 5.3.1-5 (Continued)
BIU 2 SIGNAL ASSIGNMENT

Signal	Function
Input 8	Test Input C
Opto Input 1	Phase 5 Ped Call (Signal Plan A)
Opto Input 2	Phase 6 Ped Call (Signal Plan B)
Opto Input 3	Phase 7 Ped Call
Opto Input 4	Phase 8 Ped Call
Opto Common	12 VAC
Data Transmit	Reserved
Data Receive	Reserved
Address Bit 0	Reference Table 5.3.1-3
Bit 1	
Bit 2	
Bit 3	
+24 VDC	Power Supply Interface
Logic Ground	
Earth Ground	
Line Freq. Ref.	

Reference Section 8.0 for BIU signal pin assignment.
Signals shown in parenthesis ( ) apply only to a pretimed controller.

Table 5.3.1-6
BIU 3 SIGNAL ASSIGNMENT

Signal	Function
Output 1	Timing Plan A Output
Output 2	Timing Plan B Output
Output 3	Timing Plan C Output
Output 4	Timing Plan D Output
Output 5	Offset 1 Output
Output 6	Offset 2 Output
Output 7	Offset 3 Output
Output 8	Automatic Flash
Output 9	System Special Func 1
Output 10	System Special Func 2
Output 11	System Special Func 3
Output 12	System Special Func 4
Output 13	Reserved
Output 14	Reserved
Output 15	Reserved
Input/Output 1	Ring 1 Status Bit A [O]
Input/Output 2	Ring 1 Status Bit B [O]
Input/Output 3	Ring 1 Status Bit C [O]
Input/Output 4	Ring 2 Status Bit A [O]
Input/Output 5	Ring 2 Status Bit B [O]
Input/Output 6	Ring 2 Status Bit C [O]
Input/Output 7	Red Rest Ring 1 [I]
Input/Output 8	Red Rest Ring 2 [I]
Input/Output 9	Omit All Red Ring 1 [I]
Input/Output 10	Omit All Red Ring 2 [I]
Input/Output 11	Red Recycle Ring 1 [I]
Input/Output 12	Red Recycle Ring 2 [I]
Input/Output 13	Alternate Sequence A [I]
Input/Output 14	Alternate Sequence B [I]
Input/Output 15	Alternate Sequence C [I]
Input/Output 16	Alternate Sequence D [I]
Input/Output 17	Phase Omit 1 [I]
Input/Output 18	Phase Omit 2 [I]
Input/Output 19	Phase Omit 3 [I]
Input/Output 20	Phase Omit 4 [I]
Input/Output 21	Phase Omit 5 [I]
Input/Output 22	Phase Omit 6 [I]
Input/Output 23	Phase Omit 7 [I]
Input/Output 24	Phase Omit 8 [I]
Input 1	Hold Phase 1
Input 2	Hold Phase 2
Input 3	Hold Phase 3
Input 4	Hold Phase 4
Input 5	Hold Phase 5
Input 6	Hold Phase 6
Input 7	Hold Phase 7
Input 8	Hold Phase 8
Opto Input 1	Timing Plan A Input
Opto Input 2	Timing Plan B Input
Opto Input 3	Timing Plan C Input
Opto Input 4	Timing Plan D Input
Opto Common	Interconnect Common
Data Transmit	Reserved
Data Receive	Reserved
Address Bit 0	Reference Table 5.3.1-3
Bit 1	
Bit 2	
Bit 3	
+24 VDC	Power Supply Interface
Logic Ground	
Earth Ground	
Line Freq. Ref.	

Reference Section 8.0 for BIU signal pin assignment.

Table 5.3.1-7
BIU 4 SIGNAL ASSIGNMENT

Signal	Function
Output 1	Phase 1 On
Output 2	Phase 2 On
Output 3	Phase 3 On
Output 4	Phase 4 On
Output 5	Phase 5 On
Output 6	Phase 6 On
Output 7	Phase 7 On
Output 8	Phase 8 On
Output 9	Phase 1 Next
Output 10	Phase 2 Next

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Table 5.3.1-7 (Continued)
BIU 4 SIGNAL ASSIGNMENT

Signal	Function
Output 11	Phase 3 Next
Output 12	Phase 4 Next
Output 13	Phase 5 Next
Output 14	Phase 6 Next
Output 15	Phase 7 Next
Input/Output 1	Phase 8 Next [O]
Input/Output 2	Phase 1 Check [O]
Input/Output 3	Phase 2 Check [O]
Input/Output 4	Phase 3 Check [O]
Input/Output 5	Phase 4 Check [O]
Input/Output 6	Phase 5 Check [O]
Input/Output 7	Phase 6 Check [O]
Input/Output 8	Phase 7 Check [O]
Input/Output 9	Phase 8 Check [O]
Input/Output 10	Address Bit 0 [I]
Input/Output 11	Address Bit 1 [I]
Input/Output 12	Address Bit 2 [I]
Input/Output 13	Address Bit 3 [I]
Input/Output 14	Address Bit 4 [I]
Input/Output 15	Spare
Input/Output 16	Spare
Input/Output 17	Spare
Input/Output 18	Spare
Input/Output 19	Spare
Input/Output 20	Reserved
Input/Output 21	Reserved
Input/Output 22	Reserved
Input/Output 23	Reserved
Input/Output 24	Reserved
Input 1	Ped Omit 1
Input 2	Ped Omit 2
Input 3	Ped Omit 3
Input 4	Ped Omit 4
Input 5	Ped Omit 5
Input 6	Ped Omit 6
Input 7	Ped Omit 7
Input 8	Ped Omit 8
Opto Input 1	Offset 1 Input
Opto Input 2	Offset 2 Input
Opto Input 3	Offset 3 Input
Opto Input 4	Spare
Opto Common	Interconnect Common
Data Transmit	Reserved
Data Receive	Reserved
Address Bit 0	Reference Table 5.3.1-3
Bit 1	
Bit 2	
Bit 3	
+24 VDC	Power Supply Interface
Logic Ground	
Earth Ground	
Line Freq. Ref.	

Reference Section 8.0 for BIU signal pin assignment.

5.3.2 Type 2 Controller Interface

The Type 2 TF shall provide an interface to a Type 2 CU as defined in Section 3.3.5. The interface to the CU shall be through the connectors and input/output pin terminations defined in Section 3.3.5.2.

5.3.2.1 LOAD SWITCH AND FLASH TRANSFER POSITIONS

Wired sockets shall be provided as a minimum in the quantities listed in Table 5.3.1-1 for the configuration selected. A means shall be provided to allow assigning each load switch socket to control either a vehicle, overlap, or pedestrian movement.

It shall be possible to flash either the Yellow or Red indication on any vehicle movement and to change from one color indication to the other by use of simple tools without the need to unsolder or resolder connections. All flash change means shall be accessible from the cabinet door opening without moving or disconnecting any equipment.

5.3.2.2 INTERFACE TERMINALS

Terminals shall be provided for all input and output functions required by the CU input/output mode in use and the number of load switches of the selected configuration of Table 5.3.1-1.

5.3.2.3 INPUT/OUTPUT MODE

Terminals shall be provided for the I/O Mode Bits defined in Section 3.4.5.2(17) and 3.5.5.5(15). The appropriate input/output mode (0–7) shall be programmed as required by the CU application.

5.3.3 Port 1 Communication Cables

The TF shall provide terminals for connecting communication cables to interconnect the controller Port 1 signals to the BIUs and MMU. Three adjacent terminals shall be provided for each of the **Tx Data, Tx Clock, Rx Data, Rx Clock** signals with the third terminal connected to logic ground. Sufficient terminals shall be provided to terminate the required communication cables for the selected configuration of Table 5.3.1-1. The signals from no more than three communication cables shall be connected to the same terminal.

Each communication cable shall provide twisted pairs for the **Tx Data, Tx Clock, Rx Data, Rx Clock** signals. The twisted pair shall use at a minimum 24 AWG stranded

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wire and have a characteristic impedance of 120 ohms nominal. Overall cable length shall not exceed 15 feet. The communication cable shall include an overall shield or alternately each twisted pair within the cable shall be shielded. Shields shall be terminated to logic ground at the TF communication cable terminals.

Because of the transmission line characteristics required the communications cable used should be recommended by its manufacturer for EIA-485 applications. (Authorized Engineering Information)

Each communication cable connector shall be a 15 pin metal shell D subminiature type. The connector shall utilize male contacts with 15 millionths of an inch gold plating in the contact area. The connector shall intermate with an Amp Incorporated part number 205205-1 or equivalent and be equipped with spring latches, Amp Incorporated part number 745012-1 or equivalent. Pin connections shall be as follows:

Pin	Function
1	Twisted Pair 1 +
2	Not Used
3	Twisted Pair 2 +
4	Not Used
5	Twisted Pair 3 +
6	Not Used
7	Twisted Pair 4 +
8	Not Used
9	Twisted Pair 1 -
10	Not Used
11	Twisted Pair 2 -
12	Not Used
13	Twisted Pair 3 -
14	Not Used
15	Twisted Pair 4 -

Any communication cables provided for manufacturer specific, diagnostic, or test purposes shall correspond to the above requirements.

5.3.4 Detector Rack

The TF shall include a detector rack that accommodates as a minimum the two and four channel detector configurations shown in Table 5.3.4-1. Multiple detector racks shall be capable of being combined to support a quantity of detectors in excess of the configurations listed.

Table 5.3.4-1
DETECTOR RACK CONFIGURATIONS

Detector Rack Configuration	Detector Channels	No. of 2/4 Channel Detectors	BIU Req'd
1	8	4/2	1
2	16	8/4	1

The Type 2 CU Interface allows connecting detector outputs directly to the CU. As such the use of the detector rack is optional when using a Type 2 CU. (Authorized Engineering Information)

Pretimed CU may not require the use of detectors. As such the detector rack is optional when using a pretimed CU. (Authorized Engineering Information)

5.3.4.1 DIMENSIONS

The detector rack shall be capable of being shelf mounted or in a EIA 482.6 mm (19 inch) rack (EIA Standard RS-310) and shall not exceed 152.40 mm (6.00 inches) in height and have a maximum depth of 215.90 mm (8.50 inches).

5.3.4.2 DESIGN

The detector rack shall provide a 44 terminal, double row, 3.962 mm (0.156 inch) contact spacing, Cinch Jones card edge connector 50-44A-30M, or equivalent centered vertically for each detector module. Connector center to center spacing shall be 30.48 mm (1.20 inches). In addition, a dual row 64 pin female DIN 41612 Type B connector centered vertically shall be provided for the Detector Rack BIU. Pin 1 for these connectors shall be located at the top of the detector rack. Card guides shall be provided on the top and bottom of the card rack for each connector position.

The BIU connector shall be the first connector in the detector rack, with all other connectors located to the right of the BIU. The detector module connectors shall be numbered sequentially from Slot 1 through Slot 8. The detector rack signals shall be interconnected to allow inserting a two channel detector in each slot and a four channel detector in each even numbered slot. Detector module outputs shall be assigned to channel numbers in pairs sequentially starting with Slot 1. Reference Section 6.5 for detector module pin assignments.

The detector module communication address inputs shall be connected to correspond to the connector slot number as shown in Table 5.3.4-2.

The detector communications address is intended for future use by detectors. (Authorized Engineering Information)

Table 5.3.4-2
DETECTOR MODULE COMMUNICATIONS ADDRESS

		Communications Address		
Slot	Channels	Bit 0	Bit 1	Bit 2
1	3–4	OFF	OFF	OFF
2	1–2	ON	OFF	OFF
3	7–8	OFF	ON	OFF
4	5–6	ON	ON	OFF
5	11–12	OFF	OFF	ON
6	9–10	ON	OFF	ON

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Table 5.3.4-2 (Continued)
DETECTOR MODULE COMMUNICATIONS ADDRESS

		Communications Address		
Slot	Channels	Bit 0	Bit 1	Bit 2
7	15–16	OFF	ON	ON
8	13–14	ON	ON	ON

Voltage Levels: OFF = Not Connected
ON = Connected to Logic Ground

At least 30% of the area above and beneath each detector shall be open to allow for the free flow of air through the detector rack. There shall be no obstruction within 25.4 mm (1.0 inches) above and below the detector rack within the open area.

The front portion of the detector rack shall be provided with a marker strip to allow identification of detector phase assignment or function.

5.3.4.3 DETECTOR RACK BIU

The Detector Rack shall utilize a BIU conforming to the requirements of Section 8.0 for all detector interface functions. The detector rack BIU address inputs shall control the assignment of detector functions as shown in Tables 5.3.4-3 and 5.3.4-4.

Table 5.3.4-3
DETECTOR RACK BIU ADDRESS ASSIGNMENT

BIU	Detector	BIU Address			
Number	Channels	Bit 0	Bit 1	Bit 2	Bit 3
9	1–16	OFF	OFF	OFF	ON
10	17–32	ON	OFF	OFF	ON
11	33–48	OFF	ON	OFF	ON
12	49–64	ON	ON	OFF	ON
13	Reserved	OFF	OFF	ON	ON
14	Reserved	ON	OFF	ON	ON
15	Spare	OFF	ON	ON	ON
16	Spare	ON	ON	ON	ON

Voltage Levels: OFF = Not Connected
ON = Connected to Logic Ground

Table 5.3.4-4
BIU 9 SIGNAL ASSIGNMENT

Signal	Function
Output 1	Detector Reset Slot 1/2
Output 2	Detector Reset Slot 3/4
Output 3	Detector Reset Slot 5/6
Output 4	Detector Reset Slot 7/8
Output 5	Reserved
Output 6	Reserved
Output 7	Reserved
Output 8	Reserved
Output 9	Reserved
Signal	Function
Output 10	Reserved
Output 11	Reserved
Output 12	Reserved
Output 13	Reserved
Output 14	Reserved
Output 15	Reserved
Input/Output 1	Channel 1 Call [I]
Input/Output 2	Channel 2 Call [I]
Input/Output 3	Channel 3 Call [I]
Input/Output 4	Channel 4 Call [I]
Input/Output 5	Channel 5 Call [I]
Input/Output 6	Channel 6 Call [I]
Input/Output 7	Channel 7 Call [I]
Input/Output 8	Channel 8 Call [I]
Input/Output 9	Channel 9 Call [I]
Input/Output 10	Channel 10 Call [I]
Input/Output 11	Channel 11 Call [I]
Input/Output 12	Channel 12 Call [I]
Input/Output 13	Channel 13 Call [I]
Input/Output 14	Channel 14 Call [I]
Input/Output 15	Channel 15 Call [I]
Input/Output 16	Channel 16 Call [I]
Input/Output 17	Channel 1 Fault Status [I]
Input/Output 18	Channel 2 Fault Status [I]
Input/Output 19	Channel 3 Fault Status [I]
Input/Output 20	Channel 4 Fault Status [I]
Input/Output 21	Channel 5 Fault Status [I]
Input/Output 22	Channel 6 Fault Status [I]
Input/Output 23	Channel 7 Fault Status [I]
Input/Output 24	Channel 8 Fault Status [I]
Input 1	Channel 9 Fault Status
Input 2	Channel 10 Fault Status
Input 3	Channel 11 Fault Status
Input 4	Channel 12 Fault Status
Input 5	Channel 13 Fault Status
Input 6	Channel 14 Fault Status
Input 7	Channel 15 Fault Status
Input 8	Channel 16 Fault Status
Opto Input 1	Reserved
Opto Input 2	Reserved
Opto Input 3	Reserved
Opto Input 4	Reserved
Opto Common	Reserved
Data Transmit	Connected to Data Receive of each detector
Data Receive	Connected to Data Transmit of each detector
Address Bit 0	Reference Table 5.3.4-3
Bit 1	
Bit 2	
Bit 3	Logic Ground
+24 VDC	Power Supply Interface

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Table 5.3.4-4 (Continued)
BIU SIGNAL ASSIGNMENT

Signal	Function
Logic Ground	
Earth Ground	
Line Freq. Ref.	
Reference Section 8.0 for BIU signal pin assignment.	

Detector functions for channels 17–64 shall be assigned to BIU number 10–12 in the same sequence as shown in Table 5.3.4-4.

The Detector Reset outputs shall be connected to pin C of both assigned slots to provide for two channel or four channel detector reset functions.

The Data Transmit and Data Receive functions are intended for future use by detectors. (Authorized Engineering Information)

5.3.4.4 DETECTOR LOOP CONNECTIONS

The channel 1 and 2 loop input pins of each detector connector position actually required for a particular application shall be connected to field terminals using twisted pairs having a minimum of 20 AWG stranded conductor wire with 19 strands. Three adjacent field Terminals shall be provided for each loop input.

Field installation practices or detector unit design may require connecting the shield of the loop lead-in cable to the third terminal. (Authorized Engineering Information)

5.3.4.5 POWER SUPPLY CONNECTIONS

The detector rack shall provide terminals or other connection means for the following power supply signals:

+12 VDC
+24 VDC
Logic Ground
Earth Ground
Line Frequency Reference

The +12 VDC is intended to provide power only to detectors. (Authorized Engineering Information)

5.3.5 Power Supply

The TF shall include a power supply to provide regulated DC power, unregulated AC power and a line frequency reference for the Detector rack, BIUs, load switches, and other auxiliary equipment.

The Type 2 Controller interface provides 500 milliamps of +24 VDC power. As such the use of the cabinet power supply is optional when using a Type 2 controller. (Authorized Engineering Information)

5.3.5.1 DIMENSIONS

The power supply shall be capable of being shelf mounted or in an EIA 486.2 mm (19 inch) rack (EIA Standard RS-310). The power supply shall not exceed 152.40 mm (6 inch) in height and have a maximum depth of 215.90 mm (8.50 inches) including connectors, harnesses and protrusions.

5.3.5.2 ENVIRONMENTAL REQUIREMENTS

The power supply shall perform its specified functions under the environmental conditions set forth in Section 2.0.

5.3.5.3 ELECTRICAL REQUIREMENTS

1. The power supply shall provide positive 12 +1 volts and 24 +2 volts DC power regulated over an **AC line** voltage variation from 89 volts to 135 volts from 1/8 load to full load and unregulated 12 volts AC. The unregulated voltage shall nominally measure 12 volts with an **AC line** voltage of 120 volts and shall be no less than 7.5 volts with an **AC line** voltage of 89 volts.
2. Minimum average continuous current capability shall be as shown below with DC voltages having less than 0.5 volts peak-to-peak ripple:

+12 VDC	2.0 Amps
+24 VDC	2.0 Amps
12 VAC	0.250 Amps

Voltage regulation does not have to be maintained if current exceeds values shown.

The +12 VDC is intended to provide power only to detectors. (Authorized Engineering Information)

3. Under full load conditions the power supply shall provide 50 milliseconds of hold up time for +12 VDC and +24 VDC upon loss of **AC line** voltage. During the hold up period the +12 VDC shall not drop below +10.8 VDC and the +24 VDC shall not drop below +18 VDC.
4. The +12 VDC and +24 VDC outputs shall withstand a 10 millisecond 10 ampere load surge.
5. The front panel of the power supply shall include over current protection devices for the **AC line** and all output voltages.
6. A line frequency output shall provide a reference to the **AC line** frequency. This output shall alternate at the line frequency (nominally 60 pulses per second) and shall be **True** in phase with the positive half cycle and shall switch within 5 degrees of the zero crossing point of the **AC line**.

The line frequency output shall have the following characteristics:

a. Shall be capable of providing 50 milliamperes of current in the **False** state.
b. Current sinking capability in the **True** state shall be a minimum of 50 milliamperes.
c. The output shall have a rise and fall time of no greater than 50 microseconds when switching a load capacitance of 10,000 picofarads.

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5.3.5.4 POWER SUPPLY INPUTS

5.3.5.4.1 AC Line

This shall be the current protected side of 120 VAC 60 hertz power source within the power supply.

5.3.5.4.2 AC Neutral

This shall be the unfused and unswitched side of 120 VAC 60 hertz power source taken from neutral output of ac power source. The 12 VAC power supply output shall be referenced to **AC Neutral**.

This input shall not be connected to **Logic Ground** or **Earth Ground** within the power supply.

5.3.5.4.3 Earth Ground

This input shall be electrically connected to the power supply chassis and connector shell.

This input shall not be connected to **Logic Ground** or **AC Neutral** within the power supply.

5.3.5.4.4 Pin Connections

The power supply connector shall be located on the front of the unit, have a metallic shell which is connected to the chassis ground internally and mate with an MS3106( )-18-1SW cable connector, or equivalent.

Connector pin terminations shall be as follows:

Pin	Function
A	AC Neutral
B	Line Frequency Reference
C	AC Line
D	+12 VDC
E	+24 VDC
F	Reserved
G	Logic Ground
H	Earth Ground
I	12 VAC
J	Reserved

5.3.6 Field Terminals

5.3.6.1 GENERAL

Terminals for signal heads, detectors, primary feed, and interconnections shall meet the requirements of this section, including Table 5.3.6-1.

Table 5.3.6-1
FIELD TERMINALS

Function	Type	Size	Characteristics
Signal Feeds	Screw or Compression	#10 or larger 7.93 mm (5/16 inch) minimum	10 Amps min. Shall terminate minimum of three #14 AWG wires
Detector Lead-In	Screw or Compression	#8 or larger 6.35 mm (1/4 inch) minimum	Shall terminate minimum of one #12 AWG wire
Interconnect	Screw or Compression	#6 or larger 6.35 mm (1/4 inch) minimum	Shall terminate minimum of one #12 AWG wire
Primary Feeds	Compression	Not Applicable	Shall terminate minimum of one #6 AWG wire
Earth Ground	Compression	Not Applicable	Shall terminate minimum of one #8 AWG wire

1. Terminal connections shall be made with slotted head screws or equivalent connecting means. Screw size shown in Table 5.3.6-1 is not applicable to compression type Terminals.
2. All materials, including screws and threaded portions, used in terminals and terminal blocks shall be nickle plated brass or stainless steel.
3. A terminal block shall be capable of withstanding without breakdown for one minute the application of a 60 Hz sinusoidal potential of 600 volts RMS applied to the terminal between live parts that are not conductively interconnected and between live parts and the surface to which the terminal block is mounted.
4. Terminal blocks shall have mechanical characteristics to properly support wiring without warping the block.

5.3.6.2 NUMBER AND SIZE OF TERMINALS

1. One terminal shall be provided for each load switch output.
2. It shall be possible to terminate a minimum of 16 #14 AWG or 5 #10 AWG neutral leads.

5.3.6.3 FIELD TERMINAL NOMENCLATURE

Field terminals shall be numbered using the following format:

1. Load Switch Field Terminals shall be labeled with the load switch number and output per the following example:

Function	Label
Load Switch 1 Green	1G
Load Switch 1 Yellow	1Y
Load Switch 1 Red	1R

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2. Detector loop field terminals shall be labeled with the letter "L" followed by the detector channel number and loop connection (A or B) per the following example:

Function	Label
Detector Channel 1	L1A
Loop	L1B
Detector Channel 2	L2A
Loop	L2B

3. Pedestrian call field terminals shall be labeled with the letters "PC" followed by the phase assignment per the following example:

Function	Label
Phase 1 Ped Call	PC1
Phase 2 Ped Call	PC2
Ped Call Common	PC COMM

4. Preempt call field terminals shall be labeled with the letters "PE" followed by the preempt number per the following example:

Function	Label
Preempt 1 Call	PE1
Preempt 2 Call	PE2

5. Coordination interconnect field terminals shall be labeled as follows:

Function	Label
Timing Plan A	TPA
Timing Plan B	TPB
Timing Plan C	TPC
Timing Plan D	TPD
Offset 1	OFT1
Offset 2	OFT2
Offset 3	OFT3
Interconnect Common	IC COMM

6. The AC power service field terminals shall be labeled as follows:

Function	Label
AC Line	LINE
AC Neutral	NEUTRAL
Earth Ground	EARTH

7. The system interface field terminals shall be labeled as follows:

Function	Label
Transmit 1	TX1
Transmit 2	TX2
Receive 1	RX1
Receive 2	RX2

5.3.7 Terminal Types and Practices

1. All terminals carrying 120 VAC in normal operation shall be covered unless otherwise protected by recessing or by terminal strip barriers. This includes all terminals exposed when the front door of the cabinet is open and all panels and covers are in their normal operation position.
2. All MMU input channels that can be used to monitor the maximum number of signals available in a given configuration in Tables 5.3.1-1 or 5.3.4-1 shall be terminated. Provision shall be made to terminate any unused red monitoring inputs.
3. The MMU supply, control input and control output leads actually required to be used in a particular configuration shall be terminated.

All other points not enumerated above, including "spare," "reserved," "manufacturers use only," and "no connection" shall not be required to be installed in the CU, MMU, or detector harness.

5.4 ELECTRICAL REQUIREMENTS

5.4.1 AC Service

The TF shall operate properly when supplied with single-phase AC power, 89–135 volts, 60 ±3 Hz.

5.4.2 Power Distribution Within Cabinet

(See Figure 5.4.2-1).

5.4.2.1 GROUNDING SYSTEM

The grounding system in the cabinet shall be divided into three separate and distinct circuits, all of which shall be connected together at a single point as shown in Figure 5.4.2-1.

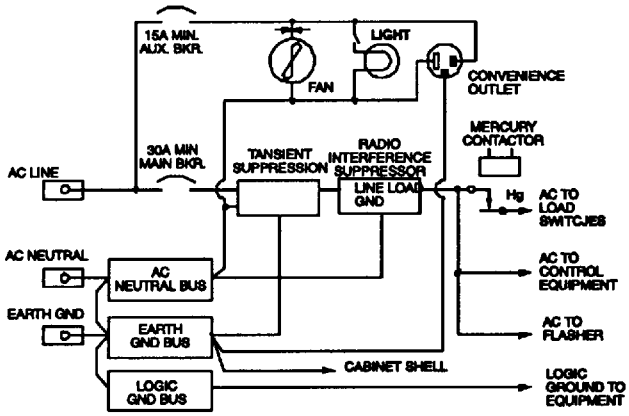

Figure 5.4.2-1
CABINET POWER DISTRIBUTION SCHEMATIC

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The purpose of this requirement is to eliminate ground loops, adequately direct transients to ground, and to allow for testing of the separation between the grounding circuits by temporarily removing the jumpers. (Authorized Engineering Information)

Field installation practices may require separating AC **Neutral** and/or **Logic Ground** from **Earth Ground** within the cabinet. (Authorized Engineering Information)

1. The **AC Neutral** bus is the set of terminals within the cabinet to which all of the neutral conductors are terminated. The **AC Neutral** bus shall be a solid metallic multi-terminal strip located in close proximity to the primary feed entering the cabinet. Subsidiary neutral bus terminal strips may be located as necessary in the cabinet for use with the control equipment. Neutral terminal strip(s) shall be insulated from the cabinet.
2. The **Earth Ground** bus is the set of terminals within the cabinet that is directly and permanently connected to the cabinet shell and the earth. The **Earth Ground** bus shall be a solid metallic multi-terminal strip located in close proximity to the power service entering the cabinet. This **Earth Ground** shall be connected to the cabinet shell in a manner that minimizes the length of the conducting path.

   It is intended that the **Earth Ground** bus be connected to a good earth ground such as a driven ground rod or rods.(Authorized Engineering Information.)

   The **Earth Ground** connection to each unit in the cabinet shall be run separately and directly to this terminal strip or to subsidiary **Earth Ground** busses. Each metallic connector shell on a cable carrying 120 VAC shall be connected to **Earth Ground**.
3. The **Logic Ground** bus is that set of Terminals within the cabinet to which all **Logic Ground** conductors are terminated.

   All dc circuits shall use the **Logic Ground** as the return circuit.

5.4.2.2 DISCONNECTING MEANS

Type	Poles	Min. Amps	Interrupting Capacity
Main	1	30	5,000 amperes
Auxiliary	1	15	5,000 amperes

The rating of the main disconnect means with overcurrent protection shall be not less than 125% of the maximum anticipated continuous load. All disconnecting means when used shall be the "trip-indicating-trip-free" type.

5.4.2.3 SIGNAL BUS

The signal bus shall be connected to the incoming AC **line** through a signal bus mercury contactor and a overcurrent protection device. The signal bus mercury contactor shall be energized to provide power to the signal bus. The current rating of the signal bus mercury contactor shall be at least the current rating of the main overcurrent protection device.

5.4.2.4 AC SERVICE TRANSIENT SUPPRESSION

The transient suppression device for the primary feed of the cabinet shall be connected on the load side of the cabinet overcurrent protection device as shown in Figure 5.4.2-1. The transient suppression device shall withstand a 20,000 ampere surge current with a 8x20 microsecond (time to crest x time to second halfcrest) waveform twenty times at 3-minute intervals between surges without damage or degradation to the suppressor. Output voltage must not exceed 500 volts at any time during the test.

Because the severity of naturally occurring transients is highly variable AC service transient suppression requirements may vary with the application. For further information on transient protection of traffic control equipment refer to NCHRP report 317. (Authorized Engineering Information)

5.4.2.5 RADIO INTERFERENCE SUPPRESSION

Each cabinet shall be equipped with a radio interference suppressor installed at the input power point. It shall provide a minimum attenuation of 50 decibels over a frequency range of from 200 kilohertz to 75 megahertz, when used with normal installations.

The radio interference suppressor shall have a current rating equal to as a minimum the rating of the main disconnect means specified in paragraph 5.4.2.2 and be designed for operation on 120 volts, 60 hertz, single phase circuits.

The ground connection of the radio interference suppressor shall be connected only to **AC neutral** and shall not be connected to **Earth Ground** directly.

5.4.2.6 CONVENIENCE RECEPTACLE

A convenience receptacle shall be provided as part of the TF. The convenience receptacle shall be a duplex, three-prong, NEMA Type 5-15R grounding type outlet and shall have independent ground fault circuit protection.

5.4.2.7 LIGHTING FIXTURE

An incandescent or fluorescent light shall be provided as part of the TF.

5.4.2.7.1 Fluorescent Fixture

The fluorescent lighting fixture shall be mounted on the inside top of the cabinet near the front edge. The fixture shall be rated to accommodate a F15T8 lamp operated

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from a normal power factor UL or ETL listed ballast (lamp not required to be provided).

5.4.2.7.2 Incandescent Fixture

The incandescent lamp receptacle shall be mounted on the inside top of the cabinet near the front edge. The receptacle shall be rated to accommodate a 100 watt medium base lamp (lamp not required to be provided).

5.4.2.7.3 Lighting Fixture Switch

The "**On-Off**" switch for the lighting fixture shall be either of the following:

1. A toggle switch mounted on an inside control panel, or
2. A door actuated switch that turns the light **On** when the door is open and **Off** when the door is closed.

5.4.3 Communications Transient Suppression

A transient suppressor shall be provided for the system interface communications lines when used. This suppressor shall withstand a 100 ampere 10x700 microsecond waveform 20 times at 30 second intervals between surges without damage or degradation to the suppressor. The transient surge shall be applied both line to line and line to ground. Output voltage shall not exceed 8 volts line to line or 250 volts line to ground at any time during the test.

Because the severity of naturally occurring transients is highly variable communications transient suppression requirements may vary with the application. For further information on transient protection of traffic control equipment refer to NCHRP report 317. (Authorized Engineering Information)

5.5 CONTROL CIRCUITS

5.5.1 Auto/Flash Switch

An auto/flash switch shall be accessible to an operator when the cabinet door is open. The switch shall be rated by its manufacturer for the voltages and currents that may be expected to be present in the part of the control circuit where it is used.

The switch positions shall be labeled "**Auto**" and "**Flash.**" In the "**Auto**" position, this switch does not affect the normal operation of the facilities. In the "**Flash**" position, the signal bus relay and flash transfer relays shall be de-energized, connecting the output(s) of the flasher to the appropriate field leads and interrupting the signal bus supply to the load switches.

5.5.2 Flash Transfer Control

1. The coil of the flash transfer relay(s) shall be deenergized for flashing operation.
2. The flash transfer relay(s) shall be located in close proximity to the load switches, flasher, and signal field terminals.
3. Flash transfer relay sockets shall mate with a Cinch-Jones P2408 or equivalent. They shall be wired and space provided to accept a relay as described in Section 6.4, Flash Transfer Relays.

5.5.3 Malfunction Management Unit

1. Type Selection

The type select input to the MMU shall be connected to logic ground to select Type 16 (16 channel) operation.

2. Interlock

The facilities shall be so constructed that the intersection will revert to flashing operation if the MMU is disconnected.

3. Red Enable

The **red enable** input to the MMU shall be connected to the **AC Line** side of the signal bus relay coil.

4. 24-Volt Monitoring

The MMU **24V Monitor I** input shall be connected to the +24 volt feed to the load switches. The **24V Monitor II** shall be used to monitor any other +24 volt supply(s) required for safe operation of the intersection.

If only one +24 volt power source is used in the cabinet, **24V Monitor I** and **II** shall be connected together.

5. Controller Voltage Monitor

When using a Type 1 CU the MMU **Controller Voltage Monitor** input shall be connected to the CU **Fault Monitor** output.

If a Type 2 CU is used, connection to the MMU **Controller Voltage Monitor** input will depend on the controller input/output mode. If mode 0 is used the MMU **Controller Voltage Monitor** input shall be connected to the CU **Controller Voltage Monitor** output. For all other modes (1–7) the CU **Fault Monitor** output shall be used.

6. Restart

Actuation of the start-delay shall remove power from the CU and power supply.

7. Stop Time

Stop Time shall be applied to all rings of the CU whenever the MMU is in the fault condition.

8. Flash on Fault

The MMU shall place the intersection into flashing operation when in the fault condition.

9. Load Switch Monitoring

Each of the MMU channels required for the application shall be wired to monitor the green, yellow, and red outputs of the associated load switch position in the TF as shown in Table 5.5.3-1.

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Table 5.5.3-1
MMU CHANNEL ASSIGNMENTS

MMU Channel	Load Switch
Channel 1	Load Switch 1
Channel 2	Load Switch 2
Channel 3	Load Switch 3
Channel 4	Load Switch 4
Channel 5	Load Switch 5
Channel 6	Load Switch 6
Channel 7	Load Switch 7
Channel 8	Load Switch 8
Channel 9	Load Switch 9
Channel 10	Load Switch 10
Channel 11	Load Switch 11
Channel 12	Load Switch 12
Channel 13	Load Switch 13
Channel 14	Load Switch 14
Channel 15	Load Switch 15
Channel 16	Load Switch 16

Current interrupting devices should not be placed between the point at which the load switch output is monitored and the field connection as this may prevent the MMU from detecting the absence of a field signal if the interrupting device opens. (Authorized Engineering Information)

When the circuit connected to the sensing input of the MMU exhibits high impedance characteristics such as an unconnected load, burned out lamp, or dimmers, it may be necessary to place a low impedance device external to the MMU between the MMU input and **AC Line**. (Authorized Engineering Information)

All unused Red/Dont Walk signal inputs shall be terminated to **AC Line**. (Authorized Engineering Information)

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SECTION 6
AUXILIARY DEVICES

This section defines the minimum requirements for auxiliary devices within the cabinet consisting of solid state load switches, solid state flashers, flash transfer relays, and inductive loop detectors.

6.1 Definitions

(reserved)

6.2 Three-Circuit Solid State Load Switches

This section defines the solid state load switches which are connected between the AC line power and the traffic signals. For the purpose of these standards, the term "solid state" shall be construed to mean that the main current to the signal load is not switched by electro-mechanical relay contacts.

6.2.1 Physical Characteristics

1. The overall dimensions of the switch shall not exceed 235 mm (8.75 inches) from the surface of the connector, to the front of the unit including the handle or gripping device. The switch shall be no more than 4.445 mm (1.75 inches) in width and no more than 10.668 cm (4.20 inches) in height.
2. The switch shall intermate with a Beau-Vernitron type socket S-5412 or Cinch-Jones socket S-2412SB, or equivalent.
3. The switch shall be so constructed that its lower surface will be no more than 5.334 mm (2.100 inches) below the centerline of the connector.
4. The switch shall be so constructed that no part of it will extend more than 2.286 mm (0.900 inch) to the left and 2.794 mm (1.100 inches) to the right of the centerline of the connector as viewed from the front. See Section 5, Figure 5.2.8-1.
5. Serviceable internal components of the load switch shall be readily accessible.
6. An enclosure suitably protected against corrosion shall be provided to enclose all electrical parts of the load switches.
7. The front panel of the load switch shall be provided with one indicator per input circuit to indicate the state of each input circuit of the load switch. The indicators shall be mounted as follows when oriented as normally mounted:
   Circuit A at the top.
   Circuit B in the middle.
   Circuit C at the bottom.
8. Material and Construction of Rigid Printed Circuit Assemblies
   a. Materials
      All printed circuit boards shall be made from NEMA (FR-4) glass-epoxy, flame retardant material, or equivalent. (See NEMA Standards Publication LI-1-1989, Industrial Laminated Thermosetting Products). Circuit boards exceeding 50.8 mm (2 inches) in any dimension shall be at least 1.58 mm (1/16 inch) nominal thickness. Circuit boards not exceeding 50.8 (2 inches) in any dimension shall be at least 0.79 mm (1/32 inch) nominal thickness.
   b. Conductors
      The walls of all plated-through holes shall have a minimum copper plating thickness of 0.001 inch. All circuit tracks shall have a conductivity equivalent to at least 56.7 grams of copper per square foot of surface.
   c. Component Identification
      The unit shall be designed so that each component is identified by a circuit reference symbol. This identification shall be affixed to the printed circuit board(s), to the cover of the unit, or in an assembly drawing provided with the unit.
9. The switch shall be so constructed that personnel inserting or removing the load switch will not be exposed to parts having live voltage nor be required to insert their hands or fingers into the mounting rack.

6.2.2 General Electrical Characteristics

1. Switching capabilities shall be provided for three independent circuits in each load switch.
2. Connector pin assignments shall be as shown in Figure 6.2-1.
3. The switch input and direct current voltage input shall be so isolated from the power line that transients as described in Section 2.1.6 applied to the power line with a 25 watt lamp load shall not cause a destructive failure in the load switch, and shall not cause more than 0.5 volts to appear across a 10K ohm resistor connected across a switch input and the direct current voltage input. When the transients of Section 2.1.6.1 are applied to the load switch at a temperature of 21°C ±6° C, they shall not cause the load switch to conduct, as measured by an oscilloscope.
4. The switch shall turn ON within 10 degrees of the zero voltage point of the AC line sinusoid on the first turn-on cycle. All subsequent cycles shall turn ON within 5 degrees of the zero voltage point of the AC line sinusoid. The switch shall turn ON within one half cycle following the application of the input sig-

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nal. The switch shall turn OFF within 5 degrees of the zero current point of the AC line sinusoid and within one half cycle following the removal of the input signal.

5. Each load switch shall have electrical isolation between all inputs (pins 6, 8, 9, and 10) and all outputs (pins 1, 3, 5, and 7) of at least 2000 volts DC and at least 100 megohms resistive.
6. **Logic Ground** shall not be connected to either **Earth Ground** or **AC Neutral** within the unit.
7. **Earth Ground** shall not be connected to either **Logic Ground** or **AC Neutral** within the unit.
8. All metal portions of the enclosure including the handle of the load switches shall be connected to **Earth Ground** within the unit.
9. The load switch shall perform all of its defined functions when supplied from a 24 ± 2 volt DC source.

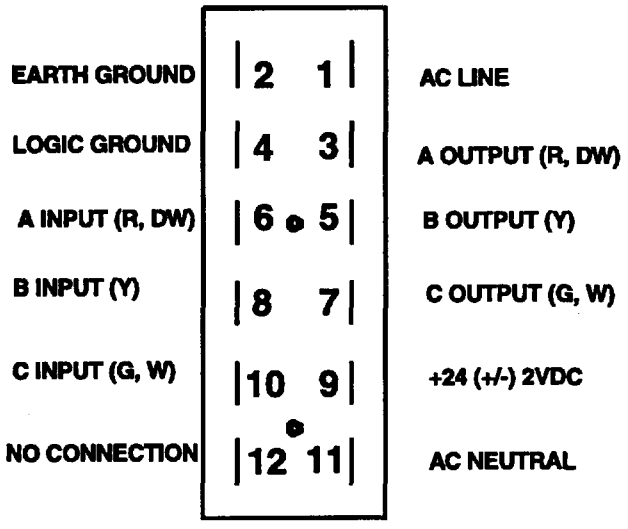

Figure 6.2-1
CONNECTOR PIN ASSIGNMENTS

Notes:
a. The terminal reference is a pin side view of the male connector.
b. Parenthetical notations associated with A, B, C inputs and outputs denote the normal usage of the termination with vehicle or pedestrian signals.
R = **Red** Y = **Yellow** G = **Green**
W = **Walk** DW = **Dont Walk**
c. *Pin 4 Logic Ground is for special function use only, not to be used for* normal switching circuit currents. During normal operation standard load switch functions shall not require a connection to this pin.

6.2.3 Input Electrical Characteristics

1. All inputs shall be negative true logic which is referenced to the common of the +24 volt DC supply and which is characterized by the following:
   a. The transition zone of the input circuitry from the conducting state to the non-conducting state (and vice versa) shall occur between 6 and 16 volts.
   b. A voltage between 0 and 6 volts shall cause the output device to conduct.
   c. A voltage greater than 16 volts shall cause the output device not to conduct.
2. In absense of an input signal, the voltage at the input shall rise to the level of the +24 VDC supply when the input is connected to this supply through an external 10 K ohm pull-up resistor.
3. The load switch shall not draw more than 20 milliamperes from a +26 VDC supply unless more than one circuit is energized in which case it shall not draw more than 20 milliamperes times the number of circuits energized.
4. Each input circuit of the load switch shall have reverse polarity protection.

6.2.4 Output Electrical Characteristics

1. The output current from the load switch through a 1200 W load when the load switch is in the OFF state shall not exceed 10 milliamperes peak at 135 volts RMS AC.
2. Each load switch output shall have a peak stand-off voltage of 500 volts or greater.
3. Each load switch output shall have a dv/dt rating of at least 100 volts per microsecond when measured at 21° C using the circuit in Figure 6.2-2.
4. Each switching circuit shall have a minimum rating of 10 amperes RMS for either a tungsten lamp load or power factor corrected gas tubing transformer loads (power factor greater than 0.8) over a voltage range of 89 to 135 volts RMS AC at 60 hertz. Additionally, each load switch shall be capable of switching currents as low as 100 milliamperes. The load switch shall be rated for 10 amperes continuous load divided between the circuits in any proportion, and additionally each circuit shall be capable of continuously conducting 10 amperes. These ratings shall be for operation in still air when the load switch is oriented as normally mounted.
5. Each load switch circuit shall be designed to switch a 1200 watt tungsten lamp load operating from a 120 volts RMS AC source for a minimum of 10 million operations.
6. Each load switch circuit shall be capable of withstanding a one second surge current of 40 amperes RMS (56.6 peak) at 60 hertz.
7. Each load switch circuit shall be capable of withstanding a one cycle surge current of 175 amperes RMS (247.5 peak) at 60 hertz while operating from a 120 volts RMS AC source.

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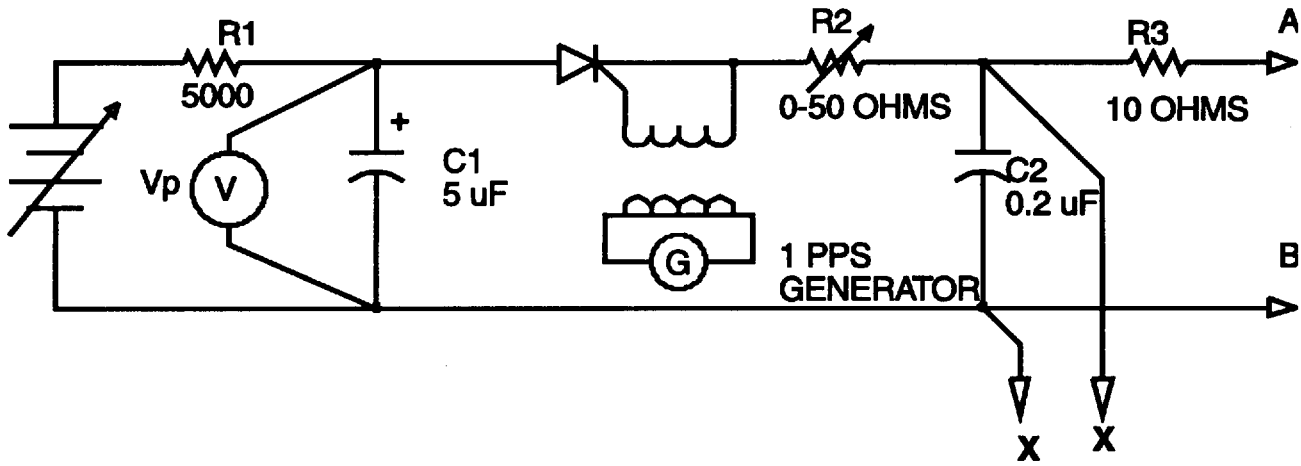

Figure 6.2-2
PIV AND DV/DT TEST CIRCUIT (CIRCUIT FOR SOLID STATE LOAD SWITCHES)

TEST PROCEDURE FOR PIV AND DV/DT TESTING

1. With the power removed from the load, connect PINS 1 (AC Line) and 11 (AC Neutral) of the load switch to terminal A of the test circuit.
2. Connect terminal B of the test circuit to PIN 3 (Circuit A) of the load switch.
3. Set Vp to 500 VDC.
4. Decrease R2 until the load switch output conducts or the value of R2 reaches zero. If the load switch starts conducting when the test pulse is applied, back R2 off slightly to a higher resistance point above which the load switch does not conduct. Conduction of the load switch circuit due to either PIV or dv/dt can be observed by the flickering or dipping of the Vp meter.
5. Measure the time required for the wave form at points x-x to reach 200 VDC dv/dt = 200/time measured.
6. Repeat the test steps 4 and 5 with terminals A and B of the test circuit reversed.
7. Connect terminal B of the test circuit to PIN 5 (Circuit B) of the load switch and connect terminal A of the test circuit to PINS 1 and 11 of the load switch.
8. Repeat steps 3 through 6 for circuit B of the load switch.
9. Connect terminal B of the test circuit to PIN 7 (Circuit C) of the load switch and connect terminal A of the test circuit to PINS 1 and 11 of the load switch.
10. Repeat steps 3 through 6 for circuit C of the load switch.

Circuit Notes:
1. R2 and R3 shall be low inductance resistors such as carbon pile devices.
2. The load connected to x-x shall be between 500k ohms and 250 megohms (resistive).

6.3 SOLID STATE FLASHERS

This section defines solid state flashers which are used to periodically interrupt a source of AC line power for the purpose of providing flashing traffic signals. For the purpose of these standards, the term "solid state" shall be construed to mean that the main current to the signal load is not switched by electro-mechanical operated contacts.

6.3.1 Type of Flasher

Dual circuit, 15 amperes RMS per circuit.

6.3.2 Physical Characteristics

1. The overall dimensions of the flasher shall not exceed 22.223 cm (8.75 inches) from the front panel surface holding the mating connector, including the any handle or gripping device. The flasher shall be no more than 48.26 mm (1.9 inches) in width and no more than 10.67 cm (4.2 inches) high.
2. The flasher shall intermate with a Beau-Vernitron socket type S-5406 or Cinch-Jones socket S-406-SB, or equivalent.
3. The flasher shall be so constructed that its lower surface will be no more than 5.334 cm (2.100 inches) below the center line of the connector configuration.

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4. The flasher shall be so constructed that no part of it will extend more than 22.860 mm (0.900 inches) to the left and 27.940 mm (1.100 inches) to the right of the centerline of the connector pin configuration as viewed from the front. See Section 5 Figure 5.2.8-3.
5. Serviceable internal components of the flasher shall be readily accessible.
6. The flasher shall be so constructed that personnel inserting or removing the module will not be exposed to any part having live voltage nor be required to insert either their hands or fingers into the load rack.
7. An enclosure suitably protected against corrosion shall be provided to enclose all electrical parts of the flasher.
8. Material and Construction of Rigid Printed Circuit Assemblies
   a. Materials
   All printed circuit boards shall be made from NEMA (FR-4) glass-epoxy, or equivalent (see NEMA Standards Publication LI 1-1989, Industrial Laminated Thermosetting Products.) Circuits boards exceeding 50.8 cm (2 inches) in any dimension shall be at least 1.59 mm (0.063 inch) nominal thickness. Circuit boards not exceeding 50.8 cm (2 inches) in any dimension shall be at least 0.79 mm (0.031 inch) nominal thickness.
   b. Conductors
   The walls of all plated through holes shall have a minimum copper plating thickness of 0.0254 mm (0.001 inch). All circuit tracks shall have a conductivity equivalent to at least 0.0610 gm/cm^2 (2 oz/ft^2) of copper. All electrical mating surfaces shall be made of non-corrosive material.
   c. Component Identification
   The unit shall be designed so that each component is identified by circuit reference symbol. This identification may be affixed to the printed circuit board(s), the cover of the unit, or in an assembly drawing provided with the unit.
9. All metal portions of the enclosure including the handle of the load switches shall be connected to **Earth Ground** within the unit.

6.3.3 General Electrical Characteristics

Flashers shall have the following electrical characteristics:

1. The flashing output shall consist of two outputs each rated at 15 amperes RMS.
2. The rating of the output circuit shall be the minimum rating for a tungsten lamp or power factor corrected gas tubing transformer load over a voltage range of 60 to 135 volts RMS AC at 60 hertz and shall not be derated for operation over the ambient temperature range of -34° to +74° C (-30° to +165° F) and the humidity range as both outlined in Section 2 Environmental Requirements.
3. Input to the solid state flasher shall consist solely of the 60 hertz AC power source. This input shall supply the power for the output circuit and also provide power to the flasher logic. The flasher shall turn **On** within 10° of the zero voltage point of the AC line sinusoid on the first flash cycle (on-off cycle). All subsequent cycles shall turn **On** within 5° of the zero voltage point. The flasher shall turn **Off** within 5° of the zero current point of the AC line sinusoid.
4. The "flashing" voltage output shall provide not less than 50 nor more than 60 flashes per minute with an **On** period of 50 ± 5 percent.
5. The flasher output shall have a dv/dt rating of 100 volts per microsecond at 21° C (70° F), when tested as shown in Figure 6.3-1.
6. The flasher output shall have a peak stand-off voltage of 500 volts or greater at 21° C (70° F), when tested as shown in Figure 6.3-1.
7. The output current from the flasher through an 1800 watt load when the flasher is in the **Off** state shall not exceed a maximum of 10 milliamperes peak at 135 volts RMS AC.
8. The flasher shall be so designed that circuit #1 will be **On** when circuit #2 is **Off**, and vice versa. The maximum **Off** period when both circuit #1 and circuit #2 are **Off**, or the maximum period when both circuit #1 and circuit #2 are ON, shall not exceed 17 milliseconds during the transition from **Off** to **On** and **On** to **Off**.
9. Connector pin assignments shall be as shown in Figure 6.3-2.
10. The front panel of the flasher shall provide two indicators to indicate the state of the output circuits of the flasher.
11. The flasher shall operate for a minimum of 10 million operations when switching an 1800 watt tungsten lamp operating from a 135 volts RMS AC source or an open circuit load.
12. Each flasher output circuit shall be capable of withstanding a one second surge current of 40 amperes RMS (56.6 peak) at 60 hertz.
13. Each flasher output circuit shall be capable of withstanding a one cycle surge current of 175 amperes RMS (247.5 peak) at 60 hertz.

6.4 FLASH TRANSFER RELAYS

These standards define the minimum requirements for an interchangeable electromechanical flash transfer relay. This relay is intended to be used for transferring traffic signal circuits from the outputs of the load switches to the output(s) of a flasher.

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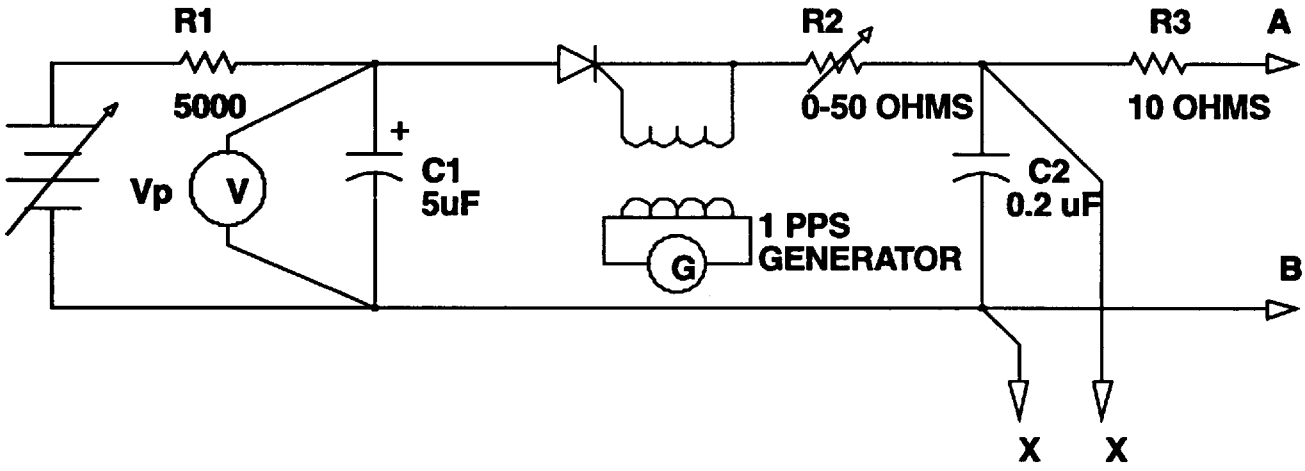

FIGURE 6.3-1
PIV AND DV/DT TEST CIRCUIT (CIRCUIT FOR SOLID STATE FLASHERS)

Test Procedure For PIV and dv/dt Testing

1. Connect pins 10 and 11 of the flasher to terminal A of the test circuit.
2. Connect terminal B of the test circuit to pin 7 of the flasher.
3. Set Vp to 500 VDC.
4. Decrease R2 until the flasher generates an output or the minimum resistance is reached. If the flasher fails, back off R2 slightly to higher resistance point at which the flasher just passes.
5. Measure time required for wave at points x-x to reach 200 VDC dv/dt = 200/time measured.
6. Repeat the test with the connector pins A and B reversed.
7. Repeat steps 1 through 6 with terminal B of the test fixture connected to pin 8 of the flasher.
8. Notes:
   a. A failure of the flasher for either dv/dt or PIV will result in the Vp meter dipping or flickering.
   b. R2 and R3 are carbon pile resistors (low inductive type).
   c. Load between x-x must be between 500 K ohms and 250 M ohms (resistive).

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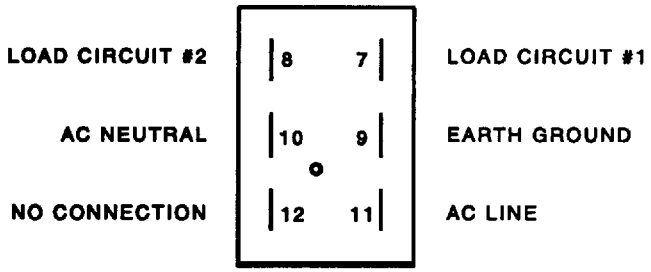


Figure 6.3-2
CONNECTOR PIN ASSIGNMENTS SOLID STATE FLASHER (VIEWED—CONNECTOR END)

6.4.1 Environmental Requirements

6.4.1.1 TEMPERATURE AND HUMIDITY

The relay shall maintain all of its defined functions over the temperature and humidity range of Section 2.1.5. Neither the protective case nor any other part shall deform when the relay is operated under full load at maximum temperature with 135 VAC continuously applied to the coil.

6.4.1.2 VIBRATION AND SHOCK

The relay shall operate and maintain its physical integrity when subjected to the vibration and shock requirements of Sections 2.1.9 and 2.1.10.

The relay contacts may momentarily change state when subjected to the vibration and shock defined above. (Authorized Engineering Information)

6.4.1.3 TRANSIENTS

The relay shall be capable of withstanding the high energy transient requirements of section 2.1.8.

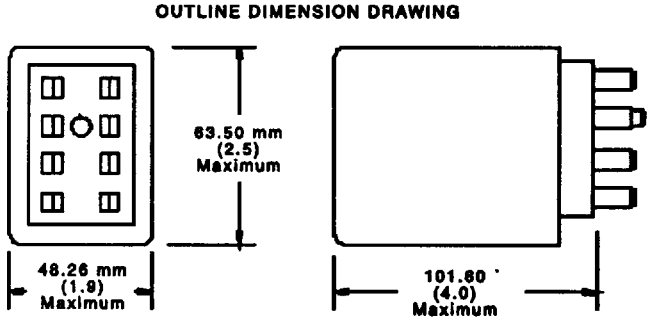
6.4.2 Mechanical Requirements

6.4.2.1 ENCLOSURE

All electrical parts of the relay shall be enclosed in a transparent plastic case. This case shall protect the relay from dust, moisture, and other contamination. It shall be constructed so that the contacts and coil assembly may be viewed through the sides of the case. It shall be sufficiently rugged to permit the relay to be inserted and removed form its mating socket using the case as a handle.

6.4.2.2 CONTACTS AND CONNECTOR

The relay shall be provided with two single-pole, double-throw (form C) contacts and mount on an eight pin spade plug base wired as shown in Figure 6.4-1. The spade plug base shall mate with a Cinch-Jones 2408SB socket or equivalent.



Note: All dimensions in parenthesis are in inches.

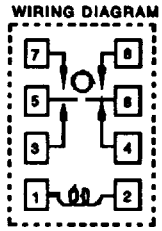


Figure 6.4-1
FLASH TRANSFER RELAY WIRING DIAGRAM

6.4.2.3 DIMENSIONS

The relay shall not exceed the physical dimensions shown in Figure 6.4-1.

6.4.3 Electrical Requirements

6.4.3.1 CONTACT RATING

The contact points and contact arms shall be capable of operating for 30,000 cycles with 10 amperes of tungsten load per contact at 120 VAC.

6.4.3.2 CONTACT MATERIAL

Contact points shall be of fine silver, silver-alloy, or superior alternative material.

6.4.3.3 COIL RATING

The relay coil shall have a maximum power consumption of 10 volt-amperes at nominal line voltage and shall be designed for continuous duty from 89 to 135 VAC.

Drop out time shall not exceed 50 milliseconds after removal of power from the relay coil.

6.4.3.4 INSULATION

The relay shall be capable of withstanding a voltage of 1500 volts RMS at 60 Hz applied between contacts and coil or frame. It shall be able to withstand a voltage of 600 volts RMS at 60 Hz applied between open contacts.

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6.5 INDUCTIVE LOOP DETECTORS

Section 6.5 responds to the need for a series of vehicle loop detectors which provide inputs for traffic-actuated or traffic-responsive control, surveillance, or data collection systems. The inductive loop detector responds to the presence of vehicles on the roadway by relying upon the effect of the conductive mass of the vehicle on the alternating magnetic field of a loop. When a vehicle passes over the loop of wire embedded in the surface of the roadway, it reacts with the alternating magnetic field which is associated with that loop.

These standards cover the performance and design requirements of interchangeable inductive loop detector units. A detector unit used with a sensor loop embedded in the surface of a roadway detects vehicles moving or standing in the detection zone of the sensor loop. The output of the loop detector unit may be used directly to provide an input to a vehicle-actuated traffic CU or provide inputs to traffic-responsive control and surveillance systems. Loop detectors generate outputs indicative of vehicles passing through the sensor loop zone of detection. This output may be used for counting (volume) or for detecting presence time representative of the time that vehicles are in the sensor loop zone of detection (occupancy), or both.

6.5.1 Loop Detector Definitions

6.5.1.1 VEHICLE DETECTOR SYSTEM

A system for indicating the presence or passage of vehicles.

6.5.1.2 LOOP DETECTOR SYSTEM

A vehicle detector system that senses a decrease in inductance of its sensor loop(s) during the passage or presence of a vehicle in the zone of detection of the sensor loop(s).

6.5.1.3 SENSOR LOOP

An electrical conductor arranged to encompass a portion of roadway to provide a zone of detection and designed such that the passage or presence of a vehicle in the zone causes a decrease in the inductance of the loop that can be sensed for detection purposes.

6.5.1.4 ZONE OF DETECTION

That area of the roadway within which a vehicle is detected by a vehicle detector system.

6.5.1.5 LOOP DETECTOR UNIT

An electronic device which is capable of energizing the sensor loop(s), of monitoring the sensor loop(s) inductance, and of responding to a predetermined decrease in inductance with an output which indicates the passage or presence of vehicles in the zone of detection.

6.5.1.6 CHANNEL

Electronic circuitry which functions as a loop detector unit.

6.5.1.7 LEAD-IN CABLE

The electrical cable which serves to connect the sensor loop(s) to the input of the loop detector unit.

6.5.1.8 DETECTOR MODE

A term used to describe the duration and conditions of the occurrence of a detector output.

6.5.1.9 CROSSTALK

The adverse interaction of any channel of a detector unit with any other detector channel.

6.5.2 Functional Standards

6.5.2.1 OPERATION

The loop detector unit defined and described in this standard shall respond to changes in the inductance of the sensor loop/lead-in combination(s) connected to its loop input terminals. It shall develop a detection output when there is a sufficiently large decrease in the magnitude of the connected inductance.

The sensor loop(s) connected to the detector unit input terminals shall be located at the intended zone(s) of detection. The sensor loop(s) shall be connected to the detector unit by means of lead-in cable.

The sensor loop(s) shall be so configured that the presence of a vehicle in each zone of detection causes a sufficient decrease in inductance to cause an output response from the detector unit.

6.5.2.2 CONFIGURATIONS AND DIMENSIONS

6.5.2.2.1 Configurations

This standard covers detector unit configurations shown in Table 6.5-1.

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Table 6.5-1
DETECTOR UNIT TYPES

Rack Mount Detector Type	NEMA Detector Designations	Delay/Extension Timing
2 Channel	Type A	None
4 Channel	Type B	None
2 Channel	Type C	Included
4 Channel	Type D	Included

Each channel shall be provided with independent loop input terminals and shall deliver detection information on independent output terminals.

6.5.2.2.2 Dimensions

1. Two-channel card rack units shall be 28.96 mm max W x 114.30 mm H x 117.8 mm D (1.14 inches max. W x 4.5 inches H x 7.00 inches D), excluding the handle as shown in Figure 6.5-1.
2. Four-channel card rack units shall be 59.44 mm (2.34") max. W x 114.3 mm (4.5") H x 177.8 mm (7.00") D, excluding the handle as shown in Figure 6.5-2.

6.5.2.3 ACCESSIBILITY

The detector unit shall be easily disassembled to gain access for maintenance. When thus disassembled, the detector unit shall be operational for trouble shooting.

6.5.2.4 MATERIAL AND CONSTRUCTION OF RIGID PRINTED CIRCUIT ASSEMBLIES

6.5.2.4.1 Materials

All printed circuit boards shall be per Section 3.2.3.1.

6.5.2.4.2 Component Identification

All components shall be identified per Section 3.2.3.3.

6.5.2.5 ENVIRONMENTAL REQUIREMENTS

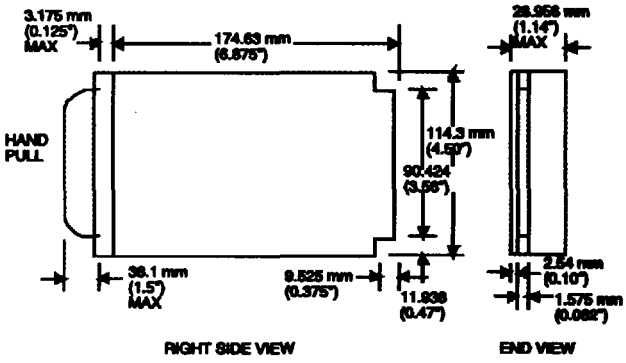
Loop detector units shall operate in accordance with requirements listed herein under the following environmental conditions.

6.5.2.5.1 VOLTAGE, DC SUPPLY

1. Voltage Range—The voltage range shall be 10.8 VDC minimum to 26.5 VDC maximum.
2. Ripple—The maximum supply ripple shall be 500 millivolts peak to peak.

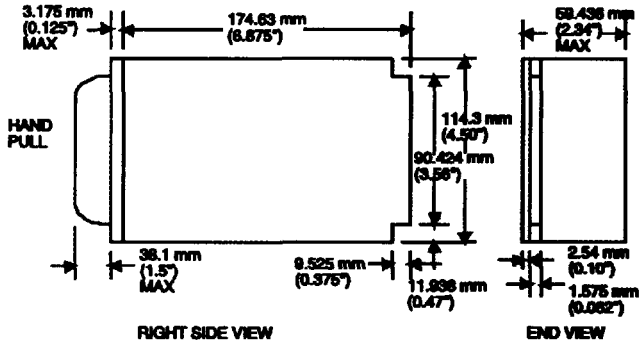
6.5.2.5.2 Temperature and Humidity

Temperature and humidity shall be in accordance with 2.1.5.



Not to Scale
All dimensions in metric
±0.020 Tolerance (where applicable)

Figure 6.5-1
TWO CHANNEL CARD RACK UNIT



Not to Scale
All dimension in metric
±0.020 Tolerance (where applicable)

Figure 6.5-2
FOUR CHANNEL CARD RACK UNIT

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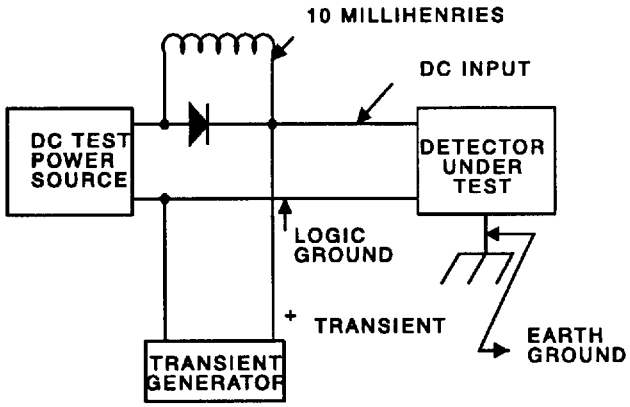
6.5.2.5.3 Transients, DC Powered Units

Loop detector units shall operate normally when the test impulse described in 2.1.7 is applied as follows:

1. Between **Logic Ground** and the DC Supply power input. The test setup shown in Figure 6.5-3 shall be used for this test.
2. Across the output terminals of each channel while in both the detect and non-detect condition.
3. Between **Logic Ground** and the control inputs.

Detector loop inputs are specifically excluded from this test.



TEST CONDITIONS:

1. The transient generator is described in 2.1.7.
2. The input voltage shall be 10.8 to 26.5 volts DC measured at the input terminal to the loop detector unit under test.
3. The DC power source must be capable of supplying at least 50 milliamperes per channel.
4. When testing for the reverse polarity transient, the diode shown shall be reversed.

Figure 6.5-3
TEST CONFIGURATIONS

6.5.2.5.4 Transients, Loop Detector Input Terminals

The loop detector unit shall be capable of withstanding the eight nondestructive transient tests described in Figure 6.5-4. Each test shall be repeated 10 times with the loop detector unit operating from its normal power source. The time between repetitions shall not exceed 10 seconds.

The energy source shall be a capacitor, oil filled, 10 microfarads ± 5 percent, internal surge impedance less than 1 ohm connected in accordance with Figure 6.5-4. The voltage on the capacitor shall be adjusted as described herein. The test push button shall be activated for at least one second for each of the eighty test repetitions.

After the foregoing tests, the loop detector unit shall operate normally.

6.5.2.5.4.1 Test Numbers 1 and 5. The loop detector unit shall withstand the discharge of a 10 microfarad capacitor charged to ± 1000 volts applied directly across the loop detector unit sensor loop input pins with no sensor loop load present.

6.5.2.5.4.2 Test Numbers 2, 3, 4, 6, 7, and 8. The loop detector unit shall withstand the discharge of a 10 microfarad capacitor charged to ± 2000 volts applied directly across either the loop detector unit sensor loop input pins or from either side of the sensor loop input pins to equipment ground. The loop detector unit sensor loop input pins shall have a dummy resistive load attached equal to 5.0 ohms + 10 percent.

6.5.2.5.5 Vibration

The loop detector unit shall maintain both its physical integrity and operating characteristics after being subjected to the vibration test in 3.13.8. This test shall be run at nominal voltage and room environmental conditions.

6.5.2.5.6 Shock

The loop detector unit shall suffer neither permanent mechanical deformation nor any damage which renders it permanently inoperable after being subjected to the shock test described in 3.13.9.

This test shall be run at room environmental conditions without power applied to the unit.

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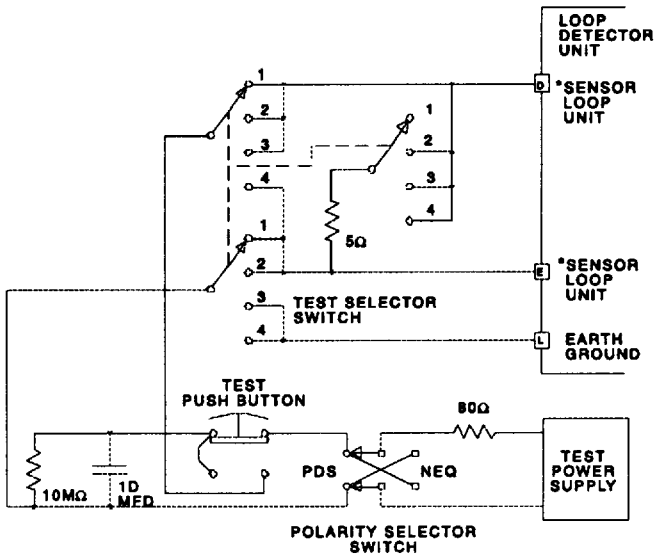

TRANSIENT TEST CONFIGURATIONS

Test Number	Test Selector Position	Power Supply Setting +/- 5%	Polarity Selector	Load Across Detector Input	Tested Inputs
1	1	1000	Positive	None	D to E
2	2	2000	Positive	5 Ohms	D to E
3	3	2000	Positive	5 Ohms	D to L
4	4	2000	Positive	5 Ohms	E to L
5	1	1000	Negative	None	D to E
6	2	2000	Negative	5 Ohms	D to E
7	3	2000	Negative	5 Ohms	D to L
8	4	2000	Negative	5 Ohms	E to L

* The pin desgnations shown are for Channel 1. Similar tests shall be performed on all channels (i.e., pin pairs J and K, P and R, and U and V, respectively and as applicable) of the loop detector unit.

Figure 6.5-4
LOOP INPUT TERMINAL TRANSIENT TESTS

6.5.2.6 POWER INPUTS

6.5.2.6.1 Detector DC Supply Voltage

This input supplies power. The current consumption shall not exceed 50 milliamperes per channel. The return for this input is **Logic Ground** as described in 6.5.2.7. This input shall not be connected within the unit to any loop input. The input shall draw a surge current not to exceed 5 amps at the time of power application to the input. The detector shall not be damaged by insertion to or removal from a powered detector rack.

6.5.2.6.2 Low Supply Voltage Automatic Reset

A **Reset** condition shall be activated anytime the input DC supply voltage falls below that which is required for operation, as defined in this standard.

A **Reset** condition shall not be activated when the DC Supply Input falls below 10 volts for less than 0.25 milliseconds.

6.5.2.7 LOGIC GROUND

This input is the return for the detector DC Supply input. This point shall not be connected within the unit to AC **Neutral, Earth Ground,** or to any loop input terminal.

6.5.2.8 EARTH GROUND

The loop detector unit shall have a terminal for connection to the chassis of the unit. This input shall not be connected to **Logic Ground**, AC- (neutral), or to any other point within the unit, except that it shall be permissible to use this input as a return for transient protection devices.

If the unit has a metallic case or front panel, the case and/or front panel shall be connected to **Earth Ground.**

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6.5.2.9 DC CONTROL INPUTS

Control inputs shall have the following characteristics as measured from **Logic Ground**.

6.5.2.9.1 "Low" or Active State

A voltage between 0 and 8 volts shall be considered the **Low** or active state.

6.5.2.9.2 "High" or Inactive State

A voltage greater than 16 volts shall be considered the **High** or inactive state.

6.5.2.9.3 Transition Voltage Zone Of Input Circuitry

Transition zone of input circuitry from **Low** state to **High** state and vice versa shall occur between 8 and 16 volts.

6.5.2.9.4 External Transition Time

External transition from **Low** state to high state and vice versa shall be accomplished within 0.1 milliseconds.

6.5.2.9.5 Maximum Current

Over the voltage range 0 to 26 volts DC, the maximum current "in" or "out" of any input control terminal shall be less than 10 milliamperes. The input circuitry shall be returned to the detector DC supply in such a manner that the removal of all connections to the input shall allow the voltage at the input terminal to rise to the Detector DC supply voltage.

6.5.2.9.6 Signal Recognition

Any input signal (including external Reset, Pin C) shall respond as defined in paragraph 3.3.5.1.3.

All channels shall remain in a RESET condition while Pin C is held in an Active State (low) voltage.

6.5.2.9.7 Activation of Delay/Extension Feature

The application of a **Low** state voltage to a **Delay/Extension** input shall function to inhibit the delay timing function and/or enable the extend timing function.

This input is provided for downward compatibility. (Authorized Engineering Information)

6.5.2.9.8 Activation of Detector Address Feature

The application of a **Low** state voltage to a **Detector Address** input shall activate the detector address feature. Three address input pins shall provide for a maximum of 8 hard wired addresses.

6.5.2.10 LOOP INPUTS

Two loop input terminals shall be provided for each sensor channel. These inputs shall be isolated (resistance $> 10^6$ and breakdown voltage 1000 VRMS) from logic ground, AC neutral, and the control input and output circuits.

6.5.2.11 LOOP/LEAD IN ELECTRICAL PROPERTIES

Each channel of the detector unit shall function in accordance with the specific requirements of this standard and in addition shall operate without significant degradation with any sensor loop/lead-in combination which exhibits the following electrical properties as measured at the detector unit terminals of the lead-in:

1. Inductance at 50 KHz—50 to 1000 microhenries.
2. Q at 50 KHz—greater than 5.
3. Resistance to earth ground—greater than 1 megohm.
4. Field installation practices or detector unit design may require grounding the shield of the loop lead-in cable. Such grounding should be in accordance with the detector manufacturer's recommendation.

6.5.2.12 TEST LOOP CONFIGURATIONS

Sensor loop and lead-in combinations used to verify the performance requirements of this standard shall consist of the following combinations of 1.828 m x 1.828 m (6 ft. x 6 ft) three turn loops and shielded lead-in cable as illustrated in Figure 6.5-5.

1. Single-loop 1.828 m x 1.828 m (6 ft. by 6 ft.), three turns, with 30.48 m (100 ft.) of lead-in (80–105 microhenries).
2. Single-loop 1.828 m x 1.828 m (6 ft. by 6 ft.), three turns, with 304.8 m (1,000 ft.) of lead-in (260–320 microhenries).
3. Four loops 1.828 m x 1.828 m (6 ft. by 6 ft.), three turns, in a row in the direction of travel and separated by 2.743 m (9 feet), series/parallel connected with 76.0 m (250 ft.) of lead-in (100–140 microhenries).

6.5.2.13 TEST VEHICLE DEFINITION

Detector units shall detect all vehicles which ordinarily traverse the public streets and highways and which are comprised of sufficient conductive material suitably located to permit recognition and response by the detector system.

Vehicles are classified by this standard in accordance with the reduction in inductance resulting when they are centered in the single 1.828 m x 1.828 m (6 ft. x 6 ft.), three turn-test loop with 30.48 (100 feet) of lead-in.

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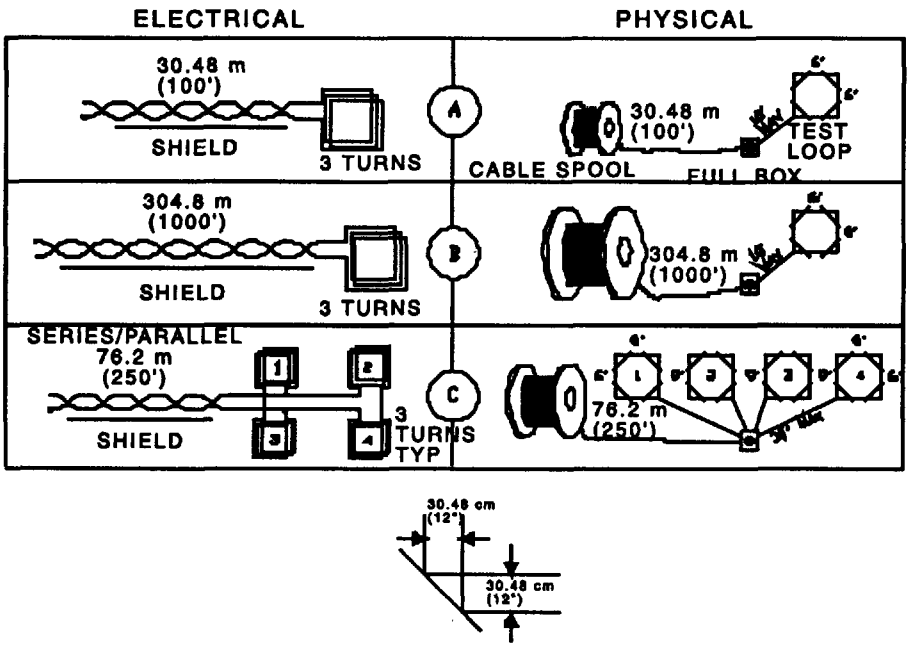

Figure 6.5-5
TEST LOOP CONFIGURATIONS

Construction—Loop dimension tolerances shall be ±50.8 mm (2 inches). Connections shall be soldered and waterproofed. Loops shall be installed in a nonreinforced pavement and located at least 0.914 m (3 feet) from any conductive material. Lead-in cable shall be spooled. Loop leads shall exit at one corner of the loop structures. All loop corners shall be chamfered 0.305m (12 inches).

Loop Wire—Each loop shall be three turns of AWG #14 crosslinked polyethylene insulated, stranded copper wire, such as IMSA (International Municipal Signal Association) Specification 51-3, 1984, or equivalent. Loop inductance shall be between 60–80 microhenries.

Lead-in Wire—The lead-in wire shall be AWG #14 twisted pair, aluminum polyester shield, polyethylene insulation, polyethylene jacket, inductance between 20 uH and 24 uH per 30.48 m (100 feet), such as IMSA Specification 50-2, 1984, or equivalent. For standardized test purposes, the shield shall be insulated from ground.

Field installation practices or detector unit design may require grounding the shield of the loop lead-in cable. Such grounding should be in accordance with the detector manufacturer's recommendation. (Authorized Engineering Information)

Sawslot—The conductors shall be placed at the bottom of a 38.1 mm ±6.35 mm (1-1/2" ± 1/4 inch) deep by 6.35 mm (1/4 inch) wide sawslot. Pavement sawslot shall be filled with a suitable epoxy or equivalent sealant.

These minimum reductions are as follows:

Class 1: 0.13 percent (dL/L) or 0.12 microhenries (dL) inductance change with a single 1.83 m x 1.83 m (6 ft x 6 ft), three turn loop, with 30.48 m (100 ft) lead-in (small motorcycle).

Class 2: 0.32 percent (dL/L) or 0.3 microhenries (dL) inductance change with a single 1.83 m x 1.83 m (6 ft x 6 ft), three turn loop, with 30.48 m (100 ft) lead-in (large motorcycle).

Class 3: 3.2 percent (dL/L) or 3.0 microhenries (dL) inductance change with a single 1.83 m x 1.83 m (6 ft x 6 ft), three turn loop, with 30.48 m (100 ft) lead-in (automobile).

The maximum reduction caused by a class three vehicle shall be 5.4 percent (dL/L) or 5 microhenries (dL) inductance change with a single 1.83 m x 1.83 m (6 ft x 6 ft), three turn loop with 30.48 m (100 ft) lead-in.

6.5.2.14 SENSITIVITY

The detector unit shall be capable of detecting any of the vehicles defined in 6.5.2.13 on any of the test loops defined in 6.5.2.12.

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6.5.2.15 SENSITIVITY CONTROL

When detecting test vehicles as described in 6.5.2.13 and operating on any of the test loop configurations described in 6.5.2.12, each channel of the detector unit shall include means to adjust the sensitivity such that it shall not produce an output when the nearest point of any test vehicle of 6.5.2.13 is 0.914 m (36 inches) or more outside the loop(s) perimeter. A minimum of three sensitivity selections shall be provided for each detection channel.

6.5.2.16 APPROACH SPEED

The detector unit shall detect any vehicle described in 6.5.2.13 over any of the single loops described in 6.5.2.12 traveling within the speed range of 8.045 km to 128.72 km (5 to 80 miles) per hour.

The detector unit shall detect any vehicle described in 6.5.2.13 over all of the loops of the four loop configurations described in 6.5.2.12 traveling within the speed range of 8.045 km to 64.36 km (5 to 40 miles) per hour.

All channels of a multichannel detector shall be operating at the same sensitivity and connected to equivalent inductances for the purpose of these tests.

6.5.2.17 MODES OF OPERATION

Each detector channel shall be capable of functioning in the following two front panel selectable modes:

6.5.2.17.1 Presence

When a Class 2 vehicle defined in 6.5.2.13, or larger vehicle occupies the center of any test loops described in 6.5.2.12, the detector unit shall be capable of maintaining a detection output for a minimum of 3 minutes.

6.5.2.17.2 Pulse

A detection output between 100 and 150 milliseconds shall be initiated when a vehicle enters the sensor loop zone of detection.

If this vehicle remains in the zone of detection, the detector unit shall become responsive within a maximum of 3 seconds to additional test vehicles entering the zone of detection. The detector unit shall produce one and only one output pulse for a test vehicle traveling at 16.09 km (10 miles) per hour across the zone of detection of the single sensor loops defined in 6.5.2.12.

6.5.2.18 RECOVERY FROM SUSTAINED OCCUPANCY

When operating in the presence mode, and following an occupancy of any duration, the detector unit shall recover to normal operation with at least 90 percent of its selected sensitivity within one second after the zone of detection is vacated.

6.5.2.19 RESPONSE TIME

When operating in the presence mode, the detector unit shall be capable of being set to produce an output in response to a step decrease in inductance equivalent to the minimum decrease from a class one vehicle as defined in 6.5.2.13 within not more than 100 milliseconds when tested on either of the single loop test configurations described in 6.5.2.12. In response to step return to the original inductance, the detector unit shall terminate its output within no more than 100 milliseconds.

6.5.2.19.1 Variation in Response Time

The difference between the minimum measured response time and the maximum measured response time for input changes in either direction, over any number of tests, to an input change equivalent to a Class 1 vehicle shall not exceed 10 milliseconds per channel multiplied by the number of active channels. The detector must be set to the proper sensitivity to detect a Class 1 vehicle.

The difference between the minimum measured response time and the maximum measured response time for input changes in either direction, over any number of tests, to an input change equivalent to a Class 3 vehicle shall not exceed 5 milliseconds per channel multiplied by the number of active channels. The detector must be set to the proper sensitivity to detect a Class 3 vehicle.

All channels of a multichannel detector unit which are on shall be operating at the same sensitivity and connected to equivalent inductances for the purpose of these tests.

For certain specific surveillance applications involving vehicle speeds in excess of 72.405 km (45 miles) per hour, a more precise response time will be required. (Authorized Engineering Information)

6.5.2.20 TUNING

Each detector channel shall include means for accommodating the range of sensor loop/lead-in inductance.

The unit shall tune automatically upon the application of power. It shall operate with at least 90 percent of its selected sensitivity within 2 seconds after application of power.

6.5.2.21 Self-Tracking

The detector unit shall automatically accommodate those after-tuning changes in the loop/lead-in electrical characteristics as might reasonably be expected to occur in undamaged loops, properly installed in sound pavement and exhibiting the electrical properties outlined in 6.5.2.11, without producing a false output or change in sensitivity.

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6.5.2.22 RECOVERY FROM RESET

After any reset the detector shall operate with at least 90 percent of its selected sensitivity, within 2 seconds after the removal of the reset condition.

6.5.2.23 CROSSTALK AVOIDANCE

Each detector channel shall include means to prevent that channel from adversely interacting with any other channel. The means to prevent such interaction shall be either inherent, automatic, or manual switch.

6.5.2.24 DELAY/EXTENSION

Each channel of a unit with delay/extension shall have at least three modes of operation—delay, extension, and normal (neither delay nor extension). Channels 1 and 2 of four-channel detector units shall be the channels to include the delay/extension feature. Delay and extension timing shall be setable on a per channel basis with the timing programmed independently.

6.5.2.24.1 Delay

When selected, the output is delayed for the time set. If the vehicle departs before the time set, an output does not occur and the timer is reset. If a vehicle is present and the delay timer is active, when the delay inhibit is applied, the output shall become active. This delay timing is controlled by the **Delay/Extension** input defined in 6.5.2.9.7. See Figure 6.5-6.

The delay time shall be adjustable over the range from 0 to 30 seconds. The setability shall be within one second in the 0 to 15 second range and within two seconds in the 16 to 30 second range. The accuracy shall be + 1/2 second or ± 5 percent of the setting, whichever is greater. When the **Delay/Extension** input is active, the delay shall be zero (0 to 0.1 second).

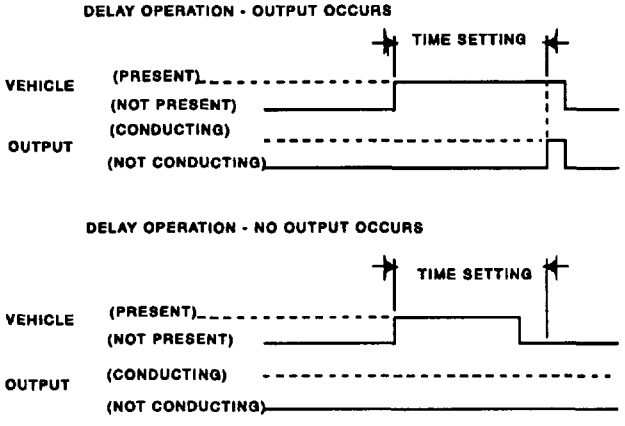

Figure 6.5-6
DELAY OPERATION

6.5.2.24.2 Extension

When selected, the output is extended after the vehicle departs the zone of detection for the time set. If a new vehicle arrives before the extension timer times out, the timer is reset, the output is maintained, and the timer resumes timing when the vehicle departs. See Figure 6.5-7. This extension timing is controlled by the **Delay/Extension** input defined in 6.5.2.9.7.

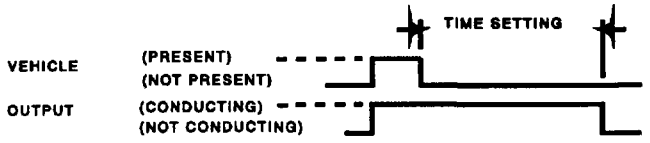

Figure 6.5-7
EXTENSION OPERATION

The extension time shall be adjustable in the range from 0 to 7-1/2 seconds. The setability shall be within 1/2 second. The accuracy shall be ± 1/2 second. When the **Delay/Extension** input is inactive, the extension shall be zero (0 to 0.1 second).

6.5.2.25 CONTROLS AND INDICATORS

All controls and indicators necessary for the operation of the detector unit shall be located on the front panel of the unit except as noted below. Multiple functions combined in a single control shall be permitted. The controls and indicators shall include, but are not limited to:

1. Output Indicator—Means to visually indicate the output state of each channel. Each channel shall have a separate indicator.
2. Sensitivity Control—Means to permit selection of the sensitivity of each channel as described in 6.5.2.15.
3. Reset—A control which unconditionally causes the detector or detection channel to retune to a non-vehicle present condition.
4. Mode Selector—Shall provide for selection of pulse or presence mode operation of each channel. Card mounting of this control shall be permitted where actuation does not require disassembly.

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5. Crosstalk Control—As required, shall provide means to prevent interaction of channels as described in 6.5.2.23.
6. Delay/Extension Selection Control—The type C and D detectors shall have either a control or combination of controls to allow for the selection of one of at least three operating modes—delay, extension, and normal (neither delay nor extension). It shall be permissible to have the normal mode selected by either setting a three position selector switch to the normal position or setting the delay/extension timing control to zero. Card mounting of the control(s) shall be permitted where actuation does not require disassembly.
7. Delay/Extension Timing Control—The type C and D detectors shall provide a means to permit setting of the time duration of the delay/extension period for each channel as described in 6.5.2.24. Card mounting of this control shall be permitted where actuation does not require disassembly.
8. Enable/disable—Means to turn on or off a channel or number of channels on a detector unit.

6.5.2.26 OUTPUTS

The output interface of each channel shall be an independent isolated solid state output. Each output device shall have the following characteristics:

6.5.2.26.1 Solid State Channel Detection Outputs

1. Output Solid State Device—Conducting indicates detection output. Also shall be conducting if the loop circuit is in a failed state.(i.e. open loop or shorted loop).
2. DC Supply Voltage Failure Condition—Output device is conductive, when terminated to a NEMA defined input, indicating a detection output condition.
3. Output Circuit Isolation—The isolation between each output device terminal pair and all other terminals shall exceed:
   a. Resistance 10^6 ohms
   b. Breakdown 1000 V rms
4. Output Rating—The output shall conduct a minimum of 20 milliamperes with a maximum 3.5 volt drop across the output terminals in the conducting state. The output shall conduct a maximum of 500 microamperes with any voltage between 0 and 26 VDC applied across the output terminals in the non-conductive state.
5. Transition Time—When switching to or from a steady state current in the range of 2.4 to 20 milliamperes, the transition time from 8 to 16 volts and vice versa shall be 0.1 milliseconds or less. The circuit(s) to which the output is connected is defined in 3.3.5.1.3.
6. Maximum Voltage—Hold off 30 VDC minimum under non-detect conditions.

6.5.2.26.2 Channel Status outputs

Each detector channel shall provide a channel status output. The channel status output shall be a solid state device with the following characteristics:

1. Output Solid State Device—Conducting indicates channel is operating properly.
2. DC Supply Voltage Failure Condition—Output device is nonconductive, indicating a fault condition.
3. Status Outputs shall be referenced to logic ground.
4. Output Rating—The output shall conduct a minimum of 20 milliamperes with a maximum 3.5 volt drop across the output terminals in the conducting state. The output shall conduct a maximum of 100 microamperes with any voltage between 0 and 26 VDC applied across the output terminals in the non-conductive state.
5. Transition Time—When switching to or from a steady state current in the range of 2.4 to 20 milliamperes, the transition time from 8 to 16 volts and vice versa shall be 0.1 milliseconds or less. The circuit(s) to which the output is connected is defined in 3.3.5.1.3
6. Maximum Voltage—When in the non-conducting state, the output shall tolerate a voltage as high as 30 VDC without damage.

6.5.2.26.3 Channel Status Reporting

The Channel Status Output shall provide for the communication of eight distinct status states as defined below:

1. Normal operation (detector and loop ok).
2. Detector failure (watch dog timeout).
3. Open loop (An open loop may be reported when the terminal inductance is >1000 microheneries and <2500 microhenries. The open loop shall be reported when the terminal inductance is >2500 microhenries).
4. Shorted loop (A shorted loop may be reported when the terminal inductance is <50 microhenries and >20 microhenries. A shorted loop shall be reported when the terminal inductance is <20 microhenries).
5. Excessive inductance change (± 25%)
6. Reserved
7. Reserved
8. Reserved

Pulse width modulation shall be utilized to encode the eight possible states as described below:

1. Continuous "low" or **On** state.
2. Continuous "high" or **Off** state.
3. 50 milliseconds "**Off**"
4. 100 milliseconds "**Off**"
5. 150 milliseconds "**Off**"
6. 200 milliseconds "**Off**"
7. 250 milliseconds "**Off**"
8. 300 milliseconds "**Off**"

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The tolerance for all times listed above shall be ± 10 milliseconds, the on time between pulses shall be 50 milliseconds ± 10 millesconds.

The channel status output shall be in State 1 during reset. If the original fail condition has been cleared and the detector resumes normal operation, the fault output will reset to State 1.

The channel status output shall reflect the current fault status of the channel, (i.e., the fault status shall be self clearing in the event that a fault condition clears).

The last channel failure status shall be stored in memory for future reference. Enunciation of the last failure status shall be accomplished through the use of the front panel indicators. If power is removed or the reset is activated, the last channel status information shall be cleared.

The particular method employed to enunciate past failure status is not specified and will be manufacturer specific. (Authorized Engineering Information)

6.5.2.27 ELECTRICAL CONNECTIONS

6.5.2.27.1 Connector Description

Two and four channel card rack units shall mate with a 44 terminal, double row, 3.2 mm (0.156 inch) contact spacing, CinchJones card edge connection 50-44A-30M, or equivalent.

6.5.2.27.2 Connector Terminations

Input-output connector pin terminations shall be as shown in Table 6.5-8.

6.5.2.27.3 Type A Two Channel Without Delay / Extension timing

The following pins shall be inactive: P, R, S, T, U, V, Y, Z, 1, 2, 13, 14, 16, 17, 18, and 22.

6.5.2.27.4 Type B Four Channel Without Delay / Extension timing

The following pins shall be inactive: 1 and 2.

6.5.2.27.5 Type C Two Channel With Delay / Extension timing

The following pins shall be inactive: P, R, S, T, U, V, Y, Z, 13, 14, 16, 17, 18, and 22.

Table 6.5-8
CONNECTOR TERMINATIONS

Pin A	Logic Ground	1. Delay/Extension input, Ch. 1
Pin B	Detector DC Supply	2. Delay/Extension input, Ch. 2
Pin C	External Reset	3. Spare
Pin D	Loop Input, Ch 1	4. Redundant Loop Input, Ch 1 (optional)
Pin E	Loop Input, Ch 1	5. Redundant Loop Input, Ch 1 (optional)
Pin F	Output, Ch 1(+)	6. Detector address Bit #0 (reserved)
Pin H	Output, Ch 1(-)	7. Status output Ch. 1
Pin J	Loop Input, Ch 2	8. Redundant Loop Input, Ch 2 (optional)
Pin K	Loop Input, Ch 2	9. Redundant Loop Input, Ch 2 (optional)
Pin L	Chassis Ground	10. Detector address Bit #1 (reserved)
Pin M	Reserved (AC neutral)	11. Reserved (AC neutral)
Pin N	Reserved (AC line)	12. Reserved (AC line)
Pin P	Loop Input, Ch 3	13. Redundant Loop Input, Ch 3 (optional)
Pin R	Loop Input, Ch 3	14. Redundant Loop Input, Ch 3 (optional)
Pin S	Output, Ch 3(+)	15. Detector address Bit #2 (reserved)
Pin T	Output, Ch 3(-)	16. Status output Ch. 3
Pin U	Loop Input, Ch 4	17. Redundant Loop Input, Ch 4 (optional)
Pin V	Loop Input, Ch 4	18.Redundant Loop Input, Ch 4 (optional)
Pin W	Output, Ch 2(+)	19. Data transmit (reserved)
Pin X	Output, Ch 2(-)	20. Status output Ch. 2
Pin Y	Output, Ch 4(+)	21. Data receive (reserved)
Pin Z	Output, Ch 4(-)	22. Status output Ch. 4

Polarization keys shall be located at three positions:
1. Between B/2 and C/3
2. Between M/11 and N/12
3. Between E/5 and F/6

Pins 6, 10, and 15 are reserved for future address pins. When the detector is installed it will be assigned an address associated with the detector position in the detector rack.

Pins 19 and 21 are reserved for future enhanced communication with the detector. Communication format and data to be exchanged have not been defined at this time. (Authorized Engineering Information)

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SECTION 7
CABINETS

This section defines the physical and functional requirements of cabinets which fully conform to this standard publication.

7.1 DEFINITIONS

These definitions define the nomenclature frequently used in this part of the Standard Publication.

The abbreviations used in this section are defined as follows:

ASTM—American Society for Testing and Materials

7.2 Materials

Cabinets shall be of either a ferrous material or of an aluminum alloy.

7.2.1 Cabinets of Ferrous Material

Cabinets shall be fabricated of carbon sheet steel having a minimum thickness of 1.85 millimeters (0.073 inch), minimum. The material shall meet the requirements in ASTM Specification No. A-245-48T (paragraph 4) or have a heat treated zinc coating of 0.015 millimeters (0.0006 inch) minimum thickness on both sides. All exterior seams shall meet the requirements for Type 4 enclosures according to NEMA Standards Publication 250-1991.

7.2.2 Cabinets of Aluminum Alloy

Cabinets shall be fabricated of either sheet aluminum or cast aluminum.

7.2.2.1 SHEET ALUMINUM

Cabinets shall he fabricated from 3.175 millimeters (0.125 inch) minimum thickness aluminum alloy sheet meeting the requirements in ASTM Specification No. 5052-H32 or equivalent. All exterior seams shall meet the requirements for Type 4 enclosures according to NEMA Standards Publication 250-1991.

7.2.2.2 CAST ALUMINUM

Cabinets shall be fabricated from aluminum alloy meeting the requirements in ASTM Specification No. 356-75 or equivalent. Flat cast surfaces exceeding 12 inches in both directions shall have a thickness of 6.35 millimeters (0.25 inch), minimum. Flat cast surfaces not exceeding 30.48 centimeters (12 inches) in both directions shall have a thickness of 4.75 millimeters (0.187 inch).

7.3 Cabinet Dimensions

The outline dimensions of cabinets shall be as shown in Table 7.3-1.

Table 7.3-1
OUTLINE DIMENSIONS

Size	Width	Height	Depth
1	40.64 (16)	60.96 (24)	30.48 (12)
2	50.80 (20)	81.28 (32)	35.56 (14)
3	60.96 (24)	101.60 (40)	38.10 (15)
4	60.96 (24)	116.84 (46)	40.64 (16)
5	76.20 (30)	121.92 (48)	40.64 (16)
6	111.76 (44)	132.08 (52)	60.96 (24)
7	111.76 (44)	182.88 (72)	60.96 (24)

All dimensions are in centimeters (inches). Tolerance on all dimensions is +10%/-0%. These are outside dimensions exclusive of hinges, handle, overhangs, vents, and adapters. Cabinet heights are measured to the lowest point of the top surface of the cabinet.

7.4 Top Surface Construction

The cabinet shall be manufactured so as to prevent the accumulation of water on its top surface.

7.5 Doors

7.5.1 Main Cabinet Door

The cabinet shall have a hinged main door which permits access to all equipment within the cabinet and visual inspection of all indications and controls. Doors shall be hinged on the right side of the cabinet as viewed from the outside facing the cabinet door opening.

7.5.2 Hinges

Door hinges, pins, and bolts shall be made of stainless steel; except that hinges on aluminum cabinets may be aluminum with stainless steel hinge pins. The hinge pins and mounting shall be tamperproof.

7.5.3 Door Stop

In Size 3 and larger cabinets, the cabinet door shall be provided with a door stop which holds the door open at the 90° (±10°) and 180° (±10°) positions. A means shall be provided to minimize the accidental release of the door stop. The stop-and-catch arrangement shall be capable of holding the door open at 90° (±10°) with a load of 73.2 Kilograms per square meter (15 pounds per square foot) applied uniformly over the face of the door.

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7.5.4 Latches and Locking Mechanism

7.5.4.1 LATCHING

A three-point latch is required on the main door of Size 3, or larger, cabinets. The latching means shall be operable without the use of tools.

7.5.4.2 ROTATION OF HANDLE

The main door handle shall rotate from the locked position such that the handle does not extend beyond the perimeter of the main door at anytime. The operation of the handle shall not interfere with the key, police door, or any other cabinet mechanism or projection.

7.5.4.3 LOCKS

All cabinets shall be provided with a main door lock, Corbin No. 15481RS, or equivalent, constructed of brass or stainless steel which shall operate with a traffic industry conventional No. 2 key, Corbin No. 1R6380, or equivalent. Two keys shall be furnished with each cabinet. When in the locked position, the lock shall prevent the movement of latching mechanism.

7.5.4.4 PROVISIONS FOR PADLOCK

Cabinets with three-point latches shall be provided with a means of externally padlocking the latching mechanism. A lock with a 9.525 millimeter (0.375 inch) diameter shackle shall be accommodated.

7.5.5 Door Opening

The main door opening of all cabinets shall be at least 80 percent of the area of the side which the door closes, exclusive of the area for plenums.

7.5.6 Gasketing

Gasketing shall be provided on all door openings and shall be dust-tight. Gaskets shall be attached with a permanent adhesive bond. The mating surface of the gasketing shall be covered with a silicone lubricant to prevent sticking to the mating surface.

7.5.7 Police Compartment

7.5.7.1 DOOR

A hinged police compartment door shall be provided on the outside face of the main cabinet door. The door shall permit access to a switch panel, but shall not allow access to exposed electrical terminals or other equipment within the cabinet.

7.5.7.2 LOCKS

The police compartment door shall be provided with a lock which can be operated by a police key, Corbin Type Blank No. 04266 or equivalent. Two keys shall be furnished with each cabinet.

7.5.7.3 COMPARTMENT SIZE

The volume of the police panel compartment with the door closed shall be 1147 cubic centimeters (70 cubic inches), minimum. Minimum internal dimensions shall be 12.70 centimeters (5 inches) high, 25.40 centimeters (10 inches) wide and 7.62 centimeters (3 inches) deep.

7.6 Shelves

The cabinet shall be provided with a sufficient number and sizes of substantial metal shelves or brackets to support the controller unit and auxiliary equipment. The equipment and shelves shall be arranged so that it is possible to remove any piece of auxiliary equipment from the cabinet without removing any other piece of auxiliary equipment.

7.6.1 Positioning

Size 3, 4, and 5 cabinets shall have provision for positioning shelves to within 30.48 centimeters (12 inches) of the bottom of the cabinet and to within 20.32 centimeters (8 inches) of the top of the cabinet in increments of not more than 5.08 centimeters (2 inches).

Size 6 and 7 cabinets shall have provisions for positioning shelves within 60.96 centimeters (24 inches) of the bottom of the cabinet and to within 20.32 centimeters (8 inches) of the top of the cabinet in increments of not more than 5.08 centimeters (2 inches).

7.7 Finish and Surface Preparation

7.7.1 Steel Cabinets

7.7.1.1 PREPARATION

The surface of the cabinet shall be suitably prepared prior to painting. If the surface is damaged, the affected area shall be repaired prior to painting.

7.7.1.2 PRIME COAT

If a primer coat is used, at least one application of a suitable primer paint shall be applied to the interior and exterior surfaces of the cabinet. If the primed surface is scratched or damaged, the affected area shall be reprimed prior to the application of the finish coat.

7.7.1.3 INTERIOR SURFACES

At least one application of a suitable exterior grade of paint shall be applied to the interior surfaces of the cabinet.

7.7.1.4 EXTERIOR SURFACES

At least one application of a suitable exterior grade paint shall be applied to the exterior surfaces of the cabinet.

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7.7.2 Aluminum Cabinets

7.7.2.1 PREPARATION: PAINTED CABINETS

The surfaces of the cabinet shall be suitably prepared prior to painting. If the surface is damaged, the affected area shall be repaired prior to painting.

7.7.2.2 PRIME COAT

If a primer paint is used, at least one application of a suitable primer paint shall be applied to the surfaces to be painted. If the primed surface is scratched or damaged, the affected area shall be reprimed prior to the application of the finish coat.

7.7.2.3 INTERIOR SURFACES

If interior surfaces are painted, at least one application of a suitable exterior grade paint shall be applied to the interior surfaces of the cabinet.

7.7.2.4 EXTERIOR SURFACES

At least one application of a suitable exterior grade paint shall be applied to the exterior surfaces of the cabinet.

7.7.3 Unpainted Aluminum Cabinets

Unpainted aluminum cabinets shall be fabricated from mill finish material and shall be cleaned with appropriate methods that will remove oil film, weld black, mill ink marks and render the surface clean, bright, smooth, and non-sticky to the touch.

7.8 Cabinet Mounting

7.8.1 Pole-Mounted Cabinets

Cabinets intended for side of pole mounting shall be provided with the hardware necessary to permit mounting to a 30.48 centimeters (12 inch) outside diameter pole.

7.8.2 Pedestal-Mounted Cabinets

Cabinets intended for pedestal mounting shall be provided with the hardware necessary to permit post top mounting on a 11.43 centimeters (4.5 inch) outside diameter pedestal pole.

7.8.3 Base-Mounted Cabinets

7.8.3.1 SIZES 3, 4, AND 5

When a Size 3, 4, or 5 cabinet is to be base-mounted, either the cabinet or its base adapter shall be constructed so that it can be mounted on the foundation shown in Figure 7.8.3-1.

Anchor bolts should extend 6.35 centimeters ± 1.27 centimeters (2.5 inches ± 0.5 inch) above the plane of the mounting foundation. Conduit should not extend more than 7.62 centimeters (3 inches) above the plane of the mounting foundation (Authorized Engineering Information).

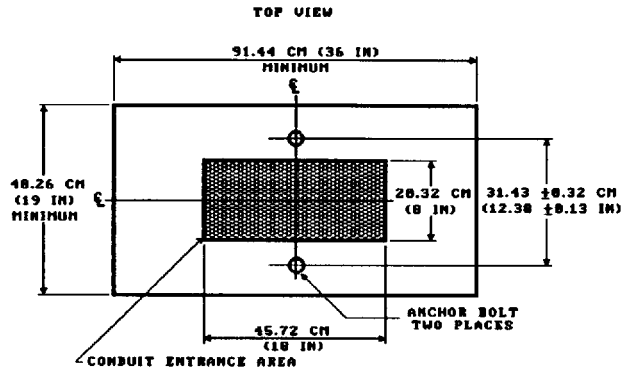

Figure 7.8.3-1
FOUNDATION FOR SIZES 3, 4, AND 5 BASE-MOUNTED CABINETS

7.8.3.2 SIZES 6 AND 7

Size 6 and 7 cabinets shall be so constructed that they can be mounted on the foundation shown in Figure 7.8.3-2.

Anchor bolts should extend 6.35 centimeters ± 1.27 centimeters (2.5 inches ± 0.5 inch) above the plane of the mounting foundation. Conduit should not extend more than 7.62 centimeters (3 inches) above the plane of the mounting foundation (Authorized Engineering Information).

7.8.4 Anchor Bolts

Anchor bolts for base-mounted cabinets shall be 19.05 millimeters (0.75 inch) in diameter, 40.64 centimeters (16 inches) long, with a 90-degree bend with a 5.08 centimeter (2 inch) leg; overall length of 45.72 centimeters (18 inches). The end opposite the leg shall be threaded for at least 7.62 centimeters (3 inches) with a 3/4 UNC-10 thread. Anchor bolts shall be steel with hot-dipped galvanized or zinc plate surface treatment.

Each anchor bolt shall be furnished with two 3/4-10 plated steel nuts and one 1/4-inch plated flat washer.

Two anchor bolts shall be provided for each Size 3, 4, or 5 cabinet intended for base mounting. Four anchor bolts shall be provided for Size 6 and 7 cabinets.

7.9 CABINET VENTILATION

7.9.1 Fan or Cooling System Design

Each cabinet shall be provided with a fan rated at 2.832 cubic meters per minute (100 cubic feet per minute), minimum.

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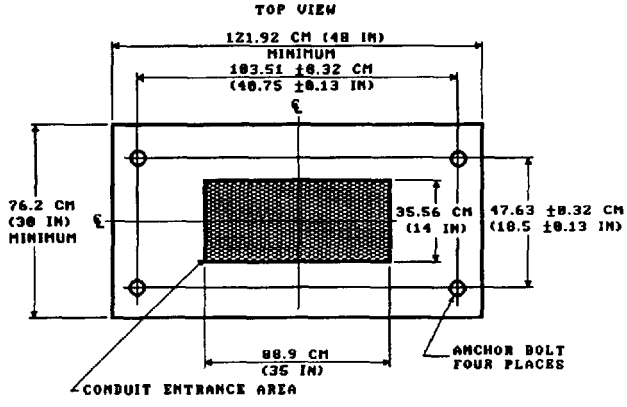

Figure 7.8.3-2
FOUNDATION FOR SIZE 6 AND 7 BASE-MOUNTED CABINETS

7.9.2 Fan or Cooling System Operation

7.9.2.1 OPERATING CONDITIONS

The fan or cooling system shall be capable of operating continuously for a minimum of 6,000 hours in a +50°C (+122°F) environment without the need for after-installation maintenance, excluding filter cleaning or replacement.

7.9.2.2 FAN OR COOLING SYSTEM CONTROLS

Each cabinet shall be provided with a thermostat to control the operation of the fan or cooling system. The thermostat turn-on point shall be manually adjustable from +33°C (+91°F) to +45°C (+113°F), with a differential of not more than +6°C (+11°F) between automatic turn-on and turn-off. The thermostat shall be located on the inside of the top portion of the cabinet not lower than 6 inches from the top of the cabinet.

7.9.2.3 FILTER

Each cabinet shall be provided with a device to filter the incoming air.

Size 1, 2, 3, and 4 cabinets shall have a replaceable filter.

Size 5, 6, and 7 cabinets shall have a replaceable filter with the following dimensions: width—40.64 centimeters (16 inches), height—30.48 centimeters (12 inches), thickness—2.54 centimeters (1 inch).

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SECTION 8
BUS INTERFACE UNIT

8.1 GENERAL

The BIU performs the interface between Port 1 at the CU and the TF and Loop Detector Racks. Its functions include controlling load switch outputs, Detector Resets, and the conditioning and conversion of TF and Loop Detector call inputs for the CU.

8.2 PHYSICAL

8.2.1 Material

All ferrous metal parts shall be protected against corrosion. All materials shall be moisture and fungus resistant.

8.2.2 Printed Circuits

Printed circuits shall meet the requirements of Section 3.2.3.

8.2.3 Dimensions

The BIU shall be 59.436 mm (2.34") W x 114.3 mm (4.50") H x 165.1 mm (6.50") D as illustrated in Figure 8.2-1

The BIU assembly shall slide freely into two card guides, each having a nominal slot width of 1.905 mm (.075 inch) and a maximum slot depth of 3.175 mm (.125 inch). The edges of the BIU assembly shall be clear of protrusions on both sides for an area of 3.175 mm (.125 inch) in height for the entire length of the assembly. The nominal thickness of the edges of the BIU assembly shall be 1.575 mm (.062 inch) ± 0.203 mm (.008 inch).

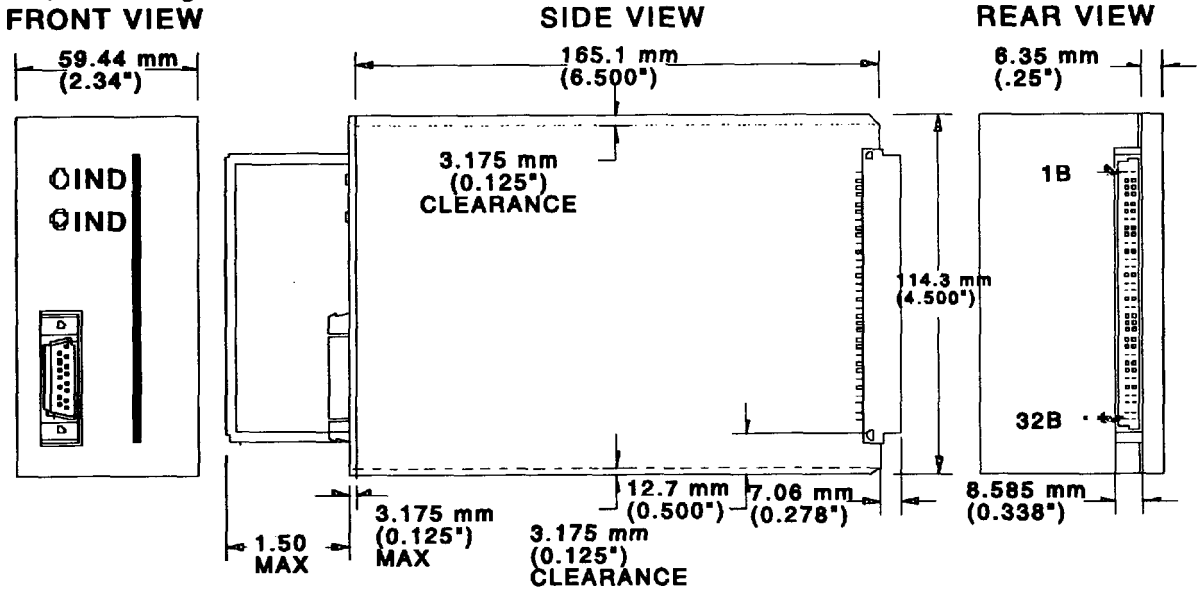
8.3 ENVIRONMENTAL REQUIREMENTS

The BIU shall perform its specified functions under the conditions set forth in Section 2, Environmental Requirements.

8.4 POWER REQUIREMENTS

The BIU shall require a nominal supply voltage of 24 VDC ± 2 VDC. A voltage of 16 VDC or less shall be considered loss of power and a voltage of 18 VDC or more shall be considered adequate for operation. The BIU shall not require more than 200 milliamperes over the voltage range of 16 to 30 VDC, and the power surge shall be limited to a maximum of 1.25 amperes from initial application of DC power.

The BIU shall not be damaged by insertion to or removal from a powered BIU Rack or Detector Rack.



NOTES:
ALL DIMENSIONS ARE IN METRIC
TOLERANCES: X.XX = ± 0.254 mm (.010")
X.XXX = ±0.127 mm (.005")

Figure 8.2-1
BUS INTERFACE UNIT

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8.4.1 Initialization

1. Upon application of DC power, the BIU shall be fully functional within 100 milliseconds, maximum. The initialized state of the BIU shall set all outputs to the 24 volt level.
2. During the loss of DC power to the BIU for 700 milliseconds or less, the BIU shall maintain the state of its outputs.
3. If DC power is restored to the BIU within 700 milliseconds following the loss of DC power, the BIU shall maintain the state of its outputs until they are updated by valid Port 1 activity.
4. Following the loss of DC power to the BIU for 1.5 seconds or greater, the BIU shall turn off all of its outputs and reinitialize all internal operations upon restoration of DC power.
5. Upon detection of loss of power, the BIU shall cease Port 1 Communcations.

8.5 INDICATORS

The BIU shall have two status indicators to represent adequate supply voltage, internal operations, and valid communications.

8.5.1 Power On Indicator

This indicator shall illuminate when the applied DC voltage is considered adequate as described in Section 8.4 and the BIU internal logic is operating properly. This indicator shall be off if either of these conditions are false.

8.5.2 Transmit Indicator

This indicator shall illuminate for a duration not less than 20 milliseconds and not more than 50 milliseconds each time the BIU transmits on its Port 1 output.

8.6 INTERFACE REQUIREMENTS

8.6.1 Port 1 Communications

Defined in Section 3.3.1.

8.6.2 Port 1 Connector

The Port 1 connector shall be a 15 pin metal shell D sub miniature type. The connector shall utilize female contacts with 15 millionths of an inch minimum gold plating in the mating area. The connector shall be equipped with latching blocks. The connector shall intermate with a 15 pin D type connector, Amp Incorporated part number 205206-1 or equivalent, which is equipped with spring latches, Amp Incorporated part number 745012-1, or equivalent.

8.6.2.1 Port 1 Connector Pin Assignments

Pin	Function
1	Rx Data +
2	Logic Ground
3	Rx Clock+
4	Logic Ground
5	Tx Data +
6	Logic Ground
7	Tx Clock +
8	Logic Ground
9	Rx Data -
10	Not Used
11	Rx Clock -
12	Earth Ground
13	Tx Data -
14	RESERVED
15	Tx CLOCK -

NOTE:Tx pins at the BIU = Rx pins at the CU; Rx pins at the BIU = Tx pins at the CU.

8.6.3 Card Rack Connector

The BIU card rack connector shall be a male 64 pin DIN 41612 type B series. The connector shall be centered at the edge of the circuit board and oriented with pin 1 located at the top of the unit. The circuit board edge shall align with the connector per DIN 41612.

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8.6.3.1 CONNECTOR PIN ASSIGNMENTS

Pin	Function
1 a	+24 VDC IN
1 b	+24 VDC IN
2 a	Output 1
2 b	Output 2
3 a	Output 3
3 b	Output 4
4 a	Output 5
4 b	Output 6
5 a	Output 7
5 b	Output 8
6 a	Output 9
6 b	Output 10
7 a	Output 11
7 b	Output 12
8 a	Output 13
8 b	Output 14
9 a	Output 15
9 b	Input/Output 1
10 a	Input/Output 2
10 b	Input/Output 3
11 a	Input/Output 4
11 b	Input/Output 5
12 a	Input/Output 6
12 b	Input/Output 7
13 a	Input/Output 8
13 b	Input/Output 9
14 a	Input/Output 10
14 b	Input/Output 11
15 a	Input/Output 12
15 b	Input/Output 13
16 a	Input/Output 14
16 b	Input/Output 15
17 a	Input/Output 16
17 b	Input/Output 17
18 a	Input/Output 18
18 b	Input/Output 19
19 a	Input/Output 20
19 b	Input/Output 21
20 a	Input/Output 22
20 b	Input/Output 23
21 a	Input/Output 24
21 b	Input 1
22 a	Input 2
22 b	Input 3
23 a	Input 4
23 b	Input 5
24 a	Input 6
24 b	Input 7
25 a	Input 8
25 b	Opto Input 1
26 a	Opto Input 2
26 b	Opto Input 3
27 a	Opto Input 4
27 b	Opto Common
28 a	Address Select 0
28 b	Address Select 1
29 a	Address Select 2
29 b	Address Select 3
30 a	Data Transmit (reserved)
30 b	Data Receive (reserved)
31 a	Earth Ground
31 b	Line Frequency Reference
32 a	Logic Ground
32 b	Logic Ground

8.6.4 Outputs

BIU pins labeled Output (n) and Input/Output (n) shall provide output from the BIU to the TF and Detector Racks as programmed in the respective command frame (Section 3.3.1.4). The ON "low" state for an output shall require a logic 1 bit in the respective Command Frame, and the OFF "high" state for an output shall require a logic 0 bit in the respective Command Frame.

Output characteristics shall be as follows:

1. The Low (operate) voltage shall be between 0 and 4 volts.
2. Current sinking capability in the Low state (TRUE) shall be at least 50 milliamperes.
3. With an external impedance of 100k ohms or greater, the transition from 4 to 16 volts (and vice versa) shall be accomplished within 0.1 millisecond.
4. The High state (FALSE) impedance shall not exceed 11 K ohms to the +24 VDC input to the BIU.
5. Any external steady-state voltage applied to an output terminal shall not exceed +30 volts DC, nor shall it cause flow of more than 3 milliamperes into the terminal, when the output is in the High state.
6. Any valid TRUE output signal, except Load Switch Driver outputs when Dimming is enabled (Section 3.3.1.4), shall dwell in this state for at least 50 milliseconds.
7. For the purpose of synchronizing all outputs of TF BIUs, command frames shall be transferred to the BIU output pins only upon receipt of a type 18 Output Transfer Frame. This Output Transfer Frame is received simultaneously by all BIU's. All TF BIUs shall update their outputs within 20 milliseconds after the receipt of the Output Transfer Frame.

8.6.5 Inputs

Type 138–141 Positive Acknowledge Frames from a BIU shall report logic 0 bits for False (24V) inputs, and shall report logic 1 bits for True (ground) inputs. Opto Inputs 1 through 4 shall report logic 0 bits when inactive, and shall report logic 1 bits when active.

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8.6.5.1 OPTO COMMON

The **Opto Common** input is the common reference pin for four Optically Isolated Inputs.

8.6.5.2 OPTO INPUTS

The **Opto** inputs are intended to provide optical isolation for Pedestrian Detector and Remote Interconnect Inputs. The **Opto** inputs are intended to connect through external 27 K ohm, 1 Watt resistors for 120 VAC operation, and are intended for direct connection to 12 VAC from the cabinet power supply for Pedestrian Detector applications. These inputs may alternatively be used for low-true DC applications when the **Opto Common** pin is connected to the 24 volt supply. (Authorized Engineering Information)

1. The **Opto** inputs shall provide electrical isolation of 10 megohms minimum resistance and 1000 VAC RMS minimum breakdown to all connector pins except the **Opto Common** pin.
2. These inputs shall exhibit a nominal impedance to the **Opto Common** pin of 5000 ohms ± 10%, and shall require 2.4 milliamperes ± 10% from a nominal 12 VAC supply.
3. The **Opto** inputs shall not recognize 3 VAC RMS or less relative to the common input.
4. The **Opto** inputs shall recognize 6 VAC RMS or more relative to the common input.
5. Any steady state voltage applied between an **Opto** input and the **Opto Common** shall not exceed 35 VAC RMS.
6. **Opto** inputs shall not be acknowledged when active for 25 milliseconds or less, and shall be acknowledged when active for 50 milliseconds or more.
7. The **Opto** inputs to the BIU shall conform to section 3.3.5.1.2 for voltage transient immunity.

8.6.5.3 LINE FREQUENCY REFERENCE

The **Line Frequency Reference** input pin receives a square wave signal from the cabinet power supply for the purpose of synchronizing BIU outputs with the AC line.

Electrical characteristics for this input shall be as follows:

1. A voltage between 0 and 8 volts shall be considered the Low state, and shall occur when the AC line is in the positive half cycle.
2. A voltage between 16 and 26 volts shall be considered the High state, and shall occur when the AC line is in the negative half cycle.
3. The **Line Frequency Reference** input shall exhibit a nominal impedance of 10 K ohms ± 10% to the +24 VDC input and shall not have more than 1000 picofarads of load capacitance.
4. The rise and fall time of the signal connected to this input shall not exceed 50 microseconds.

8.6.5.4 24 VOLT SIGNAL INPUTS

The 24 Volt Signal Inputs to the BIU shall conform to section 3.3.5.1.2 for Transient Immunity, and shall conform to section 3.3.5.1.3 for electrical characteristics.

8.6.5.4.1 Address Select Inputs

The **Address Select** input bits define the logical position of each BIU. The pins are left open or floating for a logical False, and are connected to **Logic Ground** for a logical True. There shall be 16 unique address positions selected with a binary code, using bit 0 as least significant and bit 3 as most significant. Address bit connections are illustrated in Section 5, TF.

8.6.5.4.2 Function Inputs

When the **Address Select 3** input to the BIU is inactive, the BIU pins labeled Input (n) and Input/Output (n) shall provide input to the BIU from the TF as required in Section 5.3.1.2.

When the **Address Select 3** input to the BIU is active (activating Detector Mode), the Function Input timing shall accommodate Loop Detector Calls and channel status as follows:

1. A Detector Call signal dwelling in a defined logic state for less than 0.25 milliseconds shall not be recognized.
2. A Detector Call signal dwelling in a defined logic state for 1 millisecond or more shall be recognized.
3. Each Call input shall activate a time stamp feature within the BIU to enable accurate pulse width measurement. Details on this time stamp may be found in Section 3.3.1.4-2f.
4. Detector Channel Status shall be derived from pulse width modulation encoding. These shall conform to the eight status states as outlined in Section 6.5.2.26.3.
5. The BIU shall have sufficient buffering to accumulate multiple states of Detector Channel Status between the once-per-second polls. Channel Status pulse width sequences already in process at the time of type 152–155 Positive Acknowledge Frames shall not be missed or truncated due to asynchronous polling, but shall be sent in the next poll.

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8.6.5.5 +24 VDC INPUT

The **+24 VDC** input connects to the cabinet power supply 24 volt output to supply operating power to the BIU.

8.6.5.6 EARTH GROUND

The **Earth Ground** input connects only to exposed electrically conductive panels or covers on the BIU. This input connects to **Earth Ground** in the TF, and shall not connect to **Logic Ground** within the BIU.

8.6.5.7 LOGIC GROUND

This pin supplies the current return path to the power supply and all 24 volt inputs and outputs, and shall not connect to **Earth Ground** within the BIU.

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NEMA STANDARDIZATION BACKGROUND

The purpose of NEMA Standards, their classification, and status are set forth in certain clauses of the NEMA *Standardization Policies and Procedures* manual and are referenced below:

Purpose of Standards

National Electrical Manufacturers Association Standards are adopted in the public interest and are designed to eliminate misunderstandings between the manufacturer and the purchaser and to assist the purchaser in selecting and obtaining the proper product for their particular needs. Existence of a National Electrical Manufacturers Association Standard does not in any respect preclude any member or nonmember from manufacturing or selling products not conforming to the standard.

(Standardization Policies and Procedures, p. 1)

Definition of a Standard

A Standard of the National Electrical Manufacturers Association defines a product, process or procedure with reference to one or more of the following: nomenclature, composition, dimensions, tolerances, safety, operating characteristics, performance, rating, testing, and the service for which they are designed.

(Standardization Policies and Procedures, p. 2)

Dimensions

Where dimensions are given for interchangeability purposes, alternate dimensions satisfying the other provisions of the Standards Publication may be capable of otherwise equivalent performance.

(Standardization Policies and Procedures, p. 8)

Categories of Standards

National Electrical Manufacturers Association Standards are of three classes, which have received the affirmative vote of at least two-thirds of the Subdivision votes cast in the affirmative or negative:

1. NEMA Standard, which relates to a product, process, or procedure commercially standardized and subject to repetitive manufacture.
2. Suggested Standard for Future Design, which may not have been regularly applied to a commercial product, but which suggests a sound engineering approach to future development.
3. Adoptive Standard, which is adopted in whole or in part from the standards of another organization, either domestic, regional, or international.

(Standardization Policies and Procedures, pp. 7 & 16)

Authorized Engineering Information

Authorized Engineering Information consists of explanatory data and other engineering information of an informative character not falling within the classification of NEMA Standard or Suggested Standard for Future Design, which standard has received the affirmative vote of at least two-thirds of the Subdivision votes cast in the affirmative or negative.

(Standardization Policies and Procedures, pp. 7 & 16)

Identification of Status

Standards in NEMA Standards Publications are identified as "NEMA Standard," "Suggested Standard for Future Design," or "Adoptive Standard." These indicate the status of the standard. A statement incorporating the auxiliary verb "shall" indicates that compliance with a requirement is mandatory for compliance with the standard. These classes of standards are identified in the foreword or throughout the text.

The material identified as "Authorized Engineering Information" is designated similarly. Statements incorporating other auxiliary verbs such as "should," "may," etc. refer to authorized engineering information and not to procedures required for compliance with the standard.

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