FINAL
DRAFT

INTERNATIONAL STANDARD

ISO/IEC FDIS 14776-121

ISO/IEC JTC **1**

Secretariat: **ANSI**

Voting begins on:
2007-10-02

Voting terminates on:
2007-12-02

Information technology — Small Computer System Interface (SCSI —

Part 121: Passive Interconnect Performance (PIP)

Technologies de l'information — Interface de petit système d'ordinateur (SCSI) —

Partie 121: Performance passive d'interconnexion (PIP)

Please see the administrative notes on page iii

RECIPIENTS OF THIS DRAFT ARE INVITED TO SUBMIT, WITH THEIR COMMENTS, NOTIFICATION OF ANY RELEVANT PATENT RIGHTS OF WHICH THEY ARE AWARE AND TO PROVIDE SUPPORTING DOCUMENTATION.

IN ADDITION TO THEIR EVALUATION AS BEING ACCEPTABLE FOR INDUSTRIAL, TECHNOLOGICAL, COMMERCIAL AND USER PURPOSES, DRAFT INTERNATIONAL STANDARDS MAY ON OCCASION HAVE TO BE CONSIDERED IN THE LIGHT OF THEIR POTENTIAL TO BECOME STANDARDS TO WHICH REFERENCE MAY BE MADE IN NATIONAL REGULATIONS.

Reference number
ISO/IEC FDIS 14776-121:2007(E)

© ISO/IEC 2007

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS

Not for Resale

PDF disclaimer

This PDF file may contain embedded typefaces. In accordance with Adobe's licensing policy, this file may be printed or viewed but shall not be edited unless the typefaces which are embedded are licensed to and installed on the computer performing the editing. In downloading this file, parties accept therein the responsibility of not infringing Adobe's licensing policy. The ISO Central Secretariat accepts no liability in this area.

Adobe is a trademark of Adobe Systems Incorporated.

Details of the software products used to create this PDF file can be found in the General Info relative to the file; the PDF-creation parameters were optimized for printing. Every care has been taken to ensure that the file is suitable for use by ISO member bodies. In the unlikely event that a problem relating to it is found, please inform the Central Secretariat at the address given below.

Copyright notice

This ISO document is a Draft International Standard and is copyright-protected by ISO. Except as permitted under the applicable laws of the user's country, neither this ISO draft nor any extract from it may be reproduced, stored in a retrieval system or transmitted in any form or by any means, electronic, photocopying, recording or otherwise, without prior written permission being secured.

Requests for permission to reproduce should be addressed to either ISO at the address below or ISO's member body in the country of the requester.

ISO copyright office
Case postale 56 • CH-1211 Geneva 20
Tel. + 41 22 749 01 11
Fax + 41 22 749 09 47
E-mail copyright@iso.org
Web www.iso.org

Reproduction may be subject to royalty payments or a licensing agreement.

Violators may be prosecuted.

© ISO/IEC 20## – All rights reserved

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS

Not for Resale

In accordance with the provisions of Council Resolution 21/1986, this document is **circulated in the English language only**.

© ISO/IEC 2007 – All rights reserved
Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS
Not for Resale

Foreword 3

Introduction 4

1 Scope 12

2 References 12
2.1 Approved references 12
2.2 References under development 12

3 Definitions 12
3.1 Terms 12
3.2 Acronyms 18
3.3 Symbols and abbreviations 18
3.4 Keywords 19
3.5 Conventions 20
3.6 Specification of measurement equipment 20

4 Overview 21
4.1 General 21
4.2 Open vs. closed systems related to this standard 21
4.3 Structural considerations 21
4.3.1 SCSI interconnects 21
4.3.2 SCSI passive interconnect topology 22
4.3.3 Interconnect sub-assemblies, transition regions, and bulk cable 22
4.3.4 Interconnect assemblies 22
4.3.5 Relationship between SE and DF in this document 22
4.4 Relationship between requirements on bulk cable and requirements on interconnect assemblies . 23
4.5 Physical measurement points 23
4.6 Concatenated configurations 23
4.7 Interoperability points 23
4.8 Constructions considered 24
4.9 Identification, constraints and loading requirements 25
4.9.1 Connector function identification 25
4.9.2 Constraints 25
4.9.3 Standard loads 26
4.9.3.1 Targets and initiators with no enabled terminator 26
4.9.3.2 Targets and initiators with enabled terminator 26
4.10 Nature of requirements 26
4.10.1 Measurements and tests 26
4.10.2 Performance levels and applications 26
4.10.3 Basic performance requirements for interconnect assemblies 27
4.10.3.1 Overview 27
4.10.3.2 Measurement conditions for non-precomp received signal quality requirements 28
4.10.3.3 Measurement conditions for precomp received signal quality requirements 28
4.10.4 Deriving the launch signal requirements for this standard from the signal requirements in SPI-x28
4.11 Local neighborhood concepts 29
4.12 Length specifications 29
4.13 S21 relationship among point to point and multidrop configurations 29
4.14 Accommodation of receiver compensation in interconnect requirements 30
4.15 Instrumentation and text fixture considerations 30
4.16 Signals covered by this standard 31
4.17 Error rate considerations 33

5 Summary bulk cable 34

6 Bulk cable samples, test fixtures and setups 36

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

6.1 Bulk cable samples and sample preparation 36
6.1.1 Overview 36
6.1.2 Summary 36
6.1.3 Point to point bulk cable 36
6.1.3.1 Point to point bulk cable sample preparation (SP_Bulk_PP3) 36
6.1.3.2 Point to point bulk cable sample preparation (SP_Bulk_PP10) 37
6.1.3.3 Point to point bulk cable sample preparation (SP_Bulk_PP25) 37
6.1.4 Sample preparation for multi-drop bulk cable or printed circuit boards 37
6.1.4.1 Multi-drop bulk cable sample preparation (SP_Bulk_MD3) 37
6.1.4.2 Printed circuit boards sample preparation 37
6.2 Bulk cable and printed circuit board test fixture specifications 38
6.2.1 Overview 38
6.2.2 Summary 38
6.2.3 Test fixture (FIX_Bulk_1) 38
6.2.4 Test fixture (FIX_Bulk_2) 39
6.2.5 Test fixture (FIX_Bulk_3) 40
6.2.6 Test fixture (FIX_Bulk_4) 40
6.2.7 Printed circuit boards test fixture (FIX_PCB_1) 40
6.3 Bulk cable measurement equipment and setups 41
6.3.1 Summary 41
6.3.2 Set up (SET_Bulk_1) 42
6.3.3 Set up (SET_Bulk_2) 42
6.3.4 Set up (SET_Bulk_3) 43
6.3.5 Set up (SET_Bulk_4) 43
6.3.6 Set up (SET_Bulk_5) 44
6.4 STD calibration 44

7 Level 1 bulk cable tests 46
7.1 SE tests 46
7.2 Differential local impedance 46
7.2.1 Overview 46
7.2.2 Point-to-point bulk cable 46
7.2.2.1 Sample preparation for point to point bulk cable 46
7.2.2.2 Test fixtures for point to point bulk cable 46
7.2.2.3 Measurement equipment and setup for point to point bulk cable 46
7.2.2.4 Calibration and verification procedure for point to point bulk cable 46
7.2.2.5 Test procedure and data output format 47
7.2.2.6 Acceptable values for point to point bulk cable 48
7.2.3 Multi-drop bulk cable 48
7.2.3.1 Sample preparation for multi-drop bulk cable 48
7.2.3.2 Test fixtures for multi-drop bulk cable 48
7.2.3.3 Measurement equipment and setup for multi-drop bulk cable 48
7.2.3.4 Calibration and verification procedure for multi-drop bulk cable 49
7.2.3.5 Test procedure and data output format for multi-drop bulk cable 49
7.2.3.6 Acceptable values for multi-drop bulk cable 50
7.2.4 Unpopulated printed circuit board (PCB) 50
7.3 Differential propagation time and propagation time skew 50
7.3.1 Overview 50
7.3.2 Point-to-point bulk cable 50
7.3.2.1 Sample preparation for point to point bulk cable 50
7.3.2.2 Test fixtures for point to point bulk cable 50
7.3.2.3 Measurement equipment and setup for point to point bulk cable 51
7.3.2.4 Calibration and verification procedure for point to point bulk cable 51
7.3.2.5 Test procedure and data output format for point to point bulk cable 51
7.3.2.6 Acceptable values for point to point bulk cable 52
7.3.3 Multi-drop bulk cable 52
7.3.3.1 Sample preparation for multi-drop bulk cable 52

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

7.3.3.2 Test fixtures for multi-drop bulk cable 52
7.3.3.3 Measurement equipment and setup for multi-drop bulk cable 52
7.3.3.4 Calibration and verification procedure for multi-drop bulk cable 53
7.3.3.5 Test procedure and data output format for multi-drop bulk cable 53
7.3.3.6 Acceptable values for multi-drop bulk cable 53
7.3.4 Unpopulated PCB 53
7.4 Differential capacitance by calculation 53
7.4.1 Overview 53
7.4.2 Differential capacitance by calculation for all constructions of bulk cable 53
7.4.3 Acceptable differential capacitance values for all constructions of bulk cable 53
7.5 Differential capacitance by frequency domain measurement 54
7.5.1 Point-to-point bulk cable 54
7.5.1.1 Sample preparation for point to point bulk cable 54
7.5.1.2 Test fixtures for point to point bulk cable 54
7.5.1.3 Measurement equipment and setup for point to point bulk cable 54
7.5.1.4 Calibration and verification procedure for point to point bulk cable 54
7.5.1.5 Test procedure and data output format for point to point bulk cable 54
7.5.2 Multi-drop bulk cable 54
7.5.3 Unpopulated PCB 54
7.5.4 Acceptable differential capacitance values for all constructions of bulk cable 54
7.6 Differential insertion loss 55
7.6.1 Overview 55
7.6.2 Point-to-point bulk cable 55
7.6.2.1 Sample preparation for point to point bulk cable 55
7.6.2.2 Test fixtures for point to point bulk cable 55
7.6.2.3 Measurement equipment and setup for point to point bulk cable 55
7.6.2.4 Calibration, verification and measurement procedure for point to point bulk cable 55
7.6.2.5 Acceptable values for point to point bulk cable 56
7.6.3 Multi-drop bulk cable 56
7.6.3.1 Overview 56
7.6.3.2 Sample preparation for multi-drop bulk cable 56
7.6.3.3 Test fixtures for multi-drop bulk cable 56
7.6.3.4 Measurement equipment and setup for multi-drop bulk cable 57
7.6.3.5 Calibration, verification and measurement procedure for multi-drop bulk cable 57
7.6.3.6 Acceptable values for multi-drop bulk cable 57
7.6.4 Unpopulated PCB 57
7.7 Near end cross talk (NEXT) 57
7.7.1 Overview 57
7.7.2 Point-to-point bulk cable 58
7.7.2.1 Sample preparation for point to point bulk cable 58
7.7.2.2 Test fixtures for point to point bulk cable 58
7.7.2.3 Measurement equipment and setup for point to point bulk cable 58
7.7.2.4 Calibration and verification procedure for point to point bulk cable 58
7.7.2.5 Test procedure and data output format for point to point bulk cable 60
7.7.2.6 Acceptable values for point to point bulk cable 60
7.7.3 Multi-drop bulk cable 60
7.7.3.1 Sample preparation for multi-drop bulk cable 60
7.7.3.2 Test fixtures for multi-drop bulk cable 61
7.7.3.3 Measurement equipment and setup for multi-drop bulk cable 61
7.7.3.4 Calibration and verification procedure for multi-drop bulk cable 61
7.7.3.5 Test procedure and data output format for multi-drop bulk cable 61
7.7.3.6 Acceptable values for multi-drop bulk cable 62
7.7.4 Unpopulated PCB 62

8 Summary - interconnect assemblies 63

9 Interconnect assemblies samples, test fixtures, and setups 64

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

9.1 Interconnect assembly samples and sample preparation 64
9.2 Test fixtures for interconnect assemblies 64
9.2.1 Overview 64
9.2.2 Summary 64
9.2.3 Test fixture (FIX_ASY_1) 65
9.2.4 Test fixture (FIX_ASY_2) 66
9.2.5 Test fixture (FIX_ASY_3) 67
9.2.6 Test fixture (FIX_ASY_4) 67
9.3 Interconnect assembly measurement equipment and setups 68
9.3.1 Summary 68
9.3.2 Set up (SET_ASY_1) 69
9.3.3 Set up (SET_ASY_2) 69
9.3.4 Set up (SET_ASY_3) 70
9.3.5 Set up (SET_ASY_4) 70
9.4 STD Calibration 71

10 Level 1 interconnect assembly tests 71
10.1 Differential impedance 71
10.1.1 Overview 71
10.1.2 Point-to-point interconnect assemblies 71
10.1.2.1 Test fixtures for point to point interconnect assemblies 71
10.1.2.2 Measurement equipment and setup for point to point interconnect assemblies 71
10.1.2.3 Calibration and verification procedure for point to point interconnect assemblies 71
10.1.2.4 Test procedure and data output format for point to point interconnect assemblies 71
10.1.3 Multi-drop interconnect assemblies 71
10.1.3.1 Test fixtures for multi-drop interconnect assemblies 71
10.1.3.2 Measurement equipment and setup for multi-drop interconnect assemblies 71
10.1.3.3 Calibration and verification procedure for multi-drop interconnect assemblies 72
10.1.3.4 Test procedure and data output format for multi-drop interconnect assemblies 72
10.1.4 Connectorized backplanes 72
10.1.5 Acceptable values for all constructions of interconnect assemblies 72
10.2 Differential propagation time and propagation time skew 72
10.2.1 Overview 72
10.2.2 Point-to-point interconnect assemblies 72
10.2.2.1 Test fixtures for point to point interconnect assemblies 72
10.2.2.2 Measurement equipment and setup for point to point interconnect assemblies 72
10.2.2.3 Calibration and verification procedure for point to point interconnect assemblies 72
10.2.2.4 Test procedure and data output format for point to point interconnect assemblies 72
10.2.3 Multi-drop interconnect assemblies 72
10.2.4 Connectorized backplanes 73
10.2.5 Acceptable values for all constructions of interconnect assemblies 73
10.3 Signal integrity diagrams 73
10.3.1 Overview 73
10.3.2 Requirements for all constructions of interconnect assemblies 75
10.3.2.1 Test fixtures for all constructions of interconnect assemblies 75
10.3.2.2 Measurement equipment and setup for all constructions of interconnect assemblies 75
10.3.2.3 Calibration and verification procedure for all constructions of interconnect assemblies 75
10.3.2.3.1 Overview 75
10.3.2.3.2 Non-precomp driver requirements 75
10.3.2.3.3 Precomp driver requirements 76
10.3.2.4 Test procedure and data output format for all constructions of interconnect assemblies 76
10.3.2.5 Acceptable values for all constructions of interconnect assemblies 77
10.4 Differential to common mode conversion 78
10.4.1 Overview 78
10.4.2 Requirements for all constructions of interconnect assemblies 78
10.4.2.1 Test fixtures for all constructions of interconnect assemblies 78
10.4.2.2 Measurement equipment and setup for all constructions of interconnect assemblies 78

--`,,```,,,,````-`-`,,`,,`,`,,`---
Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

10.4.2.3 Calibration and verification procedure for all constructions of interconnect assemblies 78
10.4.2.4 Test procedure and data output format for all constructions of interconnect assemblies 78
10.4.2.5 Acceptable values for all constructions of interconnect assemblies 78
10.5 Differential insertion loss 78
10.5.1 Overview 78
10.5.2 Requirements for all constructions of interconnect assemblies 79
10.5.2.1 Test fixtures for all constructions of interconnect assemblies 79
10.5.2.2 Measurement equipment and setup for all constructions of interconnect assemblies 79
10.5.2.3 Calibration, verification, and measurement procedure for all constructions of interconnect assemblies 79
Annex A (normative) Single ended bulk cble requirements 80
A.1 Overview 80
A.2 Impedance 80
A.2.1 Local impedance for SE transmission 80
A.2.1.1 Local impedance for SE transmission overview 80
A.2.1.2 Sample preparation 80
A.2.1.3 Test fixture and measurement equipment 80
A.2.1.4 Calibration and verification procedure 81
A.2.1.4.1 Instrument verification 81
A.2.1.4.2 Measurement system (with test fixture) calibration 81
A.2.1.4.3 Single ended signal transition duration (STD) calibration 82
A.2.1.5 Testing procedure 83
A.3 Capacitance 84
A.3.1 Single ended capacitance 84
A.3.1.1 Sample preparation 84
A.3.1.2 Test fixture for single ended capacitance 85
A.3.1.3 Calibration procedure 85
A.3.1.4 Measurement procedure 85
A.3.1.4.1 Planar cables - G-S-G 85
A.3.1.4.2 Round cables - shielded 85
Annex B (informative) Periodic structure effects 86
Annex C (informative) SCSI signal driver boards (SSDB) 87
Annex D (informative) Mirage effects in multi-drop subassembly TDR impedance measurement 88
D.1 Overview 88
D.2 Mirages 88
D.3 Average impedance 91
D.4 Recommendations: 91
D.4.1 Overview 91
D.4.2 Fixture 92
D.4.3 Twisted region 92
D.4.4 Flat region 93

bibliography 94

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

List of figures

Figure 1 -Relationship between S21 for different configurations 30
Figure 2 -Example cable/backplane frequency response test setup 31
Figure 3 -Test fixture (FIX_Bulk_1) 39
Figure 4 -Test fixture (FIX_Bulk_2) 39
Figure 5 -Test fixture (FIX_Bulk_3) 40
Figure 6 -Equipment setup for SET_Bulk_1 42
Figure 7 -Equipment setup for SET_Bulk_2 42
Figure 8 -Equipment setup for SET_Bulk_3 43
Figure 9 -Equipment setup for SET_Bulk_4 43
Figure 10 -Equipment setup for SET_Bulk_5 44
Figure 11 -Signal transition duration calibration 45
Figure 12 -Differential calibration 47
Figure 13 -Cursor placement for bulk cable 48
Figure 14 -Cursor placement for constant interval multi-drop cable 49
Figure 15 -TDR launch de-skew 51
Figure 16 -Propagation time measurement 52
Figure 17 -Calibration configuration 55
Figure 18 -Near end cross talk measurement region 59
Figure 19 -Measure aggressor voltage and victim voltage 60
Figure 20 -Measure aggressor voltage and victim voltage 61
Figure 21 -Test fixture (FIX_ASY_1) 65
Figure 22 -Test fixture (FIX_ASY_2) 66
Figure 23 -SCSI signal driver board (FIX_ASY_3) 67
Figure 24 -Test fixture (FIX_ASY_4) 67
Figure 25 -Detail for balun board shown in figure 24 68
Figure 26 -Interconnect assembly set up 1 (SET_ASY_1) 69
Figure 27 -Interconnect assembly set up 2 (SET_ASY_2) 69
Figure 28 -Interconnect assembly set up 3 (SET_ASY_3) 70
Figure 29 -Interconnect assembly set up 4 (SET_ASY_4) 70
Figure 30 -Distinction between parallel and serial data in the same signal path 74
Figure A.1 -Test configuration for SE impedance 81
Figure A.2 -SE impedance calibration 82
Figure A.3 -Signal transition duration calibration 83
Figure A.4 -SE impedance measurement 84
Figure A.5 -Test fixture for single ended capacitance measurement 85
Figure D.1 -Typical multi-drop cable 88
Figure D.2 -Mirage – missing flat 89
Figure D.3 -Mirage – obscured flat 90
Figure D.4 -Filtered traces 90
Figure D.5 -Average impedance conundrum 91
Figure D.6 -Long test fixture 92
Figure D.7 -Long twist, no flats 92
Figure D.8 -Short twist into various loads 93
Figure D.9 -Flat 93

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

List of tables

Table 1 -SE and DF map 15
Table 3 -Bulk cable level 1 test summary 27
Table 4 -Bulk cable level 2 measurement summary 28
Table 5 -Bulk cable sample preparation 29
Table 6 -Bulk cable and printed circuit board test fixtures 31
Table 7 -Bulk cable measurement equipment and setups 35
Table 8 -Interconnect assembly level 1 test summary 60
Table 9 -Interconnect assembly level 2 measurement summary 60
Table 10 -Test fixtures for interconnect assemblies 61
Table 11 -Interconnect assembly measurement equipment and setups 65
Table 12 -Test array example for a three port interconnect assembly 75

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

Foreword

1) ISO (International Organization for Standardization) and IEC (International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work.

2) In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75 % of the national bodies casting a vote.

3 All users should ensure that they have the latest edition of this publication.

4 No liability shall attach to IEC or ISO or its directors, employees, servants or agents including individual experts and members of their technical committees and IEC or ISO member bodies for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication of, use of, or reliance upon, this ISO/IEC publication or any other IEC, ISO or ISO/IEC publications.

5) Attention is drawn to the normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.

6) Attention is drawn to the possibility that some of the elements of this International Standard may be the subject of patent rights. ISO and IEC shall not be held responsible for identifying any or all such patent rights.

International Standard ISO/IEC 14776-121 was prepared by subcommittee 25: Interconnection of information technology equipment, of ISO/IEC joint technical committee 1: Information technology.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

Introduction

The Parallel Interface Performance standard defines requirements for measuring the electrical performance of bulk cable and interconnect assemblies for use in SPI-x applications and specification of performance limits.

The Parallel Interface Performance standard is divided into the following clauses:

- Clause 1 is the scope;
- Clause 2 enumerates the normative references;
    - Clause 3 describes the definitions, symbols, conventions and abbreviations;
    - Clause 4 provides a general overview of the concepts;
    - Clause 5 contains a summary of bulk cable requirements
    - Clause 6 contains sample preparation, fixtures and setups for bulk cable
    - Clause 7 contains bulk cable test procedures
    - Clause 8 contains a summary of interconnect assembly requirements
    - Clause 9 contains sample preparation, fixtures, and setups for interconnect assemblies
    - Clause 10 contains interconnect test requirements

    - Annex A, Single ended bulk cable requirements, forms an integral part of this standard.

The follow informative annexes are provided:

    - Annex B, Periodic structure effects
    - Annex C, Requirements for SCSI signal driver board (SSDB)
    - Annex D, Mirage effects in multi-drop subassemblyTDR impedance measurement

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

1 Scope

In the past only the performance requirements for uniform bulk cable (called "media" in earlier standards) have been specified in SCSI standards. Since bulk cable provides only part of the electrical path in a SCSI bus segment, the performance requirements of the interconnect comprising the path is incomplete if only bulk cable is considered. This document expands the coverage to the complete assembled interconnect including connectors, uniform bulk cable, and non-uniform bulk cable. A syntax and framework is described for all types of passive interconnect. The methodology for performing the electrical measurements required to determine compliance with the performance requirements for bulk cable of several types, various assembled interconnects and printed circuit board designs is included.

Details of the measurement methodology are specified to minimize the difference in measured results from different electrical testing laboratories. Details include calibration, fixturing and sample preparation, equipment, measurement procedure and data output format.

2 References

2.1 Approved references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC 14776-112, SCSI Parallel Interface standard-2 (SPI-2)
ISO/IEC 14776-113, SCSI Parallel Interface standard-3 (SPI-3)
ISO/IEC 14776-115, SCSI Parallel Interface standard-5 (SPI-5) [T10/1525D]

2.2 References under development

The reference in this subclause was correct at the time of approval of this International Standard.

The provisions of the referenced specifications, as identified in this subclause, are valid within the context of this IS. The reference to a specification within this IS does not give it any further status within ISO/IEC; in particular, it does not give the referenced specification the status of an International Standard

INCITS.362-2002, SCSI Parallel Interface Standard-4 (SPI-4)

3 Definitions

3.1 Terms

3.1.1 Accuracy: quality of freedom from mistake or error. The degree of correctness with which a measured value agrees with the true value. Not to be confused with precision - see 3.1.74.

3.1.2 Admittance: an *n*-terminal network, the complex current flowing to the *i*-th terminal divided by the complex voltage applied between the *j*-th terminal with respect to the reference point when all other terminals have arbitrary terminations. The inverse of impedance.

3.1.3 American Wire Gauge: formerly the Brown & Sharpe Gage, the standard gauge for copper, aluminum, and other conductors except steel.

3.1.4 Assembly: A subordinate element of a system that is comprised of two or more components

3.1.5 Asserted: Having a signal value associated with a logic 1.

3.1.6 Attenuation: 1) A general term used to denote a decrease in signal magnitude from one point to another. Attenuation may be expressed as a scalar ratio of the input magnitude to the output magnitude or in decibels as 20 times the log of that ratio. 2) The reciprocal of gain.

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

3.1.7 Backplane: The printed circuit board that contains the interconnect traces and connectors, into which boards or plug-in units are inserted.

3.1.8 Balanced: 1) The state of impedance on a two-wire circuit when the impedance-to-ground of one wire is equal from the impedance-to-ground of the other wire. 2) A circuit, in which two branches are electrically alike and symmetrical with respect to a common reference point, usually ground.

3.1.9 Buffer: In the sense of the IBIS standard, an isolating circuit used to prevent a driven circuit from influencing a driving circuit. A transceiver, see 3.1.98.

3.1.10 Bulk cable: Cable that is not pure connector terminated.

3.1.11 Bus: A signal line or a set of lines used by an interface system to connect a number of devices and transfer data.

3.1.12 Cable assembly: A cable that is connector terminated. Generally, a cable that has been terminated by a manufacturer and is ready for installation.

3.1.13 Calibration: Criteria to validate the measurement.

3.1.14 Capacitive coupling: The type of coupling in which the mechanism is capacitance between the interference source, and the signal system; that is, the interference is induced in the signal system by an electric field produced by the interfering source.

3.1.15 Circuit: An interconnection of electrical components.

3.1.16 Circuit element: A basic constituent part of a circuit, exclusive of interconnections. A component.

3.1.17 Common-mode: The instantaneous algebraic average of two signals applied to a balanced circuit, both signals referred to a common reference.

3.1.18 Common-mode noise: The noise voltage that appears equally and in phase from each signal conductor to ground.

3.1.19 Component: Items from which a system, assembly, or sub-assembly is assembled; for example, resistors, capacitors, inductors, semiconductors, etc. A circuit element.

3.1.20 Complementary metal oxide semiconductor: A semiconductor technology in which circuits are composed of paired NMOS and PMOS devices.

3.1.21 Complex dielectric constant: The complex permittivity of a physical medium in ration to the permittivity of free space.

3.1.22 Complex permittivity: For isotropic media, the ratio of the complex amplitude of the electric displacement density to the complex amplitude of the electric field strength.

3.1.23 Computer-aided engineering: The application of computers to the engineering process. The term applies to any computer system or program that manipulates data for the purpose or assisting engineering, design, procurement, maintenance, etc.

3.1.24 Concatenated: Two or more interconnect assemblies (similar or dissimilar) connected together as part of a single SCSI bus segment. Examples include round shielded cable connected to a backplane with no expander on the backplane and flat multidrop interconnect assembly connected to a round point to point interconnect assembly.

3.1.25 Conductivity: (σ) A macroscopic material property that relates the conduction current density (J) to the electric field (E) in the medium.

3.1.26 Connector terminated: A section of cable with connectors attached.

3.1.27 Contact: The electrically conductive portion of a connector associated with a single conductor in a cable.

3.1.28 De-asserted: Having a current value equal to a logic 0.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

3.1.29 Device: The entity that contains the SCSI driver and receiver

3.1.30 Dielectric constant: 1) That physical property which determines the electrostatic energy stored per unit volume for unit potential gradient. This value is usually is given relative to vacuum. 2) The real part of the complex dielectric constant.

3.1.31 Dielectric loss: That contribution to the attenuation constant of a propagating mode on a transmission line that represents losses associated with the dielectric properties of the insulation materials involved.

3.1.32 Differential-mode: The instantaneous algebraic difference of two signals applied to a balanced circuit, both signals referred to a common reference.

3.1.33 Differential-mode noise: The noise voltage that appears differentially between two signal wires and acts on the signal sensing circuit in the same manner as the desired signal.

3.1.34 Differential SCSI: A SCSI signal configuration that uses balanced transmission lines.

3.1.35 Discontinuity: 1) An abrupt non uniformity in a uniform transmission line that causes reflected waves. 2) An abrupt change in the cross section of the planar transmission line. Abrupt refers usually to a change in dimensions or material over a length that is short compared to a wavelength. Short is generally recognized as 0,1 wavelength or smaller.

3.1.36 Driver: 1) An electronic circuit that supplies input to another electronic circuit. 2) An electrical circuit whose purpose is to signal a binary state for transmitting information. Also referred to as a generator in international standards.

3.1.37 Electromagnetic compatibility: A system's ability to perform its specified functions in the presence of electrical noise generated either internally or externally by other systems.

3.1.38 Electromagnetic interference: Electromagnetic energy from sources internal or external to electrical or electronic equipment that adversely affect equipment by creating undesirable responses.

3.1.39 Electrostatic discharge: The sudden transfer of charge between bodies of differing electrostatic potential.

3.1.40 Element: A component, subcomponent, assembly, subassembly, or part of a physical architecture or system.

3.1.41 Expander: A device that connects SCSI device segments together to form a single SCSI domain. See SDV.

3.1.42 False: One of two binary states the other of which is true. False is usually represented by 0.

3.1.43 Gain: 1) A general term used to denote a increase in signal magnitude from one point to another. Gain may be expressed as a scalar ratio of the input magnitude to the output magnitude or in decibels as 20 times the log of that ratio. 2) The reciprocal of attenuation.

3.1.44 Group delay: The derivative of radian phase with respect to radian frequency $\partial\phi/\partial\omega$. Group delay is equal to the phase delay for an ideal non dispersive device or medium, but may differ greatly in an actual device or medium where there is ripple in the phase versus frequency characteristic. In network analyzers, $\partial\omega$ is replaced by $\Delta\omega$, and shall be sufficiently large to permit adequate measurement resolution. If $\Delta\omega$ is too large, the limit in the defining equation will not be reached, and the measured group delay is dependent upon $\Delta\omega$. Therefore the value of $\Delta\omega$ used in a measurement shall be specified.

3.1.45 Group delay time: The rate of change, with angular frequency, of the total phase shift through a network. Group delay time is the time interval required for the crest of a group of interfering waves to travel thorough a 2-port network, where the component wave trains have slightly different individual frequencies.

3.1.46 Group velocity: The velocity of propagation of a signal envelope, provided that the envelope moves without a significant change of shape. The magnitude of the group velocity is equal to the reciprocal of the rate of change of phase constant with angular frequency.

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

3.1.47 Hardware description language: A computer language with special constructs and verification protocols, used to develop, analyze, validate, and document a hardware design or computer architecture.

3.1.48 Inductive coupling: The type of coupling in which the mechanism is inductance between the interference source, and the signal system; that is, the interference is induced in the signal system by a magnetic field produced by the interfering source.

3.1.49 Insulation displacement contact: A type of contact where the connection to the cable is made by mechanically piercing the cable insulation as opposed to a connection in which the cable insulation is removed to provide access to the conductor.

3.1.50 Interconnect component: Interconnect components include cables, connectors, printed circuit boards and transition regions. All interconnect components are passive.

3.1.51 Isotropic: Pertaining to a material whose electric or magnetic properties, or both, are directionally independent.

3.1.52 Logical unit: An externally addressable entity within a target and that processes SCSI commands.

3.1.53 Least significant: Within a group of items that, taken as a whole, represents a numerical value, the item within the group with the smallest numerical weighting.

3.1.54 Loss tangent: The ratio of the imaginary part of the complex dielectric constant of a material to its real part.

3.1.55 Measurement: The process of obtaining data.

3.1.56 Microstrip: A class of planar transmission lines consisting of one or more thin conducting strips of finite width parallel to a single extended conducting ground plane. The strips are fixed to an insulating substrate attached to the ground plane. The semi-infinite space above the strips is filled with a medium of relative permittivity and permeability equal to or less than the substrate.

3.1.57 Mode: Synonymous with transmission mode. See 3.1.102.

3.1.58 Model: 1) An approximation, representation, or idealization of selected aspects of the structure, behavior, operation, or other characteristics of a real-world process, concept, or system. Models may have other models as components. 2) To serve as a model in definition 1. 3) To develop or use a model as in definition 1.

3.1.59 Most significant: Within a group of items that, taken as a whole, represents a numerical value, the item within the group with the greatest numerical weighting.

3.1.60 Multiline: A model representation of a multi-conductor component that includes the capacitive and inductive coupling among the conductors.

3.1.61 Netlist: A listing of the nets of a circuit, providing, usually in text format, a description of the connections among the components of the circuit.

3.1.62 Network: Any set of devices or subsystems connected by links joining, directly or indirectly, a set of terminal nodes.

3.1.63 Network function: Any impedance, admittance function or any other function of p that can be expressed in terms of or derived from the determinant of a network and its cofactors. This also includes voltage ratios, current ratios, and numerous other quantities.

3.1.64 Network matrix: Anyone of several matrices that relate the equivalent voltage, current, incident waves and reflected waves of an *n*-port network.

3.1.65 Network parameters: The elements of a network matrix.

3.1.66 One: A true logic state.

3.1.67 Phase angle: The measure of the progression of a periodic wave in time or space from a chosen instant or position.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

3.1.68 Phase delay: The ration of total radian phase shift, to the specified radian frequency. Phase delay is nominally constant over the frequency band of operation for nondestructive delay components.

3.1.69 Phase shift: 1) The absolute magnitude of the difference between two phase angles. 2) The displacement in time of one periodic-waveform relative to other waveforms.

3.1.70 Phase velocity: The velocity of an equiphase surface normal to the direction of propagation of a traveling wave at a single frequency, and for a given mode;

3.1.71 Planar transmission line: A transmission line composed of one or more parallel plates, slabs, or sheets of conduction or insulating material, including free space, and in which one or more layers are composed of material of differing electromagnetic properties, arranged in strips of finite cross section and aligned with the axis of propagation to form the guiding structures.

3.1.72 Pole: A value of *s* that makes a transfer function in the complex variable infinity, or its corresponding point in the *s* plane.

3.1.73 Port: A place of access to a network where the network variables maybe observed or measured. In this document the places of access include connectors on interconnect assemblies, prepared bulk cable ends and pads on unpopulated backplanes.

3.1.74 Precision: 1) The degree of exactness or discrimination with which a quantity is stated. For example 3 decimal places versus 5 decimal places. 2) The repeatability of measurement data expressed in terms of standard deviation.

3.1.75 Primary bus: The collection of signals that provides the system with the basic mechanism for exchanging data.

3.1.76 Radio frequency: A frequency in the range of 10KHz to 100 000MHz.

3.1.77 Radio frequency interference: Degradation of a wanted signal by an electromagnetic disturbance having components in the RF range.

3.1.78 Receiver: 1) An electronic circuit that recognizes input from another electronic circuit. 2) An electrical circuit whose purpose is to recognize the binary state of transmitted information.

3.1.79 Resistivity: The reciprocal of volume conductivity measured in siemens per centimeter.

3.1.80 s parameter: One of the coefficients of the scattering matrix.

3.1.81 Scattering matrix: A square array used to relate incident and reflected waves for an *n*-port network.

3.1.82 SCSI bus segment: All the conductors and connectors required to attain signal line continuity between every driver, receiver, and terminator for each signal.

3.1.83 SCSI component: A component part of a complete SCSI system. SCSI components include but are not limited to: cables, cable assemblies, devices, terminators, boards, backplanes, controllers, and chips.

3.1.84 SCSI device: A device that contains one or more SCSI ports that are connected to a service delivery subsystem and supports a SCSI application protocol. See SAM-2.

3.1.85 SCSI port: A single attachment to a SCSI bus segment from a SCSI device.

3.1.86 Signal assertion: The act of driving a signal to the true state.

3.1.87 Signal negation: The act of performing a signal release or of driving a signal to the false state.

3.1.88 Single line: A model representation of a multi-conductor component that does not include the capacitive and inductive coupling among the conductors.

3.1.89 Single-ended SCSI: A SCSI signal configuration that uses unbalanced transmission lines.

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

3.1.90 Skin depth: of a conducting material, at a given frequency, the depth at which the surface current density is reduced to 1/*e* of its value at the surface.

3.1.91 Skin effect: The tendency of alternating current to concentrate in the areas of lowest impedance.

3.1.92 Small Computer System Interface: A data-transfer interface used to connect multiple peripheral devices such as disk derives, tapes, or printers to computer systems while taking up only one slot in the computer. Previously this was known as Shugart Associates Systems Interface.

3.1.93 Simulation Program with Integrated Circuit Emphasis: An application-oriented programming language used widely to design electrical circuits.

3.1.94 Stripline: A class of planar transmission line characterized by one or more conducting strips of finite width parallel to and approximately midway between two extended conducting ground planes. The space between the planes is filled with a homogeneous insulation medium.

3.1.95 Stub: section of transmission line joined to the main transmission line and containing a non dissipative termination.

3.1.96 System: In a hierarchical approach, a collection of interacting, interrelated, or interdependent elements forming a collective functioning entity.

3.1.97 Test: Measurement to which a pass-fail criteria is applied.

3.1.98 Transceiver: A device that both transmits and receives data.

3.1.99 Transition region: the region of the cable or PCB, between the connector attachment point and the point in the bulk cable or PCB that is physically undisturbed by the connector attachment methodology.

3.1.100 Transmission line: A structure designed to guide the propagation of electromagnetic energy in a well-defined direction.

3.1.101 Transmission medium: The material on which information signals may be carried. For example: twisted-wire pairs, planar transmission lines, coaxial cable, etc.

3.1.102 Transmission mode: A form of propagation along a transmission line characterized by the presence of one of the elemental types of transverse electric, transverse magnetic, or transverse electromagnetic waves. More than one mode may be concurrent along a transmission line.

3.1.103 Transmittance: A response function for which the variables are measured at different ports.

3.1.104 True: One of two binary states, usually represented by 1, the other of which is false.

3.1.105 Two-port parameters: The network parameters for a two-port device.

3.1.106 Unbalanced: 1) The state of impedance on a two-wire circuit where the impedance-to-ground of one wire is different from the impedance-to-ground of the other wire. 2) Unbalanced frequently signifies a circuit where one side is grounded.

3.1.107 Uniform transmission line: A transmission line that has substantially identical electrical properties throughout its length.

3.1.108 Validation: The process of evaluating a system or component to ensure compliance with the functional, performance, and interface requirements.

3.1.109 Vendor-specific: A term used to describe parameters that may vary between vendors supplying similar components.

3.1.110 Verification: Confirmation by examination (testing) with evidence that specified requirements have been met.

3.1.111 Via: An electrical connection between the layers of a printed circuit board.

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

3.1.112 Zero: 1) A false logic state. 2) Any value of ρ, real or complex for which the network function is zero. 3) A value of *s* that makes a transfer function in the complex variable zero, or its corresponding point in the *s* plane.

3.2 Acronyms

AWG	American wire gauge
CMOS	complementary metal-oxide semiconductor
DCP	driver calibration pattern
DUT	device under test
EMC	electromagnetic compatibility
EMI	electromagnetic interference
ESD	electrostatic discharge
HBA	host bus adapter
HDD	hard disk drive
HVD	high voltage differential
IDC	insulation displacement contact
ISI	inter-symbol interference
LSB	least significant bit
LVD	low voltage differential
MSB	most significant bit
NEXT	near end crosstalk
PCB	printed circuit board
RF	radio frequency
RFI	radio frequency interference
RLGC	resistance, inductance, admittance, capacitance
SCSI	small computer system interface.
SE	single-ended
SPI	SCSI parallel interface
SPI-x	all versions of SPI
SPICE	simulation program with integrated circuit emphasis
SSBD	SCSI signal driver board
STD	signal transition duration
TDR	time domain reflectometer
TDT	time domain through
TDW	time domain waveform
TDWP	time domain waveform pattern
URL	uniform resource locator

3.3 Symbols and abbreviations

±	plus or minus
≈	approximately
x	multiply
+	add
-	subtract
< or LT	less than
≤ or LE	less than or equal
= or EQ	equal
> or GT	greater than
≥ or GE	greater than or equal
≠ or NE	not equal
A	ampere
c	velocity of light in a vacuum
C	coulomb or capacitance
dB	decibel

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

E	electric field
F	farad
G	conductance
g	gram
H	henry
Hz	hertz
j	square root of minus one
J	joule
J	current density
L	inductance
m	meter
N	newton
Np	neper
R	resistance
s	second
s	s parameter
T	tesla
t	time
V	volt
W	watt
Wb	weber
¹	partial differential
ϕ	radial phase
ρ	either conductance or admittance
Ω	ohm
ω	radians per second
T	10^{12}
G	10^{9}
M	10^{6}
k	10^{3}
c	10^{-2}
m	10^{-3}
μ	10^{-6}
n	10^{-9}
p	10^{-12}
f	10^{-15}

3.4 Keywords

3.4.1 Expected: Describes the behavior of the hardware in the design models assumed by this document. Other hardware design models may also be implemented.

3.4.2 Mandatory: Indicates an item that is required to be implemented as defined in this document.

3.4.3 May: Indicates flexibility of choice with no implied preference.

3.4.4 Optional: Features that are not required to be implemented by this document. However, if any optional feature defined by this document is implemented, it shall be implemented as defined in this document.

3.4.5 Shall: Indicates a mandatory requirement.

3.4.6 Should: Indicates flexibility of choice with a preferred alternative; equivalent to the phrase “it is recommended”.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

3.5 Conventions

Certain words and terms used in this American National Standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in 3.1 or in the text where they first appear. Names of signals are in all uppercase (e.g., DT DATA IN), lower case is used for words having the normal English meaning.

All parametric data are specified in terms of fundamental MKSA units - meters, kilograms, coulombs, seconds - and their derivatives - ohms, henrys, mhos, farads, volts, amperes, etc.

Numbers that are not immediately followed by lower-case b or h are decimal values.

Numbers immediately followed by lower-case b (xxb) are binary values.

Numbers immediately followed by lower-case h (xxh) are hexadecimal values.

Numbers immediately followed by a lower-case n (xxn) are a specific signal in a connector.

Numbers immediately followed by an upper case N’ (xxN’ - pronounced "xxN primed") are a specific connector number.

Decimals are indicated with a comma (e.g., two and one half is represented as 2,5).

Decimal numbers having a value exceeding 999 are represented with a space (e.g., 24 255).

An alphanumeric list (e.g., a, b, c or A, B, C) of items indicate the items in the list are unordered.

A numeric list (e.g., 1,2,3) of items indicate the items in the list are ordered (i.e., item 1 shall occur or complete before item 2).

In the event of conflicting information the precedence for requirements defined in this standard is:

1) text,
2) tables, then
3) figures.

3.6 Specification of measurement equipment

Requirements for measurement equipment is called out by reference to specific manufacturer and model in some cases because specification of all the equipment performance requirements is impractical in this document. Any equipment so specified is replaceable by equipment from other manufacturers if the performance of the equipment is substantially equivalent.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

4 Overview

4.1 General

This clause defines the relationship between the constituent parts of a passive SCSI interconnect and the measurements required to verify the performance of the interconnect.

4.2 Open vs. closed systems related to this standard

Open systems are those where all the components with interoperability points may be supplied by different suppliers and the resulting configuration is expected to meet the requirements at all interoperability points.

Closed systems are those that are comprised of components that nominally are similar to those used in open systems but where the exact parts used are always assembled in the same combination and in the same configuration and usually are the same part number from the same supplier.

Open systems require specification at all interoperability points (typically connectors) for any component. Closed systems only require that the signal received at the device meet the specification. Closed systems are much simpler to specify since the only requirement is the received signal.

This standard is focused on the open system assumption with the further restriction that open concatenated systems are not included in this standard. Open concatenated systems are those that allow connection of dissimilar passive interconnects (e.g. flat to round cable, cable to backplane, etc.) and specify the performance requirements at other than port to port interoperability points. Closed concatenated systems are comprehended within this standard if the closed system is capable of be accessed with the test fixtures and calibration procedures defined for the open system requirements. An example of a closed concatenated system is the cable assembly to passive backplane construction. In this configuration there are no requirements specified at the cable/backplane interface by SCSI standards unless an active SCSI expander port is present at that interface in which case the backplane/cable assembly connector is a SCSI device connector (the device being the expander). With the expander present, the system becomes an open system and both the cable assembly and the passive part of the backplane are separately covered by this document. See also 4.6.

4.3 Structural considerations

4.3.1 SCSI interconnects

The collection of wires, connectors, and circuits that form the electrical path between SCSI device connectors are SCSI interconnects. If the path between the SCSI device connectors does not contain any expanders or other active circuits the interconnect is passive. This standard addresses only passive SCSI interconnects.

This clause defines the structural variations of the interconnect and the physical measurement points to be used. In general, passive SCSI interconnects are complex multi-port circuits whose performance is considered from every initiator connector in the interconnect assembly to every target connector in the interconnect assembly. Requirements are also specified for connectors that support only SCSI bus segment termination.

Performance requirements for interconnect assemblies are limited to configurations that do not contain any bus segment path connectors except those within a stub length of the end of the SCSI bus segment (at the terminator). The following constitute the basic building blocks of passive interconnect:

a) conductors (wire and backplane)
b) connectors
c) transition regions (connector termination / comb out / lacing regions / vias)

Interconnect that contains enabled integral terminators are addressed in this standard even though the terminators themselves are active components and, strictly speaking, make the interconnect non-passive. If enabled integral terminators exist, the enabled integral terminators eliminate the requirement for using a standard load with an enabled terminator in that position. See 4.9.2. For interconnect that contains disabled terminators the disabled terminator shall be considered as part of the interconnect assembly under test.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

All measurements are specified through a mated connector. This means that the test fixture specification is critical since part of the tested interconnect remains with the test environment and part is removable with the interconnect assembly under test.

4.3.2 SCSI passive interconnect topology

SCSI interconnects have an N'-port construction where every connector is a possible SCSI device port and all ports are directly connected to each other in a multidrop topology. Since SCSI is a parallel bus every connector also contains a multiplicity of signal level ports (one for every differential signal).

A SCSI passive interconnect is characterized by the number of connectors and the number of signals. n ranges from 1 to 27. N' is determined by the structure of the passive interconnect and ranges from 2 to 18 (16 devices + 2 terminators). A SCSI passive interconnect may contain up to 18 x 27 = 486 signal level ports.

4.3.3 Interconnect sub-assemblies, transition regions, and bulk cable

A passive interconnect with the connectors removed is termed an interconnect sub-assembly.

Transition regions are parts of an interconnect assembly between the uniform part of the bulk cable and the connector attachment. The term "multidrop" is used to describe constructions that have transition regions in addition to those needed to attach the end connectors. Examples of interconnect sub assemblies are: twist and flat, round cable prepared for termination to connectors, and printed circuit boards without connectors.

Bulk cable is the collection of conductors and associated insulation used between the connectors or non-permanent transition regions (e.g. comb out) in a passive SCSI interconnect. Non-permanent transition regions are not part of bulk cable. Bulk cable includes permanent transition regions (e.g., flat regions used in twist and flat type bulk cable) designed for purposes of enabling connector attachment. The term bulk cable refers to physically flexible conductors and is not used to describe printed circuit boards. Printed circuit boards without connectors are included under separate headings in the clauses associated with multidrop bulk cable due to the permanent transition regions on PCB's.

Bulk cable with permanent transition regions may also be a subassembly for some interconnect assembly designs.

This document only considers the performance requirements for complete interconnect assemblies and interconnect subassemblies that have permanent transition regions.

The term "media" is not used to refer to bulk cable or any other construction addressed in this document. Similarly, the concept of "non-uniform media" does not accurately describe the situation with multidrop constructions and is also not used herein. The term "cable sub-assembly" is used to describe bulk cable that has been modified to accommodate the next higher level of assembly, typically connectors.

4.3.4 Interconnect assemblies

An interconnect with connectors installed is termed an interconnect assembly. Each SCSI connector shall be identified by all the functions listed in 4.9.1 that the connector is expected to support in service. This requirement may be more restrictive than allowed by the SCSI architecture model (SAM). SAM allows all SCSI ports to have either the initiator role or the target role or both roles. However, in practice most SCSI ports implement only one role.

4.3.5 Relationship between SE and DF in this document

SE (single ended) and DF (differential) requirements are contained in this document, described in table 1.

Table 1 - SE and DF map

	Bulk cable	Interconnect assembly
SE	Annex A	NA
DF	Clause 5, Clause 6 and Clause 7	Clause 8, Clause 9 and Clause 10

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

4.4 Relationship between requirements on bulk cable and requirements on interconnect assemblies

Performance requirements on interconnect assemblies are dictated by the signal requirements specified in SPI-x at the connectors. Bulk cable testing alone does not guarantee that interconnect assemblies made using the bulk cable meet the SPI-x requirements.

Separate performance specifications for bulk cable that are independent from the interconnect assembly are defined in this document for purposes of enabling multi sourcing for bulk cable and for allowing statements of compliance for bulk cable.

Interconnect assemblies are not required to use bulk cable that conforms to the requirements for bulk cable as long as the performance of the interconnect assembly meets its requirements.

However, the signal quality loss, the propagation time and propagation time skew, the impedance, and the cross talk are significantly determined by mechanisms intrinsic to the bulk cable.

4.5 Physical measurement points

For bulk cable the performance specifications shall be measured at the point of attachment of the stripped conductors to the test fixture. For the interconnect assemblies the performance specifications shall be measured through the mated connectors.

4.6 Concatenated configurations

Bus segments comprised of multiple interconnect assemblies connected together with one or more bus path connectors shall be termed concatenated configurations. Examples of concatenated configurations include: round cable to round cable (similar) connected together through a connector, round cable to flat cable (dissimilar) connected together with a connector, shielded cable connected to backplane with no expander on the backplane near the connector (dissimilar), and other combinations of construction. The performance of concatenated SCSI bus segments is not guaranteed by each of the constituent interconnect assemblies meeting the requirements in a non-concatenated configuration.

Interoperability points - described in 4.7 - shall be not specified at bus path connectors in concatenated configurations. If the point of connection between the sections of dissimilar physical construction is permanent, then the interconnect assembly for the entire SCSI bus segment may be treated as a single interconnect assembly whose performance requirements are addressed by this document.

4.7 Interoperability points

Interoperability points are physical points in the system where performance requirements exist at separable connectors and where it is required that the components on either side of the connector may be supplied from different compliant vendors. Interoperability points only apply to interconnect assemblies.

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

Following is a sample list where interoperability might be expected in a SCSI segment. A “Y” following the position designation means that this is considered an interoperability point in this standard. Similarly, a “N” following the position designation means that the point is not considered an interoperability point in this standard.

a) Disk drive connector mounted directly on the disk drive (Y)
b) HBA connector external connector with no internal cable on the same segment (Y)
c) HBA internal SCSI connector to internal cables with no external cable on the same segment (Y)
d) Motherboard SCSI connector where the mother board contains the HBA (in an ASIC) on board (Y)
e) Backplane connector that directly accepts a disk drive or other SCSI device (Y)
f) Backplane connector that directly connects an external cable assembly to an expander on the backplane (Y)
g) External cable assembly connector that connects to an external connector of an HBA with no internal cable on the same segment (Y)
h) External cable assembly connector that connects to an external connector of a disk drive array containing an expander immediately behind the external connector (Y)
i) Internal cable connector that directly connects to a disk drive or other SCSI device. (Y)
j) Connectors that have a separable terminator attached (Y).
k) HBA internal SCSI connector to the mother board (N)
l) External connector to a box that has external cable assembly attached and an internal cable assembly attached to the same connector (including the case where a short cable assembly is used between the HBA and the bulkhead in a PC-like packaging. (N)
m) Internal cable assembly connector for a short cable assembly used between the disk drive and the backplane (N)
n) HBA external bulkhead connector and internal connector when both internal and external cables are attached (N)
o) External cable assembly connector and backplane connector when the external cable assembly is attached directly to a backplane (N)

4.8 Constructions considered

This document addresses the performance of the following types of constructions. Other constructions may also be measured using similar procedures.

Point-to-point bulk cable:
- flat planar (ribbon)
- unshielded round
- shielded round *

Multi-drop bulk cable or printed circuit boards (unpopulated)
- twisted and flat planar (ribbon) *
- unshielded round
- printed circuit boards *

Point-to-point interconnect assemblies:
- two connector shielded *
- two connector unshielded

Multi-drop interconnect assemblies:
- multi-connector cable (e.g. external daisy chain)
- backplanes: (multi-connector) *

*most common constructions

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

4.9 Identification, constraints and loading requirements

4.9.1 Connector function identification

All connectors in the interconnect assembly shall be identified as one or more of the following 14 functions:

a) open
b) transmitter for initiator device with enabled terminator
c) receiver for initiator device with enabled terminator
d) transmitter for initiator device with no enabled terminator
e) receiver for initiator device with no enabled terminator
f) transmitter for target device with enabled terminator
g) receiver for target device with enabled terminator
h) transmitter for target device with no enabled terminator
i) receiver for target device with no enabled terminator
j) enabled terminator only
k) feed through enabled terminator with transmitter for initiator device with no enabled terminator attached on the other side of the terminator
l) feed through enabled terminator with receiver for initiator device with no enabled terminator attached on the other side of the terminator
m) feed through enabled terminator with transmitter for target device with no enabled terminator attached on the other side of the terminator
n) feed through enabled terminator with receiver for target device with no enabled terminator attached on the other side of the terminator

4.9.2 Constraints

The following configurations are used for specifying the level 1 tests in this standard:

a) Point to point shielded
b) Unshielded multidrop bulk cable up to 3 m, up to 16 drops
c) Multidrop backplanes up to 16 drops

This document does not consider configurations where another interconnect assembly is attached to a connector in the interconnect assembly under test. Concatenated configurations are not considered - for example: round cable to flat; shielded cable to backplane with no expander; shielded round to shielded round etc. are all concatenated configurations.

Each function for each connector requires a specific load to be in place during the interconnect assembly testing process - see 4.9.1.

The position of the enabled terminators shall be defined for every measurement of interconnect assembly performance. The standard load appropriate for the connectors with the enabled terminators attached shall be attached. Loading conditions for the remaining connectors in the interconnect assembly under test shall meet both of the following requirements:

a) All SCSI device ports not attached to devices with enabled terminators have a standard load appropriate for the function of the connector in place during the measurement
b) Any one target port not attached to devices with enabled terminators shall have the standard load removed to simulate hot plugging conditions

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

4.9.3 Standard loads

4.9.3.1 Targets and initiators with no enabled terminator

Standard loads for targets and initiators with no enabled terminator shall have the following properties:

a) be identified by the connector type, SCA-2, VHDCI, or HD68,
b) be optimized for SPI-5,
c) the capacitance at the connector interface shall be held to a tolerance of ± 1,0 pF at the connector,
d) the nominal signal to ground capacitances of the various portions of the standard load shall be
   - 2 pF for the connector,
   - 2 pF for the trace,
   - 1 pF for the via/pad, and
   - 6 pF the chip input capacitance,
e) the nominal signal to signal capacitance shall be 6,0 pF,
f) the distance from connector interface to chip capacitance shall be 37,5 mm ± 2,0 mm, and
g) the PCB impedance shall be 122 Ω ± 10 Ω and shall match the SPI-5 specification.

4.9.3.2 Targets and initiators with enabled terminator

Standard loads for initiators and targets with an enabled terminator shall have the following properties:

a) be identified by the connector type, SCA-2, VHDCI, or HD68,
b) be optimized for SPI-5,
c) the capacitance at the connector interface shall be held to a tolerance of ± 1,0 pF at the connector,
d) the nominal signal to ground capacitances of the various portions of the standard load shall be:
   - 2 pF for the connector,
   - 2 pF for the trace,
   - 1 pF for the via/pad,
   - 6 pF for the chip input capacitance, and
   - 3 pF for the terminator,
e) the nominal signal to signal capacitance shall be 9,0 pF,
f) the distance from connector interface to chip capacitance shall be 47,5 mm ± 2,0 mm,
g) the distance from the connector interface to the terminator shall be 27,5 ± 2,0 mm, and
h) the PCB impedance shall be 122 Ω ± 10 Ω and shall match the SPI-5 specifications.

4.10 Nature of requirements

4.10.1 Measurements and tests

A measurement is the process of acquiring data that indicates a property of the bulk cable or interconnect assembly of interest. A test is a measurement to which a pass-fail criteria is applied.

4.10.2 Performance levels and applications

Several parameters are required to verify electrical performance. Measurement of passive interconnect performance is divided into two levels:

a) level 1: those used to verify compliance to the requirements set forth in SPI-x or in this document, and
b) level 2: those needed to aid in the diagnosis of the causes of degraded performance, to set up the conditions for executing a level 1 measurement, or as additional characterization of the interconnect but are not required for specification compliance.

Since level 1 measurements are intended to determine compliance to requirements, and performance level all level 1 measurements are tests as defined above. No level 2 measurements are tests.

--`,,```,,,,````-`-`,,`,,`,`,,`---
Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

Each measured parameter of a bulk cable or an interconnect assembly is either level 1 or a level 2. In some cases a parameter may be needed solely for creating a mathematical model for the component in which case it is neither level 1 nor level 2. This standard recognizes that this parameter class exists but no details for measurements that relate only to component modeling are included.

Table 3 and Table 8 list the required level 1 tests. The same parameter may have different uses for bulk cable and interconnect assembly. For example, the parameter 'differential insertion loss' is a level 1 measurement for bulk cable and has applicability to modeling. The parameter 'differential insertion loss' for an interconnect assembly is still a level 1 measurement but only for the purposes of validating another interconnect assembly parameter and with different criteria for the requirement and is of less interest for modeling.

Emphasis is placed on the level 1 measurements and required performance levels - tests. The level 2 measurements are briefly described in this document for reference but no performance requirements are specified except in the case where the level 2 measurement is needed to set up a different level 1 measurement.

4.10.3 Basic performance requirements for interconnect assemblies

4.10.3.1 Overview

This sub clause defines the basic performance requirements for interconnect assemblies. In all cases the driver signal properties shall be measured with a compliant SCSI terminator attached to the driver connector no further than 100 mm from the driver connector. If a SCSI device is used for the driver the terminator may be part of the companion target or initiator device that is used to allow the driver device to operate.

There are five basic requirements for interconnect assemblies:

a) deliver adequate signal quality to all receivers from all drivers with worst case drivers
b) limit the creation of pair to pair skew to specified levels
c) limit the propagation time from end to end to specified levels for any pair
d) deliver transmission line impedance including that influenced by connectors and assembly processes within specified levels
e) limit the creation of common mode signals to specified levels.

For signal quality measurements each port in the interconnect assembly shall be characterized by:

a) the signal launched into the port, and
b) the signal transferred to the port from other ports in the cable assembly.

Signals delivered to every interconnect assembly port identified as a receiver shall be measured under the following conditions:

a) the most degraded allowed signal is launched from every other interconnect assembly port, one at a time,
b) the most aggressive noise sources are present on all other interconnect assembly ports that couple into the port under test,
c) resonant conditions are within acceptable bounds
d) all loading conditions defined for the receive port
e) standard loads present on all other ports not acting as driver or receiver in the specific measurement

The signal quality shall meet at least the minimum requirements for a received signal under these conditions. The signal quality at the connector of the receiving SCSI device shall satisfy the requirements for both precomp and non-precomp drivers specified in SPI-4 as well as the receive signal requirements in SPI-2, SPI-3, and SPI-5 for non-precomp drivers.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

4.10.3.2 Measurement conditions for non-precomp received signal quality requirements

The following conditions shall be present for measuring received signals when using non-precomp transmitters:

a) The pair under test (victim for cross talk) launched signal shall have 740 mV_{pp} ± 50 mV.
b) The preferred rise time is 1,0 ns ± 0,1 ns if possible by adjusting the driver used for the measurement. If it is not possible to meet this rise time use the fastest available from the driver chip but not less than 0,9 ns.
c) Aggressor lines used to generate cross talk noise shall be driven by drivers on the same integrated circuit as the driver for the pair under test (victim) and shall have the same nominal launch conditions as the driver for the pair under test.
d) Max allowed jitter is present in launched signal or the receiver requirements are additively adjusted to account for max launch jitter if max jitter is not present in launch signal used for the test. For example, if the launched signal has 50 ps less jitter than allowed, then 50 ps is added to the receive signal limits to account for the launched signal being better than worst case.
e) The data pattern running during the testing shall be 2^n-1 where n is 7 or higher.

4.10.3.3 Measurement conditions for precomp received signal quality requirements

The following conditions shall be present for measuring received signals when using precomp transmitters:

a) The launched signal on the pair under test shall use 33 % cutback (max amplitude minus 33 %) with a weak driver at 740 mV_{pp} ± 50 mV.
b) The preferred rise time is 1,0 ns ± 0,1 ns, if possible, by adjusting the driver used for the measurement. If it is not possible to meet this rise time use the fastest available from the driver chip but not less than 0,9 ns.
c) Aggressor lines used to generate cross talk noise shall be driven by drivers on the same integrated circuit as the driver for the pair under test (victim) and shall have the same nominal launch conditions as the driver for the pair under test including the same precomp properties.
d) Max allowed jitter is present in launched signal or the receiver requirements are additively adjusted to account for max launch jitter if max jitter is not present in launch signal used for the test. For example, if the launched signal has 50 ps less jitter than allowed, then 50 ps is added to the receive signal limits to account for the launched signal being better than worst case.
e) The data pattern running during the testing shall be 2^n-1 where n is 7 or higher.

4.10.4 Deriving the launch signal requirements for this standard from the signal requirements in SPI-x

SPI-x defines signal requirements at SCSI device connectors that contain drivers and receivers. SPI-x defines the transmit signal at the device connector into an idealized test load. There is no explicit requirement on the output impedance of the transmitter. For the receiver specification, the signal is specified at the device connector of the device containing the receiver. If the receiver device contains an enabled terminator then the input impedance, the capacitance and the leakage are all specified by SPI-x. Receivers in devices with enabled terminators have reduced stub length compared to those without enabled terminators. If the receiver device does not contain an enabled terminator only the capacitance and leakage are specified by SPI-x.

In order to accommodate the requirements of measuring passive interconnect assemblies it is necessary to translate the requirements for the transmit signals specified in SPI-x to a form that is usable for interconnect assemblies.

Current launched into mid-segment connectors is split evenly in both directions away from the connector while current launched into end connectors is split evenly between current transmitted into the interconnect assembly and current transmitted into the terminator. This allows nominally the same requirements to apply for the interconnect assembly performance regardless of the position of the connector containing the driver. It also reinforces the need for identifying each connector in the interconnect assembly in terms of its function (initiator, target, terminator).

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

A standard load shall be present on the connector of the device containing the receiver.

In all cases involving level 1 signal quality measurements that activity on signals other that the signal under test shall be present during the measurement.

4.11 Local neighborhood concepts

For signals, the basic idea is to not test for interactions that are insignificant to the port under test. For example in a flat cable, signals removed from the signal under test by at least 5 signal pairs do not significantly couple into the signal under test and do not need to be considered. The level of interaction deemed to be significant is left to be defined. For physical constructions the dimensional precision within which the construction shall be considered identical is 1/10 of the rise length of the fastest signal to be used in the interconnect. For a 1 ns rise time in twisted pair media, 1/10 of the rise length is approximately 25 mm. In other words, two connectors placed 100 mm apart (4 rise lengths) have local neighborhoods that do not significantly overlap. Similarly, if two connectors are less than 25 mm apart on the same cable they share a common rise length and the effects of both connectors may be considered from a lumped perspective. This standard requires measurement from only one of these closely spaced connectors (except for basic opens and shorts).

4.12 Length specifications

The length of the interconnect, if used in a sample description, may have a special meaning in this document. There are different ways to specify length for the same interconnect assembly. For example, it may require 31,4 m of wire to produce a cable assembly with 30,5 m overall connector to connector path length. This is caused by the twisting process used to form the pairs and the overall twist applied to the collection of pairs in a bulk cable. The electrical length is also important where the propagation time is part of the interest for the specification. The following is the way that this standard considers length issues:

Length parameters are separated into two types, both of which shall be specified:

a) the physical length along the geometrical center line (e.g. center line of the jacket for round cables to the center line of the unmated connector) of the completed cable assembly (not necessarily the actual wire length for any specific conductor)
b) the propagation time between electrical access points (typically connectors) in the cable assembly.

Other lengths, such as those internal to the bulk cable which may be important for creating accurate models, are not used as descriptors in this standard.

4.13 S21 relationship among point to point and multidrop configurations

The relationship of insertion loss (scattering parameter S21) is significantly different for different interconnect constructions.

Figure 1 shows the basic S21 relationships for three common configurations:

a) uniform bulk cable used in point to point applications
b) interconnect subassemblies (non-uniform bulk cable and unpopulated backplanes (no connectors)) used for multidrop applications
c) populated (with loads) multidrop cable assemblies and backplanes

The idealized curves in Figure 1 are based on using a maximum multi-drop cable assembly length of 3 m in non-concatenated applications. For point to point interconnect assemblies the maximum length is assumed to be 25 m. The point to point losses are assumed to be the same for the interconnect assembly and the bulk cable because of the dominance of the bulk cable losses with only end connectors and no loads.

The losses for the multidrop configurations are assumed to be significantly caused by resonant effects due to the loads and non-uniformities. More allowance is made for multidrop cable assemblies than for point to point cable assemblies. Due to the assumed short length for multidrop applications less primary wire loss is expected. The budget for accommodating the resonant losses comes from this lower primary wire losses in the shorter lengths for multidrop.

The low frequency losses are also less for the multidrop applications due to the assumed shorter length.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

These performance requirements are independent of length and apply to all physical constructions including backplanes.

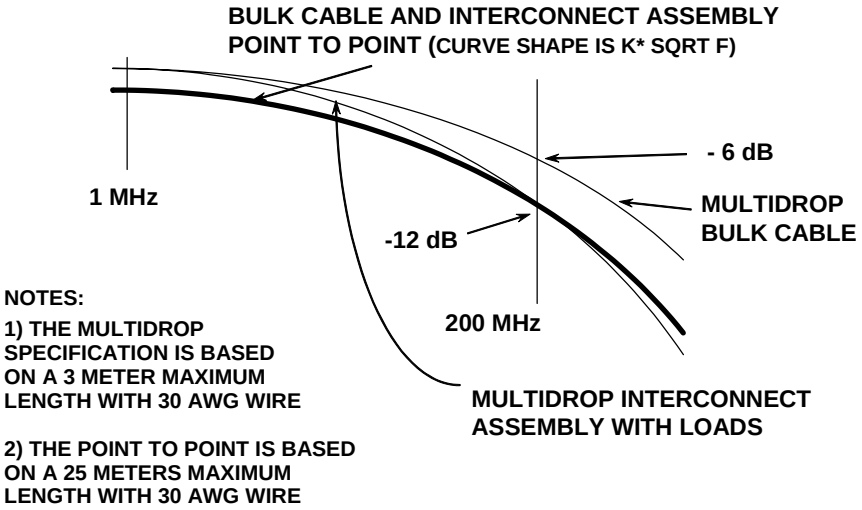


Figure 1 - Relationship between S21 for different configurations

4.14 Accommodation of receiver compensation in interconnect requirements

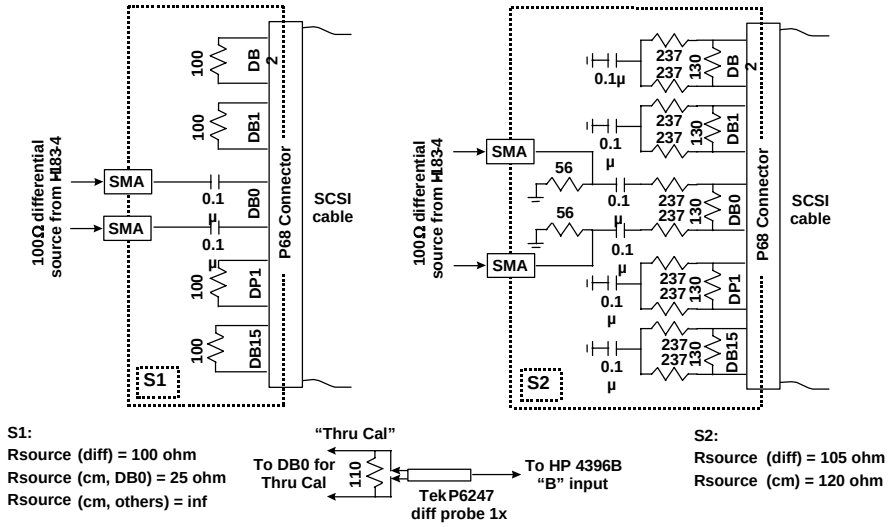
There is no allowance in the interconnect performance for margin that may exist by virtue of signal processing schemes executed in the receiver except as provided by SPI-4 and SPI-5 for pair to pair skew and by the required signal quality performance limits specified in SPI-4 and SPI-5. Interconnect performance specifications in this standard require that both the precomp driver and the non-precomp driver specifications be met for SPI-4 applications. This is required because this standard is addressing only open interconnect where the state of the driver is not known to the interconnect.

4.15 Instrumentation and text fixture considerations

This standard addresses performance at frequencies up to 650 MHz. Evidence exists that in this frequency range test fixtures and instrumentation severely affects the measurement accuracy if not designed and used properly. Details for the test fixture and instrumentation requirements are contained in the specific clauses.

An example of a high level description of a test set up is shown in figure 2.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale



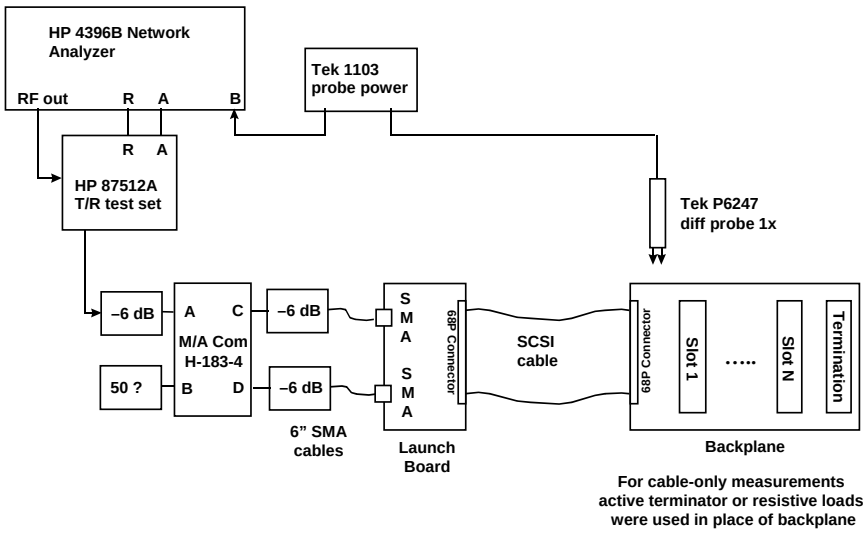


Figure 2 - Example cable/backplane frequency response test setup

4.16 Signals covered by this standard

Table 2 lists the signals covered and not covered by this standard. The signals not covered by this standard may be important for creating accurate models but are not required to meet the requirements specified for local impedance, capacitance, propagation time, NEXT, insertion loss, or signal degradation. The signals listed as not covered by this standard shall meet basic requirements for opens, shorts, and d.c. resistance as defined in SPI-x

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS
Not for Resale

Table 2: Signals covered by this standard

Applicability to this standard	Contact#	Signal	Contact#	Signal
YES	1	DB12 +	35	DB12 -
YES	2	DB13 +	36	DB13 -
YES	3	DB14 +	37	DB14 -
YES	4	DB15 +	38	DB15 -
YES	5	PARITY 1 +	39	PARITY 1 -
YES	6	DB0 +	40	DB0 -
YES	7	DB1 +	41	DB1 -
YES	8	DB2 +	42	DB2 -
YES	9	DB3 +	43	DB3 -
YES	10	DB4 +	44	DB4 -
YES	11	DB5 +	45	DB5 -
YES	12	DB6 +	46	DB6 -
YES	13	DB7 +	47	DB7 -
YES	14	PARITY 0 +	48	PARITY 0 -
NO	15	GROUND	49	GROUND
NO	16	DIFFSENSE	50	DIFFSENSE / GND
NO	17	TERMPWR	51	TERMPWR
NO	18	TERMPWR	52	TERMPWR
NO	19	RESERVED	53	RESERVED
NO	20	GROUND	54	GROUND
YES	21	ATN +	55	ATN -
NO	22	GROUND	56	GROUND
YES	23	BSY +	57	BSY -
YES	24	ACK +	58	ACK -
NO	25	RST +	59	RST -
YES	26	MSG +	60	MSG -
YES	27	SEL +	61	SEL -
YES	28	C/D +	62	C/D -
YES	29	REQ +	63	REQ -
YES	30	I/O +	64	I/O -
YES	31	DB8 +	65	DB8 -
YES	32	DB9 +	66	DB9 -
YES	33	DB10 +	67	DB10 -
YES	34	DB11 +	68	DB11 -

--`,,```,,,,````-`-`,,`,,`,`,,`---
Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS
Not for Resale

4.17 Error rate considerations

Error rate, or error ratio, is the frequency of bit errors compared to time of operations or to the number of bits transmitted. Some interconnect systems allow for finite limits on the allowed error rate. There is a trade-off between the amount of time used to sample a measurement and the likelihood of detecting an error event. If only very short sampling time is used then it is likely that error producing signal properties may not be detected. At the other extreme is very long sampling times where events not caused by the interconnect, such as shift in environmental conditions or external system noise e.g. lightning, also contribute to the error population.

Relatively low population SCSI system errors attributable to interconnect performance are affected by resonant conditions set up by specific data patterns and by cross talk noise. Serial links and optical systems typically use phase lock loop and high gain amplifier methods that produce significant amounts of Gaussian (unbounded) noise. The Gaussian noise sources produce an expectation of finite error rates in properly functioning systems. However, the driver and interconnect portions of a parallel SCSI systems using up through SPI-5 have extremely low Gaussian noise content with the consequence that there is no expectation of finite error rate for properly designed and built systems.

The requirements for measuring the signal quality include all active noise sources being on in their most aggressive mode during the measurement and using specific data patterns that may excite resonance. These noise sources and resonances are deterministic, not Gaussian. By measuring for sufficient time to expose the effects of the deterministic noise the desired performance for the interconnect is captured. Level 1 measurements in this document shall be done in a way that allows sufficient time for all non-Gaussian contributors to noise to be sampled.

The only allowed error rate for level 1 signal quality measurements in this document is zero.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

5 Summary bulk cable

This clause provides a summary of the level 1 and level 2 measurements that apply to bulk cable. Table 3 shows the level 1 measurements and table 4 shows the level 2 measurements. Most level 2 measurements in table 4 are listed for reference without further description in this document. Selected level 2 measurements are described in more detail than provided in table 4.

Table 3 - Bulk cable level 1 test summary

Test parameter	Level	Clauses	Domain	Condition	Comments
Differential local impedance	1	7.2	T	t_r = 1 ns	TDR - TEK 11801or equivalent
Differential capacitance	1	7.4, 7.5	T or F	t_r = 1 ns (T) 100 kHz and 1 MHz (F)	Impedance analyzer measurement (point to point) -- Calculated from TDR/ TDT (multidrop)
Differential propagation time	1	7.3	T	at signal transition midpoint	TDT - TEK 11801or equivalent
Differential propagation time SKEW	1	7.3	T	T_{pmax}-T_{pmin} for all pairs	Pair to pair
Differential insertion loss	1 for point-to-point 2 for multi-drop	7.6	F	S21 - sweep from 10 MHz through 650 MHz[1]	All signal pairs Network analyzer - Agilent 8753x or equivalent
Differential NEXT	1 for point-to-point 2 for multi-drop	7.7	T	Single pulse, maximum allowed amplitude, minimum STD time[2]	Tektronix 11801 with TDR or equivalent, sum of all aggressors measured one at a time with all others terminated
SE local impedance	1	Annex A	T	tr=3 ns	TDR - TEK 11801or equivalent
SE Capacitance	1	Annex A	F	100 kHz and 1 MHz	LCR meter

1 - S12 and S21 are scattering parameters that relate the incident and transmitted voltage waves in a two-port circuit.
2- STD: Signal Transition Duration

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

Table 4 - Bulk cable level 2 measurement summary

Test parameter	Level	Domain	Condition	Comments
Extended Distance Impedance (Differential)	2	F	Sweep from 30 MHz through 600 MHz	Network analyzer - Agilent 8753x or equivalent (This was a level 1 requirement in SPI-x)
Common mode impedance	2	T		Treat each pair as a single conductor - grounding shall be specified
Common mode capacitance	2	F		Treat each pair as a single conductor - grounding shall be specified
Eye diagrams (signal degradation within the pair)	2	T		One pair active
Differential to Common mode conversion	2	T		Signal- to-signal balance within the pair (sum of the + signal and the - signal)
Insertion loss skew (pair to pair)	2	F		Difference in voltage transfer function between pairs in dB
ACR (attenuation [insertion loss] to cross talk ratio)	2	F		
FEXT (far end cross talk)	2	T		Tektronix 11801 with TDR or equivalent
Rise time degradation	2	T		
Dielectric constant variation w/ frequency	2		Sweep from 300 KHz through 600 MHz	Network analyzer - Agilent 8753x or equivalent (This was a level 1 requirement in SPI-x)

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS

Not for Resale

6 Bulk cable samples, test fixtures and setups

6.1 Bulk cable samples and sample preparation

6.1.1 Overview

Bulk cable requires special preparation of samples to gain electrical access. For example conductors shall have the insulation removed and conductors shall be separated to allow connection to test fixtures. A major goal of sample preparation is minimal disturbance to the construction for measurement purposes. See 6.1.4.2 for PCB sample preparation.

6.1.2 Summary

Table 5 - Bulk cable sample preparation

Measurement	Construction	Point-to-point sample type (See 6.1.3.1 or 6.1.3.2)	Multi-drop sample type (See 6.1.4.1 or 6.1.4.2)
Differential local impedance	Flat planar	SP_Bulk_PP3	SP_Bulk_MD3
	Unshielded round	SP_Bulk_PP3	SP_Bulk_MD3
	Shielded round	SP_Bulk_PP3	NA
Differential propagation time and differential propagation time skew	Flat planar	SP_Bulk_PP10	SP_Bulk_MD3
	Unshielded round	SP_Bulk_PP10	SP_Bulk_MD3
	Shielded round	SP_Bulk_PP10	NA
Differential capacitance (calculation for TDR/TDT, measurement for F)	Flat planar	SP_Bulk_PP3	SP_Bulk_MD3
	Unshielded round	SP_Bulk_PP3	SP_Bulk_MD3
	Shielded round	SP_Bulk_PP3	NA
Insertion loss	Flat planar	SP_Bulk_PP25	NA
	Unshielded round	SP_Bulk_PP25	NA
	Shielded round	SP_Bulk_PP25	NA
NEXT	Flat planar	SP_Bulk_PP10	SP_Bulk_MD3
	Unshielded round	SP_Bulk_PP10	SP_Bulk_MD3
	Shielded round	SP_Bulk_PP10	NA

6.1.3 Point to point bulk cable

6.1.3.1 Point to point bulk cable sample preparation (SP_Bulk_PP3)

Applies to differential local impedance and frequency domain capacitance.

1) Cut sample length to 3 m ± 0,025 m
2) Remove 40 mm of outer jacket from one end (if jacket is present)
3) Remove 40 mm of overall shield from one end (if overall shield is present)
4) Trim tape materials to the base of jacket/shield (if tape materials are present)
5) Remove any filler that might interfere with the tests
6) Strip 5 mm maximum insulation from all conductors on one end
7) Except for conductors being tested, all other conductors are left floating

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

6.1.3.2 Point to point bulk cable sample preparation (SP_Bulk_PP10)

Applies to NEXT, propagation time, propagation time skew, and calculated capacitance

1) Cut sample length to 10 m ± 0,025 m
2) Remove 40 mm of outer jacket from both ends (if jacket is present)
3) Push back the overall shield from both ends (if overall shield is present)
4) Trim tape materials to the base of jacket/shield (if tape materials are present)
5) Remove any filler that might interfere with the tests
6) Strip 5 mm maximum insulation from all conductors on both ends
7) If twisting is present in pairs, untwisting for measurement purposes shall be minimized
8) All conductors except those for the pair under test are left floating except when used for NEXT
9) Ground the shield on both ends except for NEXT.

6.1.3.3 Point to point bulk cable sample preparation (SP_Bulk_PP25)

Applies to insertion loss

1) Cut sample length to 25m ± 0,1 m
2) Remove 40 mm of outer jacket from both ends (if jacket is present)
3) Remove 40 mm of overall shield from both ends (if overall shield is present)
4) Trim tape materials to the base of jacket/shield (if tape materials are present)
5) Remove any filler that might interfere with the tests
6) Strip 5 mm maximum insulation from all conductors on both ends
7) If twisting is present in pairs, untwisting for measurement purposes shall be minimized
8) Except for conductors being tested, all other conductors are left floating

6.1.4 Sample preparation for multi-drop bulk cable or printed circuit boards

6.1.4.1 Multi-drop bulk cable sample preparation (SP_Bulk_MD3)

This sub clause applies to constructions having areas prepared for connectorization with constant intervals between all adjacent areas. For example in a twisted flat design the interval between the flats is constant. These constructions may be either planar or round. Other non-uniform constructions are also within this scope. Only unshielded multidrop bulk cable is considered in this document.

Samples for constructions with different intervals between flats shall be specified in terms of specific flat sections used for termination. See Annex D for guidance concerning non-constant intervals.

If measuring only differential local impedance or NEXT, only one end of the sample needs to be prepared.

1) Cut sample length to 3m nominal. First cut shall be at the approximate center of a flat section. If preparing both ends, it is permitted to cut > 3m (but as close to 3m as possible) to permit the second cut to be at the approximate center of a flat section. Record the distance between the ends of the sample as measured on a flat surface with a scale. (This distance is required for propagation time (ns/m) and differential capacitance (pF/m) calculations.)
2) Remove 50 mm of outer jacket from both ends (if jacket is present)
3) Trim tape materials to the base of jacket (if tape materials are present)
4) Remove any filler that might interfere with the tests
5) Strip 5 mm maximum insulation from all conductors at both ends
6) Except for conductors being tested, all other conductors are left floating

6.1.4.2 Printed circuit boards sample preparation

No sample preparation is required. Electrical access is ~~to features~~ designed into the PCB for this purpose.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

6.2 Bulk cable and printed circuit board test fixture specifications

6.2.1 Overview

Test fixtures are the hardware that enables connection of the sample under measurement to the instrumentation. Test fixtures are required for every measurement specified in this document. See table 6.

6.2.2 Summary

Table 6 - Bulk cable and printed circuit board test fixtures

Measurement	Construction	Fixture for point-to-point samples	Fixture for multi-drop samples
Differential local impedance	Flat planar	FIX_Bulk_1 (6.2.3)	FIX_Bulk_1 (6.2.3)
	Unshielded round	FIX_Bulk_1 (6.2.3)	FIX_Bulk_1 (6.2.3)
	Shielded round	FIX_Bulk_1 (6.2.3)	NA
	Printed circuit board	NA	FIX_PCB_1 (6.2.7)
Differential propagation time and differential propagation time skew (calculation)	Flat planar	FIX_Bulk_1 (6.2.3)	FIX_Bulk_1 (6.2.3)
	Unshielded round	FIX_Bulk_1 (6.2.3)	FIX_Bulk_1 (6.2.3)
	Shielded round	FIX_Bulk_1 (6.2.3)	NA
	Printed circuit board	NA	FIX_PCB_1 (6.2.7)
Differential capacitance (calculation from TDR/TDT)	Flat planar	NA	calculated from TDR/TDT
	Unshielded round	NA	calculated from TDR/TDT
	Shielded round	NA	NA
	Printed circuit board	NA	calculated from TDR/TDT
Differential capacitance (frequency measurement)	Flat planar	FIX_Bulk_4 (6.2.6)	NA
	Unshielded round	FIX_Bulk_4 (6.2.6)	NA
	Shielded round	FIX_Bulk_4 (6.2.6)	NA
	Printed circuit board	NA	NA
Differential insertion loss	Flat planar	FIX_Bulk_2 (6.2.4)	FIX_Bulk_2 (6.2.4)
	Unshielded round	FIX_Bulk_2 (6.2.4)	FIX_Bulk_2 (6.2.4)
	Shielded round	FIX_Bulk_2 (6.2.4)	NA
	Printed circuit board	NA	FIX_PCB_1 (6.2.7)
NEXT	Flat planar	FIX_Bulk_3 (6.2.5)	FIX_Bulk_3 (6.2.5)
	Unshielded round	FIX_Bulk_3 (6.2.5)	FIX_Bulk_3 (6.2.5)
	Shielded round	FIX_Bulk_3 (6.2.5)	NA
	Printed circuit board	NA	FIX_PCB_1 (6.2.7)

6.2.3 Test fixture (FIX_Bulk_1)

Refer to figure 3 for the FIX_Bulk_1 test fixture. The test fixture may be constructed of semi-rigid coax, microstrip PCB, or stripline PCB.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

.

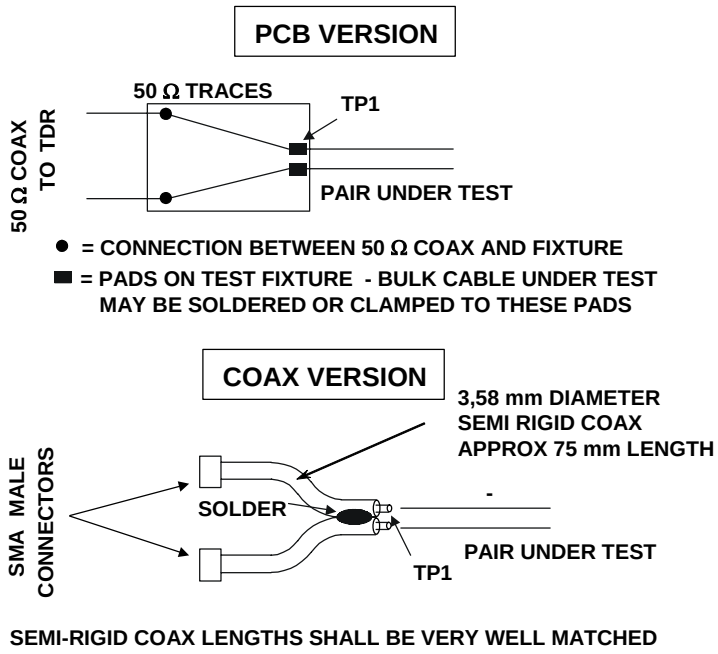


Figure 3 - Test fixture (FIX_Bulk_1)

6.2.4 Test fixture (FIX_Bulk_2)

Refer to figure 4 for the FIX_Bulk_2 test fixture.

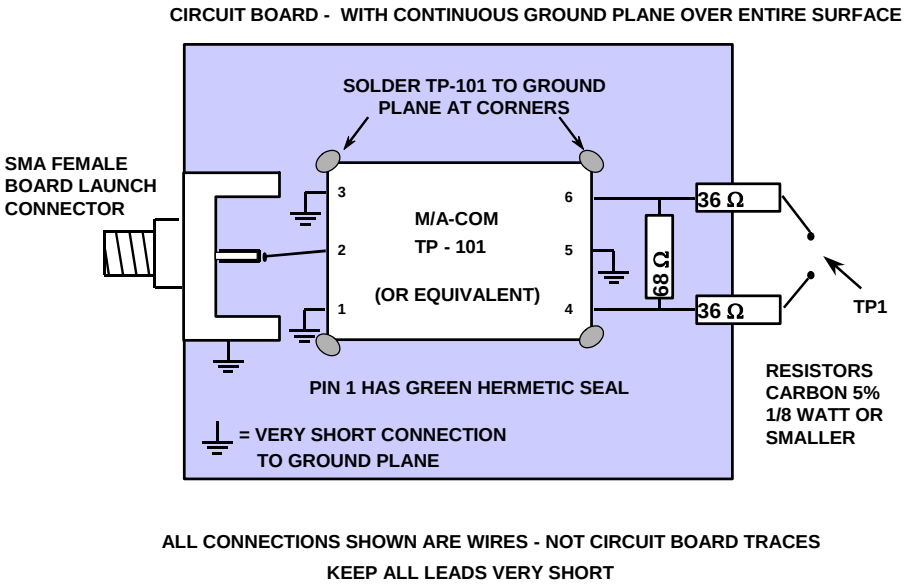
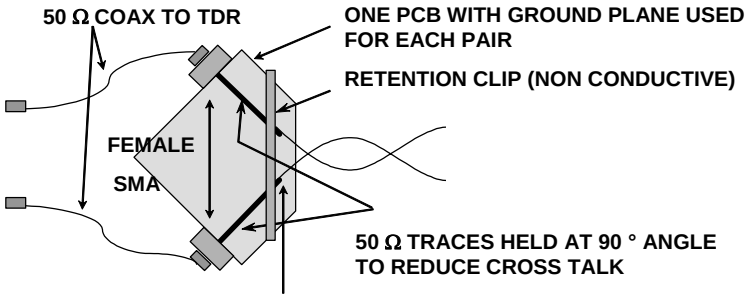


Figure 4 - Test fixture (FIX_Bulk_2)

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS
Not for Resale

6.2.5 Test fixture (FIX_Bulk_3)

Refer to figure 5 for the FIX_Bulk_3 test fixture.



TEST FIXTURE IS CALIBRATED TO REPORT VALUES AT TP1

Figure 5 - Test fixture (FIX_Bulk_3)

6.2.6 Test fixture (FIX_Bulk_4)

Test fixture FIX_Bulk_4 is used for frequency domain capacitance. An Agilent 16047B or equivalent test fixture is required. Refer to Agilent specifications for details.

6.2.7 Printed circuit boards test fixture (FIX_PCB_1)

Test fixtures for PCB's shall meet the same requirements specified in 6.2.3, 6.2.4, 6.2.5 and 6.2.6 with the attachment scheme at TP1 modified to accommodate the electrical access points on the PCB. These modifications shall be done in a manner that minimizes the length of uncontrolled impedances and keeps the differential path balanced (symmetrical equal length). Semi-rigid coax with diameter smaller than 3,58 mm may be desirable.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

6.3 Bulk cable measurement equipment and setups

6.3.1 Summary

Table 7 lists the bulk cable measurement equipment and setups.

Table 7 - Bulk cable measurement equipment and setups

Measurement	Construction	Point-to-point sample type	Multi-drop sample type
Differential. local impedance	Flat planar	SET_Bulk_1 (6.3.2)	SET_Bulk_1 (6.3.2)
	Unshielded round	SET_Bulk_1 (6.3.2)	SET_Bulk_1 (6.3.2)
	Shielded round	SET_Bulk_1 (6.3.2)	NA
Differential propagation time and propagation time skew	Flat planar	SET_Bulk_2 ()	SET_Bulk_2 ()
	Unshielded round	SET_Bulk_2 ()	SET_Bulk_2 ()
	Shielded round	SET_Bulk_2 ()	NA
Differential capacitance (calculation from TDR/TDT)	Flat planar	NA	not required - calculated from TDR/TDT
	Unshielded round	NA	not required - calculated from TDR/TDT
	Shielded round	NA	NA
Differential capacitance (frequency domain measurement)	Flat planar	SET_Bulk_3 (6.3.4)	NA
	Unshielded round	SET_Bulk_3 (6.3.4)	NA
	Shielded round	SET_Bulk_3 (6.3.4)	NA
Insertion loss	Flat planar	SET_Bulk_4 (6.3.5)	SET_Bulk_4 (6.3.5)
	Unshielded round	SET_Bulk_4 (6.3.5)	SET_Bulk_4 (6.3.5)
	Shielded round	SET_Bulk_4 (6.3.5)	NA
NEXT	Flat planar	SET_Bulk_5 (6.3.6)	SET_Bulk_5 (6.3.6)
	Unshielded round	SET_Bulk_5 (6.3.6)	SET_Bulk_5 (6.3.6)
	Shielded round	SET_Bulk_5 (6.3.6)	NA

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS
Not for Resale

6.3.2 Set up (SET_Bulk_1)

Figure 6 shows the equipment setup for SET_Bulk_1.

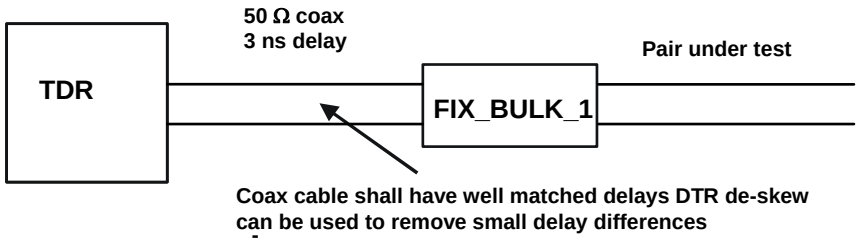


Figure 6 - Equipment setup for SET_Bulk_1

The length of the two coax cables from the TDR to the fixture shall be long enough to contain two complete signal transitions. For the 1 ns STD this minimum length is that required to accommodate approximately 3 ns propagation time, or 6 ns round-trip. For coax having solid fluorocarbon or solid polyolefin dielectrics, the physical length is approximately 0,6 m.

6.3.3 Set up (SET_Bulk_2)

Figure 7 shows the equipment setup for SET_Bulk_2.

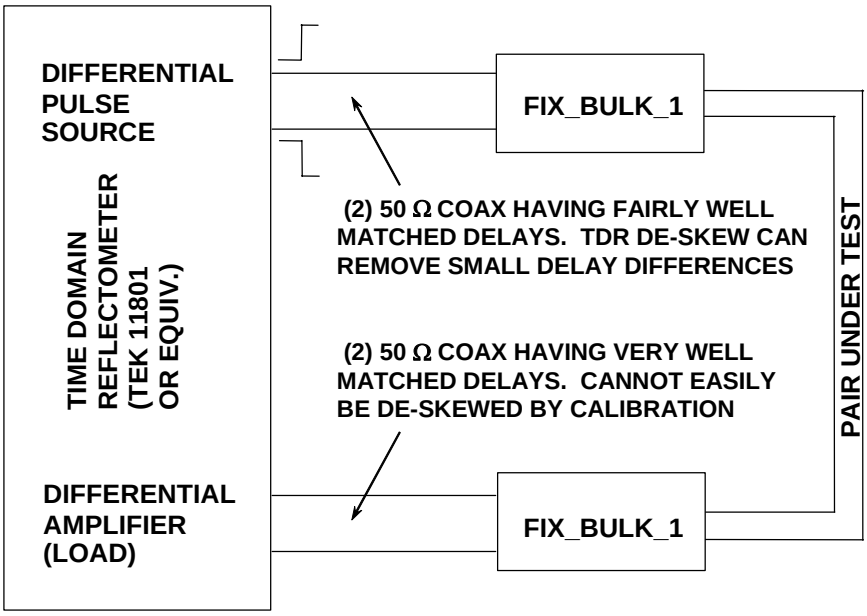


Figure 7 - Equipment setup for SET_Bulk_2

--`,,```,,,,````-`-`,,`,,`,`,,`---
Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS
Not for Resale

6.3.4 Set up (SET_Bulk_3)

Figure 8 shows the equipment setup for SET_Bulk_3.

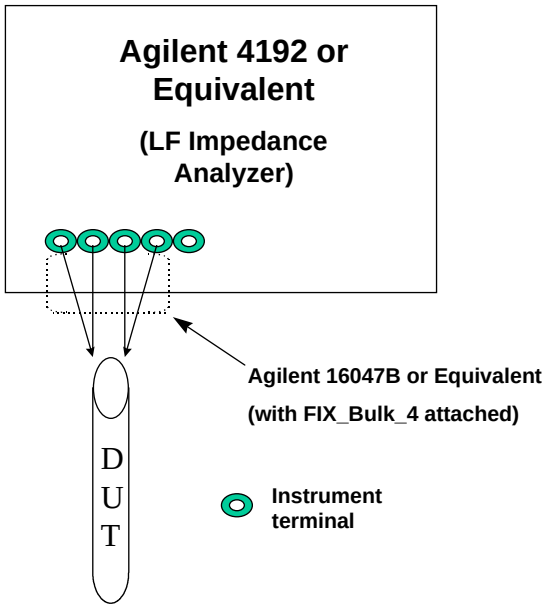


Figure 8 - Equipment setup for SET_Bulk_3

6.3.5 Set up (SET_Bulk_4)

Figure 9 shows the equipment setup for SET_Bulk_4.

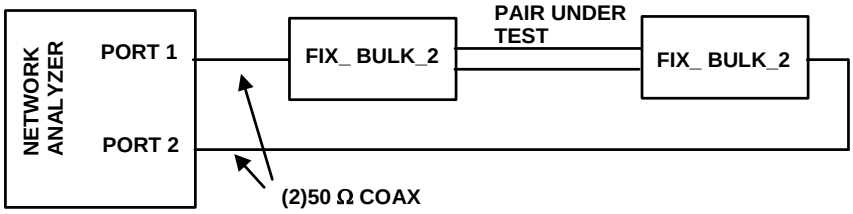


Figure 9 - Equipment setup for SET_Bulk_4

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS
Not for Resale

6.3.6 Set up (SET_Bulk_5)

Figure 10 shows the equipment setup for SET_Bulk_5**.**

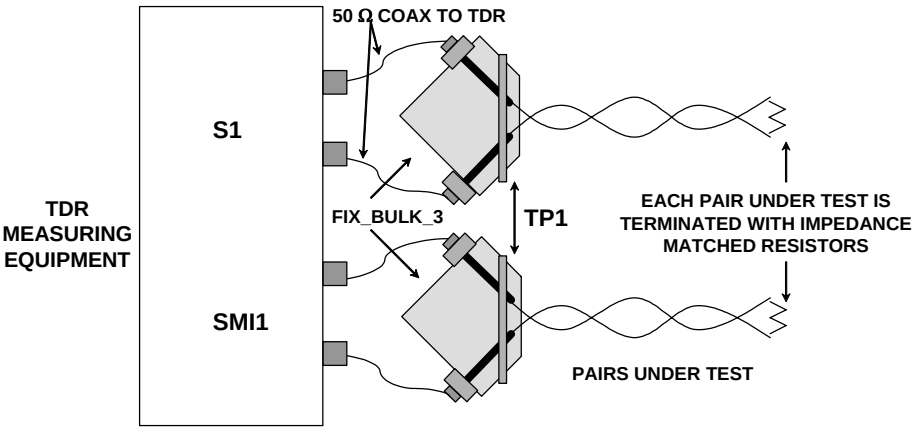


Figure 10 - Equipment setup for SET_Bulk_5

6.4 STD calibration

STD calibration is required for local impedance and NEXT tests. Differential local impedance is measured using 1 ns signal transition duration.

The length of coax(es) from the TDR to the Fixture shall be long enough to contain two complete transitions. For the 1ns STD this minimum length is approximately 3 ns delay, or 6 ns round-trip. For coax having solid fluorocarbon or polyolefin dielectrics, this is about 0,6 m physical length.

This calibration ensures that the proper STD is presented to the DUT. Place a short on the test fixture where the DUT would be attached (“TP1”). Use the filter function on the TDR to set the measured STD (20 % to 80 %) to the required value (+/- 5 %), according to the detailed procedure described below. It may be desirable to use a separate test fixture that is nominally identical to the actual cable test fixture for this step.

Assuming a falling edge, set up the display on the TDR as shown in figure 11**.** This display has the following properties:

1) The time scale on the display is 1,0 ns/div for the 1 ns STD.
2) Set the horizontal position such that the midpoint of the displayed curve is near the center of the display and the 100 % and 0 % baselines are clearly visible as shown in figure 11**.**

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

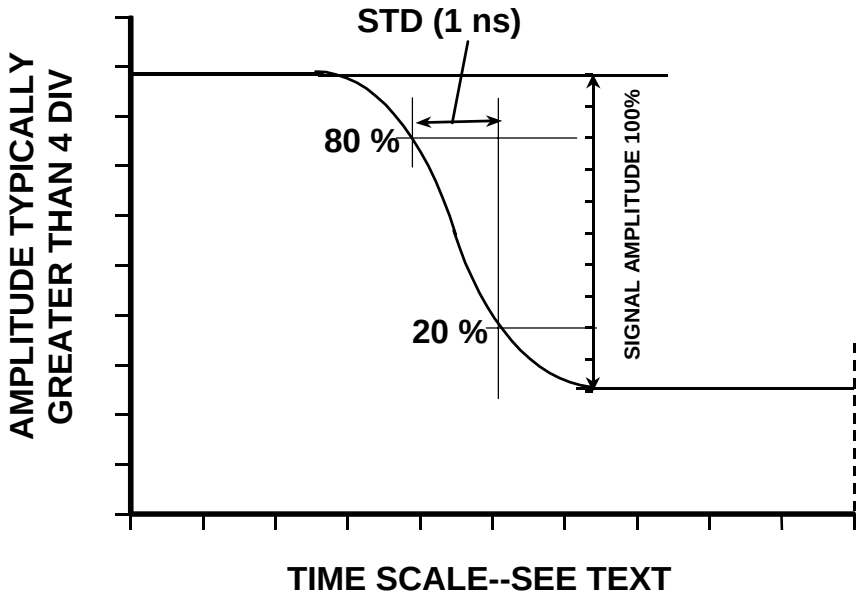


Figure 11 - Signal transition duration calibration

The STD is the time between the 20 % and 80 % values of the displayed signal amplitude (most instruments do this calculation automatically). When the instrument does not automatically measure STD, perform the following steps:

1) Measure the voltage at 100 % (V_{100})
2) Measure the voltage at 0 % (V_0)
3) The voltage at 20 % is {$V_{20} = V_0 + 0{,}2\ (V_{100} – V_0)$}
4) The voltage at 80 % is {$V_{80} = V_0 + 0{,}8\ (V_{100} – V_0)$}
5) Set cursors at V_{20} and V_{80} and measure the time difference

Adjust the TDR filter so that the required STD is achieved.

--`,,```,,,,````-`-`,,`,,`,`,,`---
Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS
Not for Resale

7 Level 1 bulk cable tests

7.1 SE tests

All SE tests shall be performed according to the requirements defined in Annex A. These tests apply to point to point bulk cable only. No SE specifications are provided for multi-drop bulk cable

7.2 Differential local impedance

7.2.1 Overview

Requirements for measuring differential local impedance for all bulk cable constructions are contained in 7.2. Local impedance (TDR) is the impedance over a specified time interval range sufficient to capture all the designed features of the bulk cable.

7.2.2 Point-to-point bulk cable

7.2.2.1 Sample preparation for point to point bulk cable

All point to point constructions shall use sample preparation method SP_Bulk_PP3 defined in 6.1.3.1. Use of samples longer than 3 m is permitted, for example, SP_Bulk_PP10 defined in 6.1.3.2.

7.2.2.2 Test fixtures for point to point bulk cable

All point to point constructions shall use the test fixture FIX_Bulk_1 defined in 6.2.3.

7.2.2.3 Measurement equipment and setup for point to point bulk cable

All point to point constructions shall use the measurement equipment and setup SET_Bulk_1 defined in 6.3.2.

7.2.2.4 Calibration and verification procedure for point to point bulk cable

Twisted pair and flat planar point to point, unshielded round point to point, and shielded round point to point constructions shall use the calibration and verification procedure defined in this sub clause.

It is not necessary to perform a separate instrument verification for this test. The calibration includes the instrument.

1) connect the 50 Ω cables to the test fixture.
2) at “TP1” in the fixture, connect a 100 Ω ± 0,1 % low inductance chip resistor - IMS style TPI-1206 or equivalent.
3) use a differential unfiltered trace and use TDR cursors to measure the resistance value, R100, approximately 4 ns after the resistor discontinuity as depicted in figure 12.
4) in a similar manner, in place of “TP1” connect a 137 Ω ± 0,1 % low inductance chip resistor - IMS style TPI-1206 or equivalent.
5) use a differential unfiltered trace and use the TDR cursors to measure the resistance value, R137, approximately 4 ns (displayed) after the resistor discontinuity.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

Figure 12 is an example of a differential calibration trace.

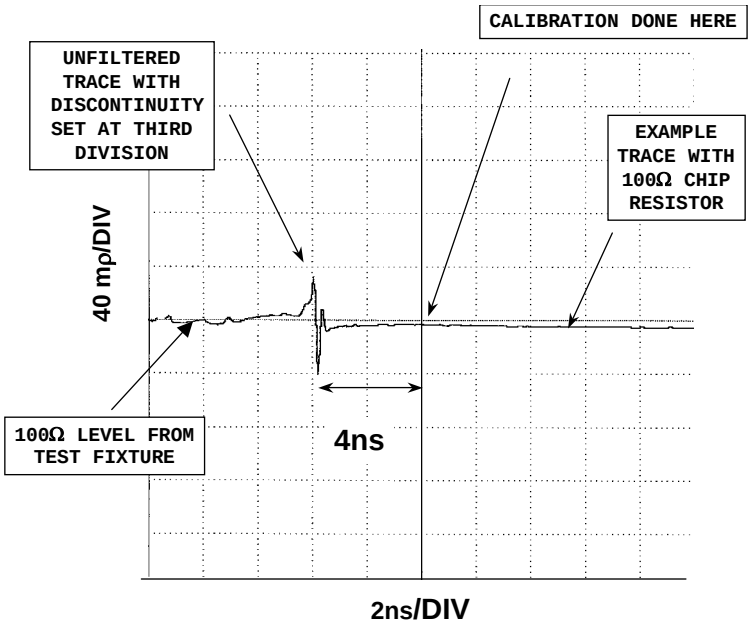


Figure 12 - Differential calibration

For R100 and R137 the equation is:

$$Z_{corrected} = \frac{100(1{,}37 \bullet X1 - X2 - 0{,}37 \bullet Measured)}{X1 - X2}$$

Where:

X1 is the measured value of 100 Ω ± 0,1 %

X2 is the measured value of 137 Ω ± 0,1 %

Optional Correction:

a) Correction is recommended when measurements from samples are close to the specification limits, or where either X1 ≠ (100 ± 2) Ω or X2 ≠ (137 ± 2) Ω.
b) Uncorrected data may be used when X1 = (100 ± 2) Ω and X2 = (137 ± 2) Ω, and the sample measurements are not close to the specification limit.

7.2.2.5 Test procedure and data output format

Twisted pair and flat planar point to point, unshielded round point to point, and shielded round point to point constructions shall use the test procedure defined in this sub clause.

Connect the DUT to the test fixture and record the TDR trace using the method described below. Figure 13 shows the TDR display setup to use for this measurement.

1) set the time scale to 2 ns/div (total time axis span of 20 ns).
2) set the vertical scale (mρ) to 40 mρ/div.
3) with the DUT disconnected turn off any filtering.
4) set the horizontal position such that the discontinuity is on the third division from the left.
5) adjust the vertical position to place the 100 Ω reference (cable and fixture to TDR) approximately at the fifth vertical division from the bottom (centered).
6) set the rise time filter to achieve 1 ns STD (rise time). See 6.4
7) attach the DUT to the fixture.

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

8) set the TDR cursors to measure ohms. Set the cursors on the trace as it crosses the 5th and 6th time divisions as shown in figure 13. Some instruments may not measure Ω between the cursors, but instead measure mρ, which is converted to Ω using the following equation for a 100 Ω system

$$\text{Ohms} = 100\left(\frac{1+\rho}{1-\rho}\right)$$

(1 000 mρ = 1 ρ):

9) set the TDR to measure minimum and maximum ohms between the cursors set in previous step.

These measurements ignore the small error factor caused by losses in the cable which varies with gauge size. This error increases the measured impedance slightly.

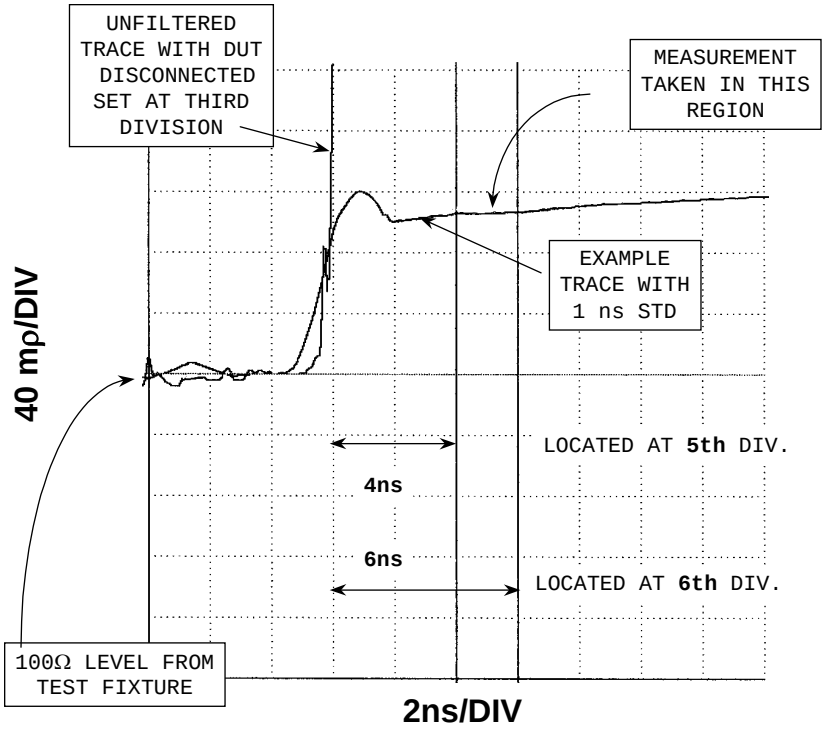


Figure 13 - Cursor placement for bulk cable

7.2.2.6 Acceptable values for point to point bulk cable

Impedance shall be between 110 Ω and 135 Ω inclusive.

7.2.3 Multi-drop bulk cable

7.2.3.1 Sample preparation for multi-drop bulk cable

All multidrop constructions shall use sample preparation method SP_BULK_MD3 defined in 6.1.4.1.

7.2.3.2 Test fixtures for multi-drop bulk cable

All multi-drop constructions shall use the test fixture FIX_Bulk_1 defined in 6.2.3.

7.2.3.3 Measurement equipment and setup for multi-drop bulk cable

All multi-drop constructions shall use the measurement equipment and setup SET_Bulk_1 defined in 6.3.2.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS
Not for Resale

7.2.3.4 Calibration and verification procedure for multi-drop bulk cable

Same as 7.2.2.4.

7.2.3.5 Test procedure and data output format for multi-drop bulk cable

Multi-drop constructions shall use the procedure defined in this sub clause.

Connect the DUT to the test fixture and record the TDR trace using the method described below. Figure 14 shows the TDR display setup to use for this measurement.

1) set the time scale to 2 ns/div (total time axis span of 20 ns).
2) set the vertical scale (mρ) to 40 mρ/div.
3) with the DUT disconnected turn off any filtering.
4) set the horizontal position such that the discontinuity is on the third division from the left.
5) adjust the vertical position to place the 100 Ω reference (cable and fixture to TDR) approximately at the fifth vertical division from the bottom (centered).
6) set the rise time filter to achieve 1 ns STD (rise time). See 6.4
7) attach the DUT to the fixture.
8) set the TDR cursors to measure ohms. Set the cursors on the trace as it crosses the 5th and 8th time divisions as shown in Figure 14. Some instruments may not measure Ω between the cursors, but instead measure mρ, which is converted to Ω using the following equation for a 100 Ω system

$$\text{Ohms} = 100\left(\frac{1+\rho}{1-\rho}\right)$$

(1 000 mρ = 1 ρ):

9) set the TDR to measure minimum, mean and maximum ohms between the cursors set in previous step.

These measurements ignore the small error factor caused by losses in the cable which varies with gauge size. This error increases the measured impedance slightly.

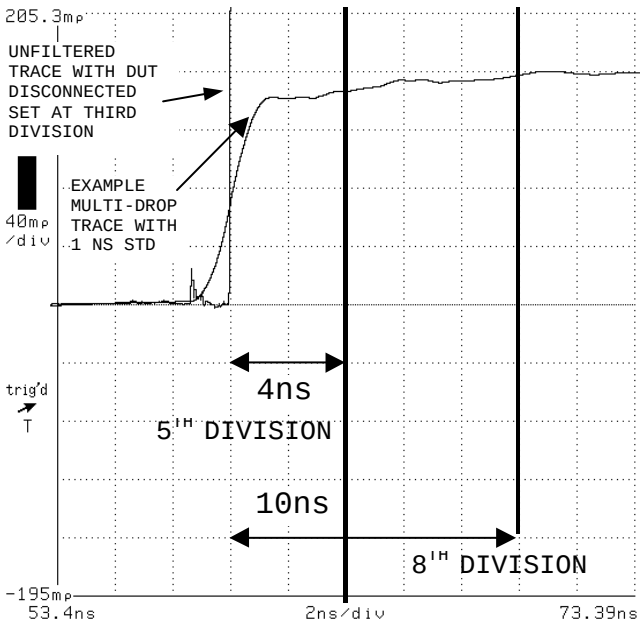


Figure 14 - Cursor placement for constant interval multi-drop cable

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS
Not for Resale

7.2.3.6 Acceptable values for multi-drop bulk cable

Acceptable values for multi-drop bulk cable shall be between 110 and 135 ohms.

7.2.4 Unpopulated printed circuit board (PCB)

Use the same procedures, equipment and acceptable values defined for multidrop bulk cable with appropriate modifications for the PCB structure being used.

7.3 Differential propagation time and propagation time skew

7.3.1 Overview

Requirements for measuring differential propagation time for all bulk cable constructions are contained in 7.3.

7.3.2 Point-to-point bulk cable

7.3.2.1 Sample preparation for point to point bulk cable

All point-to-point constructions shall use sample preparation method SP_Bulk_PP10 described in 6.1.3.2.

7.3.2.2 Test fixtures for point to point bulk cable

All point-to-point constructions shall use two test fixtures FIX_Bulk_1 described in 6.2.3.

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

7.3.2.3 Measurement equipment and setup for point to point bulk cable

All point-to-point constructions shall use the measurement equipment and setup SET_Bulk_2 described in 6.3.3.

7.3.2.4 Calibration and verification procedure for point to point bulk cable

A wide variety of time domain reflectometers exist, having different programming procedures. The following procedure outlines the steps necessary to de-skew the signal source.

1) Set instrument to differential TDR mode. Two traces are displayed, one going positive, the other going negative.
2) With the test fixture attached by coax to the TDR outputs (with no DUT attached), adjust the time-base until the rising edge and the falling edge are approximately as shown in figure 15. (200 ps/div recommended).
3) Define a trace that is Positive_pulse + Negative_pulse. Because the two pulses are equal amplitude but opposite polarity, the resultant display is flat, except for the region where the edges are skewed. See Figure 15.

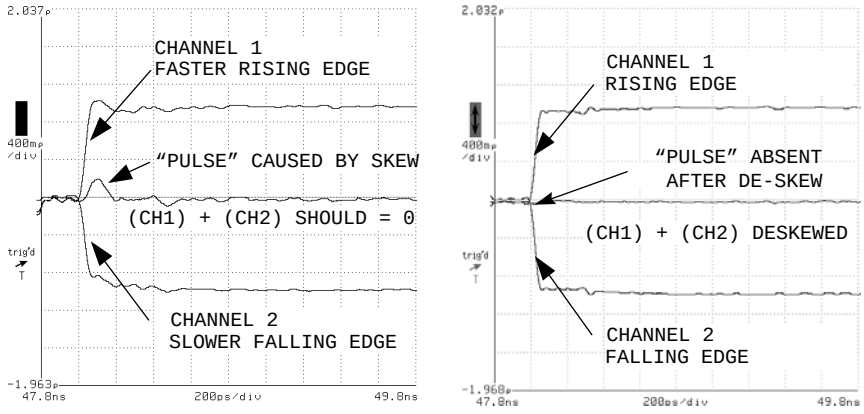


Figure 15 - TDR launch de-skew

4) Adjust the delay between Positive_pulse and Negative_pulse so that the calculated trace is as flat as possible in the rise-time / fall-time region.
5) Use solder, clamps, or extremely short cable to attach the two fixtures together so that pulse goes directly from the source fixture to the load fixture. The coaxes going from Setup 6 lower fixture to the measurement instrument shall be extremely well matched for delay.
6) Define two traces for the load inputs of the system: Channel 3 and Channel 4. Measure the propagation delay (at 50 %) between Channels 3 and 4. This should be less than 10 ps. This is the built-in measurement system skew. If measured skew is much above 10 ps, then the lower fixture has built-in delay mismatch, or the lower coaxes are mismatched.

Do not disturb fixtures from step 6. The calibration and verification procedure is complete.

7.3.2.5 Test procedure and data output format for point to point bulk cable

1) Adjust the display to look approximately as shown at the left in figure 16. Recommend 5 ns/div and high resolution horizontal acquisition. The two waveforms are the test system responses of Channels 3 and 4, with a "zero-length" sample.
2) Remove the connection between the two fixtures.
3) Attach the sample to each fixture. The display should look approximately like the right in figure 16. It may be necessary to slightly reposition Channels 3 and 4 vertically.

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

4) Use the instrument's built-in software to measure the delay between each set of displays at the 50 % points. Record the results.
   Delay 3: Channel 3 "Zero Length" to Channel 3 with sample
   Delay 4: Channel 4 "Zero Length" to Channel 4 with sample

   Calculate the following for each pair:

$$Time_{Propagation} = \frac{Delay3 + Delay4}{2}$$

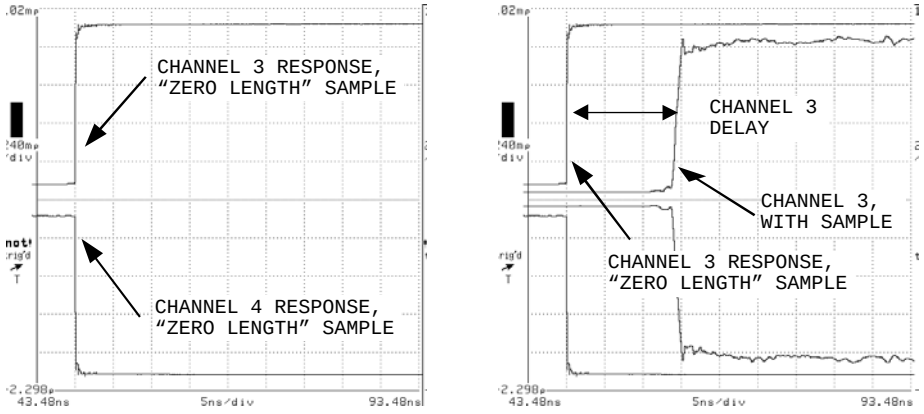


Figure 16 - Propagation time measurement

Propagation time measurement may also be performed using differential traces.

7.3.2.6 Acceptable values for point to point bulk cable

Propagation time shall be between 0 ns and 135 ns for a 25 m sample. The absolute value of the propagation time skew shall be between (0 and 2,0) s for a 25 m sample.

7.3.3 Multi-drop bulk cable

7.3.3.1 Sample preparation for multi-drop bulk cable

All multi-drop constructions shall use sample preparation method SP_Bulk_MD3 described in 6.1.4.1.

7.3.3.2 Test fixtures for multi-drop bulk cable

All multi-drop constructions shall use two test fixtures FIX_Bulk_1 described in 6.2.3.

7.3.3.3 Measurement equipment and setup for multi-drop bulk cable

All multi-drop constructions shall use the measurement equipment and setup SET_Bulk_2 described in 6.3.3.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS
Not for Resale

7.3.3.4 Calibration and verification procedure for multi-drop bulk cable

Same as 7.3.2.4.

7.3.3.5 Test procedure and data output format for multi-drop bulk cable

Same as 7.3.2.5.

7.3.3.6 Acceptable values for multi-drop bulk cable

The acceptable values apply to the results measured on the 3 m sample defined in 7.2.3.1. The maximum propagation time for any signal pair is 16,2 ns. The maximum absolute value of pair to pair propagation time skew between any two signal pairs is 0,35 ns. For sample lengths that are within 20 % of 3 m the allowed values are scaled with length.

7.3.4 Unpopulated PCB

All unpopulated PCB's shall use the same methods and performance requirements described for multidrop bulk cable with appropriate modifications for the test fixtures to accommodate the PCB electrical access points.

7.4 Differential capacitance by calculation

7.4.1 Overview

Differential capacitance is specified either by using a calculation methodology based on the differential local impedance and differential propagation time or by using a direct measurement in the frequency domain. The material in the remainder of this clause describes the requirements for the calculation methodology.

7.4.2 Differential capacitance by calculation for all constructions of bulk cable

For all constructions of bulk cable the differential capacitance is calculated by the following method:

Use the local differential impedance measured in 7.2, Z_0, and the differential propagation time measured in 7.3.

Calculate the propagation time in seconds per meter, T_p.

Use the following equation to calculate capacitance in Farads per meter.

$$C(\text{Farad / meter}) = \frac{T_p(\text{seconds / meter})}{Z_0}$$

7.4.3 Acceptable differential capacitance values for all constructions of bulk cable

Acceptable values are (26 to 46) pF/m.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

7.5 Differential capacitance by frequency domain measurement

7.5.1 Point-to-point bulk cable

7.5.1.1 Sample preparation for point to point bulk cable

Point to point bulk cables uses sample preparation SP_Bulk_PP3 described in 6.1.3.1.

7.5.1.2 Test fixtures for point to point bulk cable

The text fixture (Agilent 16047B or equivalent) is imbedded in the measurement equipment described in 7.5.1.3.

7.5.1.3 Measurement equipment and setup for point to point bulk cable

An Agilent 4192x or equivalent impedance analyzer is used in SET_Bulk_3 described in 6.3.4.

7.5.1.4 Calibration and verification procedure for point to point bulk cable

Connect test fixture Agilent 16047 to test equipment (Agilent 4192A), leave measurement terminals open.

1) Set ‘Display’ A to C using the arrows
2) Set ‘Circuit Mode’ to ‘Parallel’
3) Set ‘Spot freq’ to desired measurement frequency (for example: 2 MHz)
4) Set ‘ZY Range’ to ‘Auto’
5) Select ‘Open’

7.5.1.5 Test procedure and data output format for point to point bulk cable

Designate one conductor of the pair as conductor 1, the other as conductor 2, and the shield as conductor 3. All other conductors are left floating on both ends.

1) Connect conductor 1 to the low terminal of the test fixture. Connect 2 and 3 to the high terminal
2) Record capacitance from display A as measurement Ca
3) Connect conductor 2 to the low terminal of the test fixture. Connect conductors 1 and 3 to the high terminal
4) Record capacitance from display A as measurement Cb
5) Connect conductors 1 and 2 to the low terminal of the test fixture. Connect conductor 3 to the high terminal
6) Record capacitance from display A as measurement Cc
7) Calculate the differential capacitance as follows:
   $C=\{2\ (Ca+Cb)-Cc\}/\{4*L\}$ where L = cable length

7.5.2 Multi-drop bulk cable

Multidrop bulk cable shall use the time domain calculation method described in 7.4.2.

7.5.3 Unpopulated PCB

Unpopulated PCB’s shall use the time domain calculation method described in 7.4.2.

7.5.4 Acceptable differential capacitance values for all constructions of bulk cable

Acceptable values are (26 to 46) pF/m at 100 kHz and 1 MHz.

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

7.6 Differential insertion loss

7.6.1 Overview

Differential insertion loss, S21, is a measurement of the loss of sinusoidal signal amplitude across a specified spectrum that is caused by the DUT. Insertion loss is the difference between the test setup losses with no DUT and the losses in the test setup with the DUT present.

Level 1 differential insertion loss requirements apply only to point to point bulk cable constructions. There are no level 1 requirements for insertion loss on multi-drop bulk cable. Material in 7.6 relating to multi-drop insertion loss is level 2. Details for insertion loss measurements on multi-drop structures (bulk cable and unpopulated PCB's), recommended sample preparation, test setup, fixture, calibration and measurement procedure are provided for reference in this sub clause.

Methods that do not require the use of baluns may be acceptable if equivalence exists to the balun based methods described in this document.

7.6.2 Point-to-point bulk cable

7.6.2.1 Sample preparation for point to point bulk cable

Point to point bulk cables uses sample preparation SP_Bulk_PP25 described in 6.1.3.3.

7.6.2.2 Test fixtures for point to point bulk cable

Point to point bulk cable uses two test fixtures FIX_Bulk_2 described in 6.2.4.

7.6.2.3 Measurement equipment and setup for point to point bulk cable

Point to point bulk cables uses setup SET_Bulk_4 described in 6.3.5.

7.6.2.4 Calibration, verification and measurement procedure for point to point bulk cable

Calibration is achieved by measuring the system and fixture response, with two fixtures connected as shown in figure 17. This measured system response shall be saved and later removed from the data taken after the sample is inserted.

There are many different models of network analyzers whose instrument settings are varied. However, the basic steps are the same from model to model. These steps are listed below.

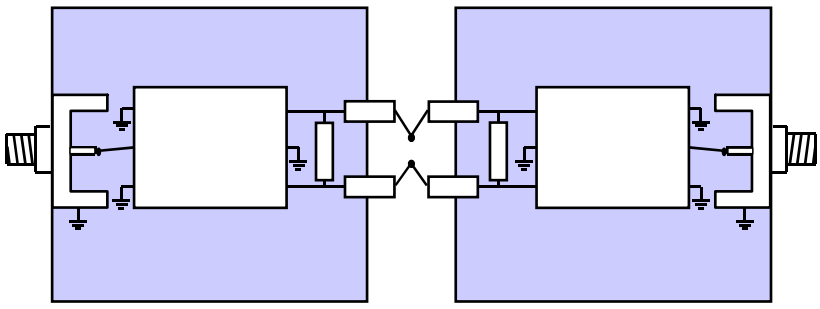


Figure 17 - Calibration configuration

1) Set start frequency to 10 MHz.

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

2) Set stop frequency to 650 MHz or higher.
3) Set horizontal frequency scale to linear where possible.
4) Set number of points to > 400 where possible.
5) Set IF bandwidth <= 100 Hz.
6) Set to measure S21 (insertion loss), Log magnitude.
7) Recommended initial vertical settings: 0 dB at top of screen, 10 dB per division.
8) Connect to test fixtures as shown in figure 17.
9) Record the system response with just test fixtures. This response is usually stored in the network analyzer (by placing into “memory”). If the network analyzer cannot store the system response, the response is recorded to a computer for subsequent processing.
10) Detach the two fixtures.
11) Reposition the two fixtures to be at least 50 mm apart during the measurement. This minimizes fixture-to-fixture cross talk.
12) Attach the sample between the two fixtures.
13) Record S21.
14) (a) For network analyzers that are able to store the fixture response in memory, set the display to show {S21 divided by memory}, (b) For network analyzers that cannot store the fixture response in memory, subtract the retrieved stored fixture data from the retrieved sample data. (Subtracting dB is the same as dividing linear. The network analyzer performs the division and then converts to dB.)
15) Record the result as dB versus linear (where possible) frequency.

7.6.2.5 Acceptable values for point to point bulk cable

S21 shall be between (0 and -12) dB at 200 MHz for the 25 m sample used for the measurement.

7.6.3 Multi-drop bulk cable

7.6.3.1 Overview

Bulk cable measured without terminations or loads produces results that are of questionable value. Therefore, insertion loss measurements on multi-drop cables are level 2.

Multi-drop cables contain periodic structures that cause strong resonances at frequencies determined by the intervals between the twist sections and the flat sections. Harmonic and sub-harmonic resonances exists.

The insertion loss of short samples does not scale with insertion loss of long samples. For example, a typical multi-drop cable sub-assembly might have a total of four flats on 0,25m center spacing. From end to end this sample has three (3) repetitive structures, and exhibits slight resonances at the appropriate frequencies.

A 25m sample of the same cable has 99 repetitive structures and exhibits very strong resonances that are very misleading relative to the performance of the shorter sample.

7.6.3.2 Sample preparation for multi-drop bulk cable

Multi-drop bulk cable sample preparation SP_Bulk_MD3 is described in 6.1.4.1., except that the recommended sample length is the maximum required in the specific application instead of 3 m as specified for SP_Bulk_MD3.

Measurement results from short samples have unavoidable fixture effects and mismatch effects that are normally hidden in long samples.

7.6.3.3 Test fixtures for multi-drop bulk cable

Multi-drop bulk cables use test fixture FIX_Bulk_2 described in 6.2.4.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

7.6.3.4 Measurement equipment and setup for multi-drop bulk cable

Multi-drop bulk cables use setup SET_Bulk_4 described in 6.3.5.

7.6.3.5 Calibration, verification and measurement procedure for multi-drop bulk cable

Refer to 7.6.2.4 above.

7.6.3.6 Acceptable values for multi-drop bulk cable

Since this is a level 2 measurement no acceptable values are specified.

7.6.4 Unpopulated PCB

Insertion loss for unpopulated PCB is treated in the same way as multidrop bulk cable. This is a level 2 measurement.

7.7 Near end cross talk (NEXT)

7.7.1 Overview

NEXT is a measure of the signal caused by the driven pair that is coupled into undriven pairs at the end nearest the driver on the driven pair.

Level 1 requirements apply only to the REQ and ACK signals for point to point constructions. Other signals may be measured as level 2 using the methods defined herein.

There are no level 1 requirements for multi-drop NEXT. Material in 7.7 relating to multi-drop NEXT is level 2. However, details for NEXT measurements on multi-drop structures (bulk cable and unpopulated PCB's), recommended sample preparation, test setup, fixture, calibration and measurement procedure are provided for reference in this sub clause. This measurement was selected for inclusion in this standard because this measurement is frequently done in practice and commonality of execution is in the best interest of the industry.

This test is limited to the single applied pulse method. The pair with the applied pulse is the aggressor pair and the pair with the induced noise is the victim pair. In this method pulses with known differential amplitude, 1 ns STD signal are applied to one pair at a time in the DUT, and the signal induced on the victim pair is measured.

The sum of the noise produced by all high speed signal pairs (DATA, PARITY, REQ and/or ACK) on the single victim pair is the crosstalk. If the victim pair is one of the high speed pairs there are 19 aggressor pairs. If the victim pair is not one of the high speed pairs there are 20 aggressor pairs. (If the REQ is the victim pair then the ACK pair is included as an aggressor pair. If ACK is the victim pair then the REQ pair is included as an aggressor pair.)

All 26 signals listed in table 2 as applicable to PIP are victim pairs.

Single pulse tests (which eliminate the effects of resonance) are deterministic in the causes of the induced noise (due to the mapping of the time and space as in the TDR tests), and produce the worst case results.

The aggressor pulses are of the same type used for the impedance test: start with single ended signals: + signal typically at 250 mV and the - signal typically at 250 mV of opposite polarity. The differential incident pulse is therefore typically 500 mV [250 mV - (-250 mV)].

The use of actual worst case data patterns on the aggressor lines has been extensively debated and considered. This is the natural excitation that was initially considered. Extensive testing has shown that resonance conditions and effects of test fixtures may severely distort the measured results when using real data patterns. Sometimes these effects improve the crosstalk performance and other times they exacerbate it. It is very difficult to diagnose the intensity and cause of resonance and fixture effects when using a real data pattern. The single pulse eliminates these effects and gives a worst case result that may be attributed to as much of the system as required. For example, if connector termination techniques are causing the crosstalk then that may be revealed by examining the time points associated with the termination points.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

The value of the recorded disturbance in the victim line from a single aggressor is the differential peak value of the induced noise at a time position within the DUT excluding the test fixture region. The effect of multiple aggressors is treated differently for point to point versus multi-drop constructions.

The peak measurement (not peak to peak) is the important parameter because receivers measure the differential signal relative to a differential zero position. Even if the intensity of the crosstalk signal is greater with a peak to peak measurement the receiver is only affected by that portion that deviates from the zero differential level (i.e., the peak level).

Since crosstalk is a linear function of amplitude, it is not required that the actual aggressor signal be the maximum differential amplitude. A scaling technique is used to compensate for equipment that is not capable of launching 500 mV amplitude signals.

Each of the DATA, PARITY, REQ and ACK pairs is treated as an aggressor for bulk cable. No other signals are treated as aggressors for this measurement. Each of the DATA, PARITY, REQ or ACK pairs shall be separately excited unless the pair is the pair under test (the victim pair).

Each of the DATA, PARITY, REQ or ACK pairs shall be treated as a victim line. There are 19 aggressors in this case.

For C/D, I/O, MSG, ATN, BSY, SEL, as victims all 20 high speed signals act as aggressors (DATA, PARITY, REQ, and ACK pairs).

The induced absolute peak noise (deviation from zero differential) on the victim pair measured at a time position not associated with the test fixture shall be recorded as the crosstalk contribution from that aggressor signal. The results from each aggressor signal are added to yield the total crosstalk. The method of addition is diffferent for point to point versus multidrop.

7.7.2 Point-to-point bulk cable

7.7.2.1 Sample preparation for point to point bulk cable

Point-to-point bulk cable uses sample preparation SP_Bulk_PP10 in 6.1.3.2.

7.7.2.2 Test fixtures for point to point bulk cable

Point-to-point bulk cable uses two test fixtures FIX_Bulk_3 in 6.2.5. An acceptable alternate is Fix_Bulk_1 in 6.2.3.

7.7.2.3 Measurement equipment and setup for point to point bulk cable

Point-to-point bulk cable setup uses SET_Bulk_5 in 6.3.6. The length and properties of the 50 Ω coaxes connecting the aggressor signal and the victim measurement instrument to the test fixture should be the same length. Absorbtive (not reflecting) hardware filters are preferred to produce the rise time required although software filtering is allowed.

If using hardware filters, place one filter in each S1 channel on the instrument side, see 6.3.6 for location of S1.

7.7.2.4 Calibration and verification procedure for point to point bulk cable

The STD calibration is done using the same method as for the TDR tests in 6.4. If using hardware filters the filters shall be selected to deliver the required STD during the measurement. This may require specifying hardware filters that allow for some loss of high frequency content in the test setup. The same STD is used for both aggressor and victim displays.

Reference times are determined as shown in figure 18.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

.

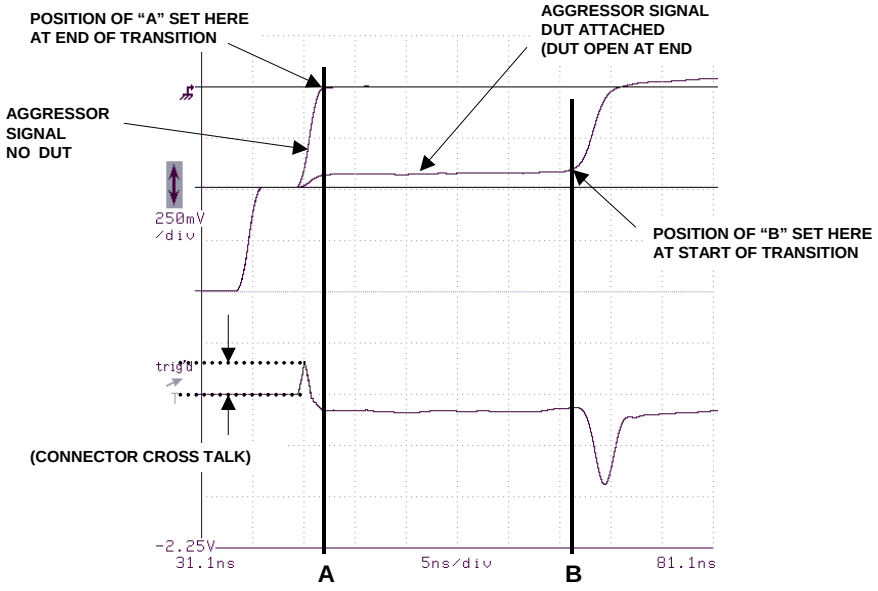


Figure 18 - Near end cross talk measurement region

Vertical line "A" is defined by using only a test fixture with an open circuit load (no DUT attached). Vertical line "A" represents the end of the test fixture and the beginning of the bulk cable.

Crosstalk in the region to the left of vertical line "A" is dominated by fixture cross talk (or in an interconnect assembly by connector and connector attachment crosstalk).

Vertical line "B" is defined by connecting a DUT to the test fixture with an open circuit on the end of the DUT. Vertical line "B" represents the end of the DUT.

Crosstalk in the region to the right of vertical line "B" is dominated by multiple reflections bouncing between the open circuit impedance and the fixture impedance.

Crosstalk in the region between vertical lines "A" and "B" is dominated by the bulk cable.

Recommended details: Aggressor signal scale, 250 mV/div. Victim signal scale, 50 mV/div. Use averaging for capturing cross talk waveform on victim pair.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS
Not for Resale

7.7.2.5 Test procedure and data output format for point to point bulk cable

Using the conditions specified in 7.7.2.4 and referring to figure 18:.

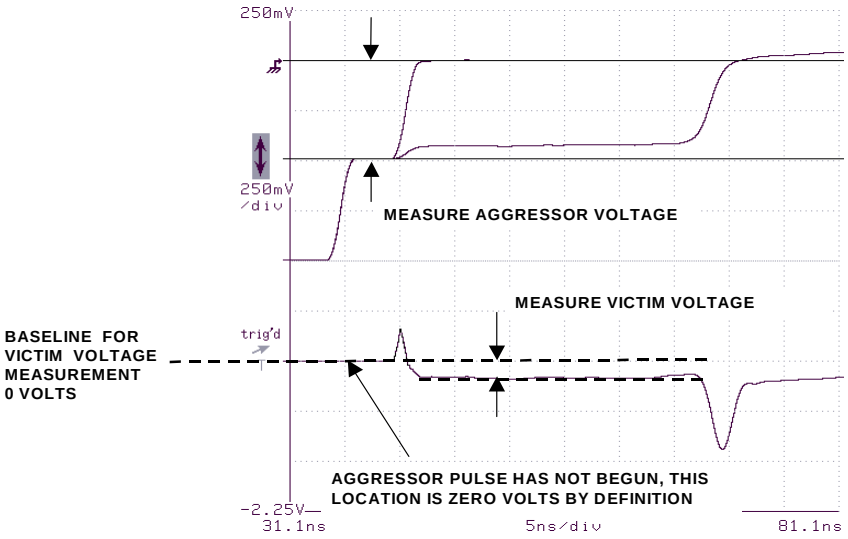


Figure 19 - Measure aggressor voltage and victim voltage

1) Measure the aggressor voltage, using cursors, as shown in figure 19.
2) Record ("store") separately the waveform on the victim line in the time interval between "A" and "B" for each of the 19 or 20 aggressor signals (see 7.7.1).
3) Measure the victim voltage, using cursors, as shown above in figure 19. The victim voltage is the mathematical difference between the "baseline" voltage and the absolute value of the peak crosstalk within the region specified by figure 18.
4) The crosstalk voltage for the victim pair is the sum of all the absolute voltages recorded in the previous step for all aggressors.

Crosstalk percent is calculated as follows:

%NEXT = [(crosstalk voltage) / (peak to peak differential aggressor voltage)] x 100 %

7.7.2.6 Acceptable values for point to point bulk cable

The maximum level of NEXT is 3 % for either the REQ or ACK signals as the victim line.

7.7.3 Multi-drop bulk cable

Multi-drop cables contain deliberate discontinuities that increase cross-talk compared to point-to-point bulk cable.

Bulk cable measured without terminations or loads produces results that are of questionable value. Therefore, NEXT measurements on multi-drop cables are level 2.

7.7.3.1 Sample preparation for multi-drop bulk cable

Multi-drop bulk cable sample preparation SP_Bulk_MD3 is described in 6.1.4.1., except that the recommended sample length is the maximum required in the specific application instead of 3 m as specified for SP_Bulk_MD3.

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

All pairs shall be open at the far end of the sample under test and all pairs except the aggressor and victim shall be open at the near end.

7.7.3.2 Test fixtures for multi-drop bulk cable

Multi-drop bulk cable uses test fixture Fix_Bulk_1 in 6.2.3. An acceptable alternate is FIX_Bulk_3 in 6.2.5.

7.7.3.3 Measurement equipment and setup for multi-drop bulk cable

Multi-drop bulk cable setup uses SET_Bulk_5 in 6.3.6.

7.7.3.4 Calibration and verification procedure for multi-drop bulk cable

See 7.7.2.4.

7.7.3.5 Test procedure and data output format for multi-drop bulk cable

Using the conditions specified in 7.7.2.4 and referring to figure 18:

a) Measure the aggressor voltage, using cursors, as shown below in figure 20.

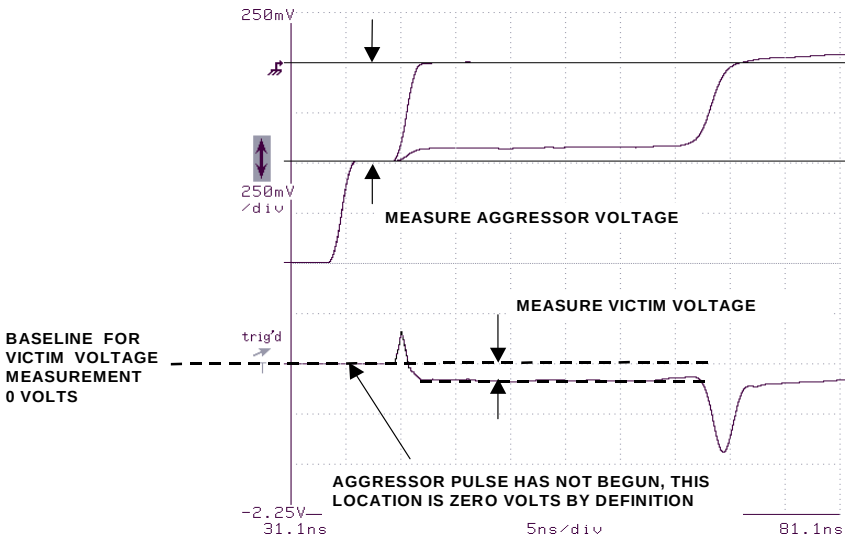


Figure 20 - Measure aggressor voltage and victim voltage

b) Record ("store") separately the waveform on the victim line in the time interval between "A" and "B" for each of the 19 or 20 aggressor signals (see 4.16). Most modern oscilloscopes permit storage of waveforms for later use.
c) Using the oscilloscope math functions, define a new trace, "SUM", that is the sum of all 19 or 20 stored victim waveforms.
d) Measure the victim voltage, using cursors, as shown above in figure 20. The voltage is the mathematical difference between the "baseline" voltage and the peak cross talk within the region specified by figure 18. (The baseline voltage will not measure zero. Measurement instruments have "offset", they indicate some small voltage when the input is actually zero volts. The example described below adds 19 separate cross talk measurements, which multiplies the small offset voltage by 19).
e) The reported cross talk for the victim pair is the peak of the SUM waveform.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS
Not for Resale

Crosstalk percent is calculated as follows:

%NEXT = [SUM / (peak to peak differential aggressor voltage)] x 100 %

It may be necessary to use fewer than 19 or 20 waveforms at a time. For example, using a Tektronix 11801 with 19 aggressors, the following process may be used:

Stored trace A = sto1 + sto2 + sto3 + sto4 + sto5 + sto6 + sto7.

Stored trace B = sto8 + sto9 + sto10 + sto11 + sto12 + sto13 + sto14.

Stored trace C = sto15 + sto16 + sto17 + sto18 + sto19 .

SUM (sum of all victim waveforms) = A + B + C.

This scheme is simple addition where the number of constituents in each intermediate waveform is irrelevant.

The letters A, B, and C are numbers assigned by the operator.

7.7.3.6 Acceptable values for multi-drop bulk cable

Since this is a level 2 measurement no acceptable values are specified.

7.7.4 Unpopulated PCB

NEXT for unpopulated PCB's is treated in the same way as multidrop bulk cable. This is a level 2 measurement.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

8 Summary - interconnect assemblies

Table 8 - Interconnect assembly level 1 test summary

Test parameter	Level	Domain	Condition	Comments
Differential local impedance	1	T	STD=1 ns	TDR - TEK 11801or equivalent, no standard loads used
Propagation time	1	T	at signal transition midpoint	TDT - TEK 11801or equivalent, standard loads required
Propagation time skew	1	T	T_{pmax}-T_{pmin} for all pairs	Pair to pair
Differential signal integrity diagrams (eye and TDW) (differential signal degradation within the pair)	1	T	Specified data pattern activity on neighboring lines provided by a SSDB	Requires meeting differential insertion loss requirements
Differential to common mode conversion	1	T	Specified data pattern activity on neighboring lines provided by a SSDB	+signal to - signal common mode within the pair (sum of the + and - signals)

Table 9 - Interconnect assembly level 2 measurement summary

Test parameter	Level	Domain	Condition	Comments
Differential insertion loss	2 (diagnostic for suckouts)	F	S21 - sweep from 10 MHz through 650 MHz[1]	All signal pairs Network analyzer - Agilent 8753x or equivalent
1 - S21 is a scattering parameters that relates the incident and transmitted voltage waves in a two-port circuit.				

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

9 Interconnect assemblies samples, test fixtures, and setups

9.1 Interconnect assembly samples and sample preparation

Interconnect assemblies have connectors attached (by definition of interconnect assemblies). These connectors provide the means for attaching the DUT to test fixtures. No other requirements are specified for sample preparation for interconnect assemblies.

9.2 Test fixtures for interconnect assemblies

9.2.1 Overview

Test fixtures are the hardware that enables connection of the sample under measurement to the instrumentation.

Test fixtures are required for every measurement specified in this document.

9.2.2 Summary

Table 10 lists the test fixtures for interconnect assemblies.

Table 10 - Test fixtures for interconnect assemblies

Measurement	Construction	Point-to-point sample type	Multi-drop sample type
Differential local impedance, propagation time, and propagation time skew	Unshielded and shielded	FIX_ASY_1, (9.2.3)	FIX_ASY_1, (9.2.3)
Differential signal integrity diagrams (eye and TDW) and differential to common mode conversion	Unshielded and shielded	FIX_ASY_2, (9.2.4) and FIX_ASY_3, (9.2.5)	FIX_ASY_2, (9.2.4) FIX_ASY_3, (9.2.5), and an unterminated standard load, (4.9.3.1)
Differential insertion loss	Unshielded and shielded	FIX_ASY_4, (9.2.6)	FIX_ASY_4, (9.2.6) and an unterminated standard load, (4.9.3.1)

--`,,```,,,,````-`-`,,`,,`,`,,`---
Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS
Not for Resale

9.2.3 Test fixture (FIX_ASY_1)

Refer to figure 21 for FIX_ASY_1. The test fixture may be constructed of microstrip PCB or stripline PCB.

.

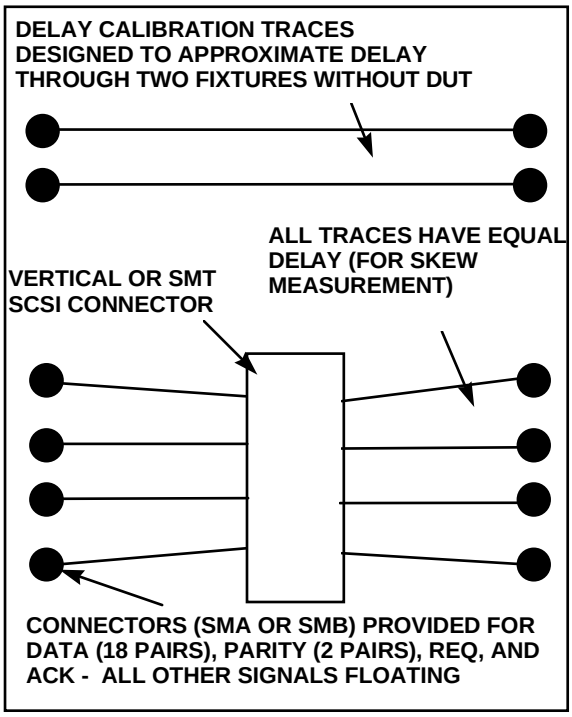


Figure 21 - Test fixture (FIX_ASY_1)

The shields for the connectors on the test fixture shall be connected directly to the PCB ground plane. All unused connector pins shall be left unterminated (floating).

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS
Not for Resale

9.2.4 Test fixture (FIX_ASY_2)

Figure 22 shows Test fixture (FIX_ASY_2).

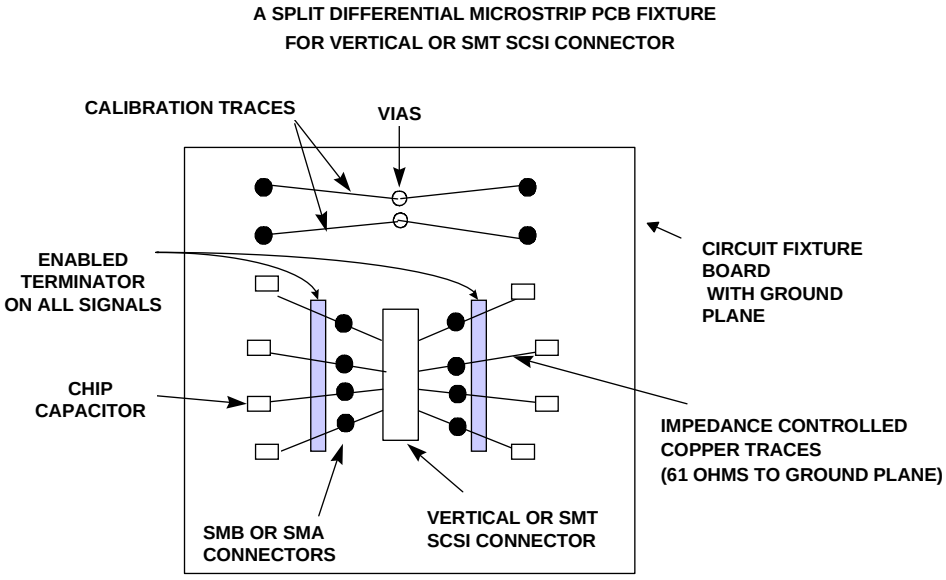


Figure 22 - Test fixture (FIX_ASY_2)

The shield for the connector on the test fixture shall be connected directly to the PCB ground plane. All connector ground pins shall be tied to the PCB ground plane. All connector pins unused by the SSDB shall be terminated to the ground plane using resistors of (62± 5 %) Ω (62 ohm 1 % chip resistors are readily available and recommended) and located as close as possible to the connector vias.

An enabled SCSI terminator shall be connected to all signals. The terminator is enabled and termpwr is required to be present at the terminator for the enabled terminator to be operational.

This test fixture also shall serve as a standard load with an enabled terminator and shall additionally meet the requirements in 4.9.3.2. It may be possible to modify this design to build a standard load without enabled terminators as defined in 4.9.3.1.

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

9.2.5 Test fixture (FIX_ASY_3)

Figure 23 shows the SCSI signal driver board (FIX_ASY_3).

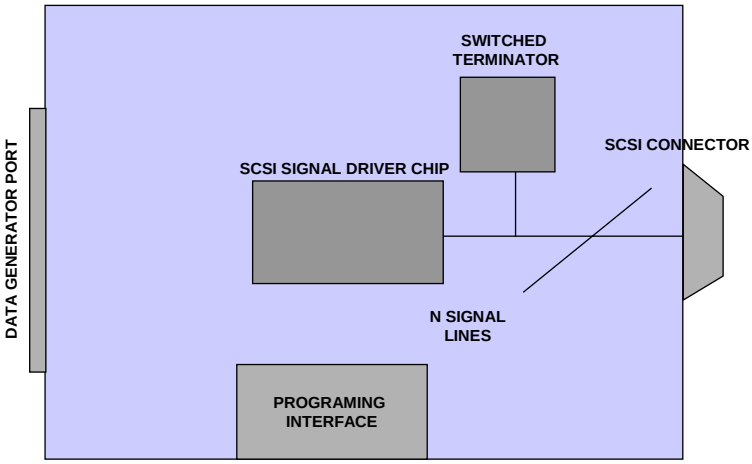


Figure 23 - SCSI signal driver board (FIX_ASY_3)

9.2.6 Test fixture (FIX_ASY_4)

Figure 24 shows test fixture (FIX_ASY_4).

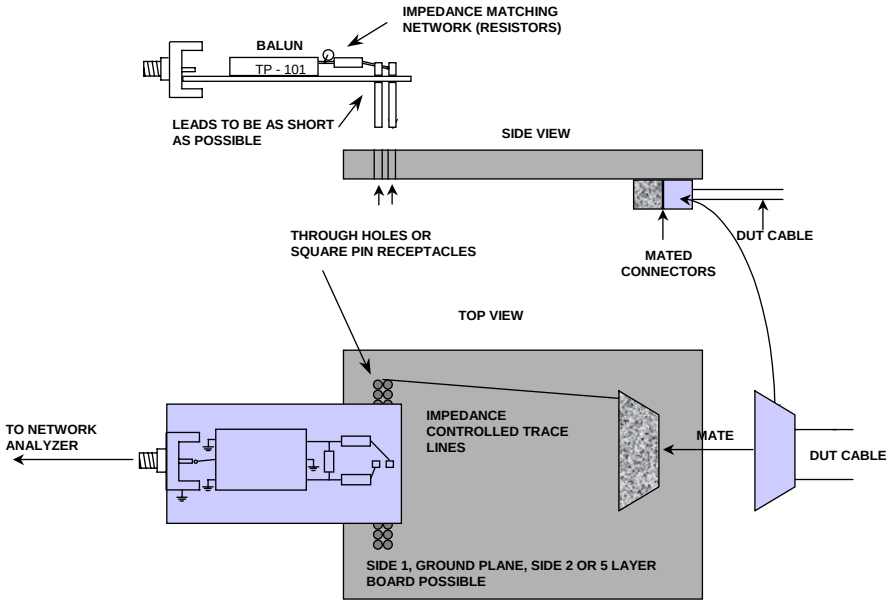


Figure 24 - Test fixture (FIX_ASY_4)

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS
Not for Resale

Figure 25 shows detail for balun board shown in figure 24.

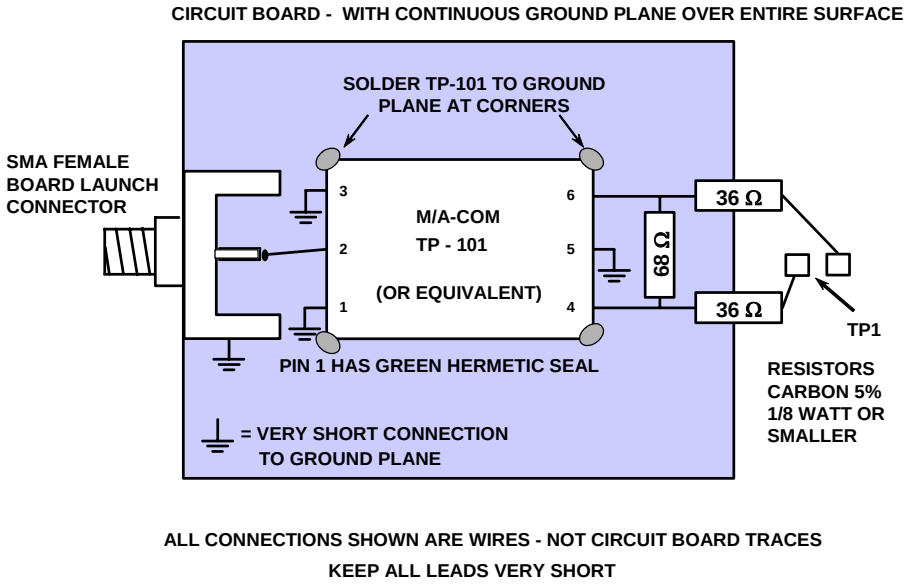


Figure 25 - Detail for balun board shown in figure 24

9.3 Interconnect assembly measurement equipment and setups

9.3.1 Summary

Table 11 shows the interconnect assembly measurement equipment and setups.

Table 11 - Interconnect assembly measurement equipment and setups

Measurement	Construction	Point-to-point sample type	Multi-drop sample type
Differential local impedance	Unshielded and shielded	SET_ASY_1, (9.3.2)	SET_ASY_1, (9.3.2)
Propagation time and propagation time skew	Unshielded and shielded	SET_ASY_2, (9.3.3)	SET_ASY_2, (9.3.3)
Differential signal integrity diagrams (eye and TDW) and differential to common mode conversion	Unshielded and shielded	SET_ASY_3, (9.3.4)	SET_ASY_3, (9.3.4)
Differential insertion loss	Unshielded and shielded	SET_ASY_4, (9.3.5)	SET_ASY_4, (9.3.5)

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS
Not for Resale

9.3.2 Set up (SET_ASY_1)

Figure 26 shows interconnect assembly set up 1 (SET_ASY_1).

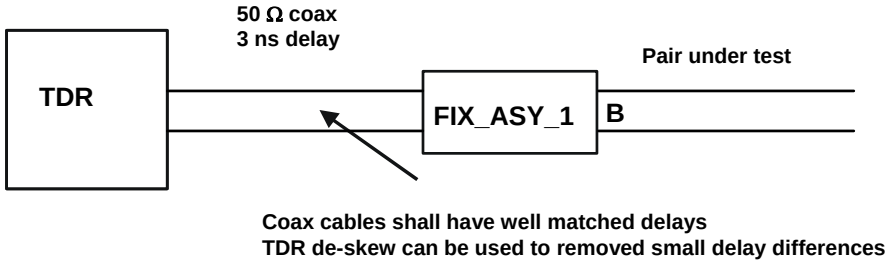


Figure 26 - Interconnect assembly set up 1 (SET_ASY_1)

9.3.3 Set up (SET_ASY_2)

Figure 27 shows interconnect assembly set up 2 (SET_ASY_2).

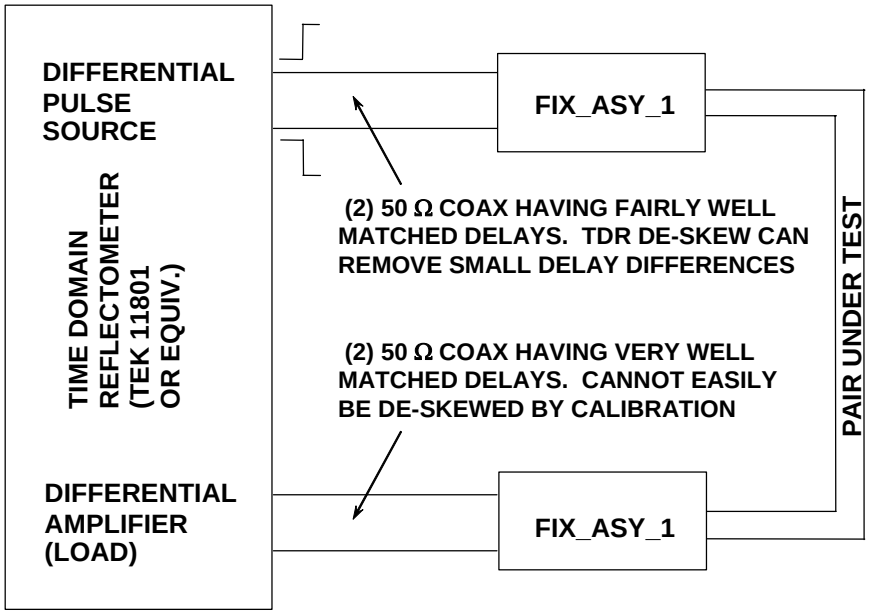


Figure 27 - Interconnect assembly set up 2 (SET_ASY_2)

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

9.3.4 Set up (SET_ASY_3)

Figure 28 shows Interconnect assembly set up 3 (SET_ASY_3).

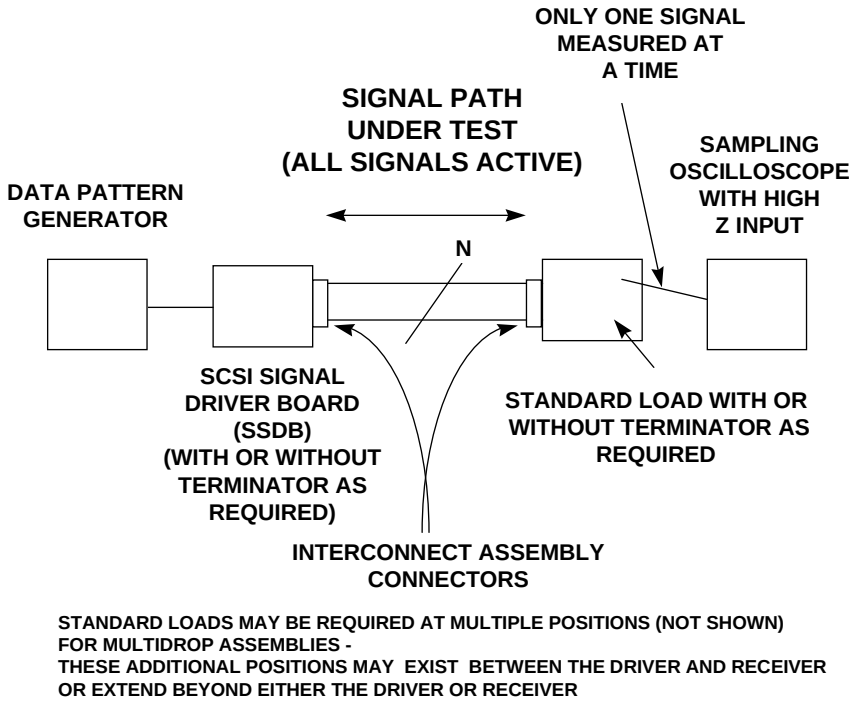


Figure 28 - Interconnect assembly set up 3 (SET_ASY_3)

9.3.5 Set up (SET_ASY_4)

Figure 29 shows interconnect assembly set up 4 (SET_ASY_4).

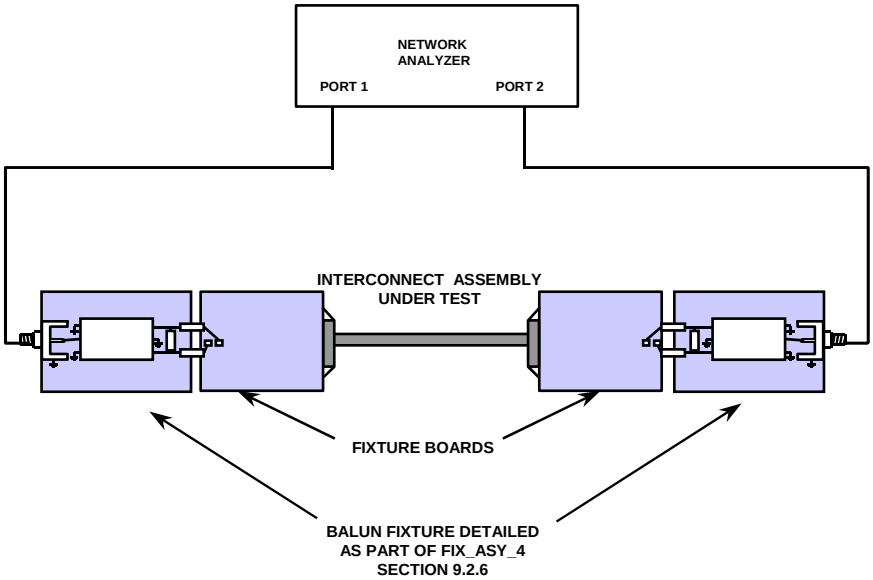


Figure 29 - Interconnect assembly set up 4 (SET_ASY_4)

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS
Not for Resale

9.4 STD Calibration

The STD calibration procedure for interconnect assemblies is the same as that described in 6.4 for bulk cable.

10 Level 1 interconnect assembly tests

10.1 Differential impedance

10.1.1 Overview

This requirement is necessary to ensure that the interconnect assembly has the basic impedance level provided by the bulk cable. Requirements relating to reflections in the system are included in the signal integrity diagram tests. The impedance values used for specification compliance are recorded only in the bulk cable portion of the interconnect assembly.

If there is no clearly identifiable bulk cable portion in the regions defined in 7.2.2.5 and 7.2.3.5 then requirements under 10.1 are not applicable.

The impedance in the connector and transition regions may be visible in the measurements, however, there are no performance requirements specified for the connector and transition regions. No standard loads are used for these measurements. The STD used is 1 ns. The connector and the transition regions are not expected to determine the interconnect assembly differential impedance performance with loads.

10.1.2 Point-to-point interconnect assemblies

10.1.2.1 Test fixtures for point to point interconnect assemblies

Test fixtures for point to point interconnect assemblies are defined in 9.2.3.

10.1.2.2 Measurement equipment and setup for point to point interconnect assemblies

Measurement equipment and setup for point to point interconnect assemblies is defined in 9.3.2.

10.1.2.3 Calibration and verification procedure for point to point interconnect assemblies

Use the same requirements as specified in 7.2.2.4.

10.1.2.4 Test procedure and data output format for point to point interconnect assemblies

Use the same requirements as specified in 7.2.2.5. In the case of assemblies, where the time scale called out for measurement exceeds the length of the cable assembly be sure to readjust the right cursor to accommodate the short assembly.

10.1.3 Multi-drop interconnect assemblies

Use the same requirements as specified in 10.1.2 in its entirety.

10.1.3.1 Test fixtures for multi-drop interconnect assemblies

Test fixtures for multi-drop interconnect assemblies are defined in 9.2.3.

10.1.3.2 Measurement equipment and setup for multi-drop interconnect assemblies

Measurement equipment for multi-drop interconnect assemblies are defined in 9.3.2.

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

10.1.3.3 Calibration and verification procedure for multi-drop interconnect assemblies

Use the same requirements as specified in 7.2.2.4.

10.1.3.4 Test procedure and data output format for multi-drop interconnect assemblies

Use the same requirements as specified in 7.2.3.5.

10.1.4 Connectorized backplanes

Use the same procedures and equipment defined for multi-drop interconnect assemblies with appropriate modifications for the PCB structure being used.

10.1.5 Acceptable values for all constructions of interconnect assemblies

Acceptable values for multi-drop interconnect assemblies shall be between 110 Ω and 135 Ω.

10.2 Differential propagation time and propagation time skew

10.2.1 Overview

This test measures the differential signal propagation time and pair to pair skew. This test is performed on interconnect assemblies that are terminated with connectors consistent with SCSI signal assignments specified in SPI-x. Propagation time skew is the difference between the propagation time between two port connectors of any two signals in the interconnect assembly when the signal is driven from the same port for both signals. Multidrop interconnect assemblies have all the loads in place when the measurement is done.

Propagation time skew requirements apply only to initiator/target port combinations. The maximum propagation time skew for any specific combination of ports is the maximum difference in propagation time between any two signals. The maximum propagation time skew for the interconnect assembly is the largest port to port skew found for any pair of ports that act as initiator/target pairs.

10.2.2 Point-to-point interconnect assemblies

10.2.2.1 Test fixtures for point to point interconnect assemblies

This test requires the test fixture defined in 9.2.3.

10.2.2.2 Measurement equipment and setup for point to point interconnect assemblies

This test requires the measurement equipment and setup defined in 9.3.3.

10.2.2.3 Calibration and verification procedure for point to point interconnect assemblies

Use the same requirements as specified in 7.3.2.4.

10.2.2.4 Test procedure and data output format for point to point interconnect assemblies

Use the same requirements as specified in 7.3.2.5.

10.2.3 Multi-drop interconnect assemblies

Use the same requirements as specified in 10.2.2 except that standard loads appropriate for the connector function shall be in place for all connectors that are not used as the driver or receiver for the measurement.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

10.2.4 Connectorized backplanes

Connectorized backplanes are treated as a multidrop interconnect assembly for propagation time measurements.

Due to the small size of backplanes the propagation time is likely to be significantly smaller than for cable based interconnect assemblies. The propagation time skew, however, may be significantly larger in a backplane than in a similar length cable based interconnect assembly.

10.2.5 Acceptable values for all constructions of interconnect assemblies

The propagation time from initiator connector to target connector shall not exceed 160 ns. The propagation time skew from initiator connector to target connector shall not exceed 2.5 ns.

10.3 Signal integrity diagrams

10.3.1 Overview

Signal integrity diagrams are used to determine the quality of the signal delivered to the receiver at the device connector. Two methods are used: eye diagrams and time domain waveforms (TDW).

An eye diagram is an amplitude/time representation of a series of signals displayed on a common scale for each bit time. A single bit time is used for the display. The eye diagram is used to determine the extreme timing and amplitude populations in the signal in the presence of cross talk and complex data patterns.

The timing reference for measuring eye diagrams shall be derived from the same timing reference used to generate the driver signals and shall remain the same during the entire data acquisition process for any signals measured. The position of the eye mask that determines compliance shall be set using the methods described in SPI-5.

Requirements based on signal integrity diagram measurements shall be met at the nominal data rate, 10 % above the nominal data rate and 10 % below the nominal data rate to account for effects not present in the specific measurement condition such as resonant conditions, small length differences, and load variations.

Differential to common mode conversion measurements (see 10.4) are also made using the methods described for eye diagrams with only a change in the signal recording scheme.

A TDW is a time domain display of the entire waveform for the repeating data pattern. Detailed structure is visible from individual transitions with this methodology. It is used to determine if the required signal amplitudes and transition rates specified in SPI-3, SPI-4, and SPI-5 are met.

The TDW is acquired from a measurement that uses a repeating data pattern having the properties described in SPI-5 and a sampling oscilloscope set to trigger off a timing reference that is derived from the same timing reference (clock) used to generate the driver signals. The position of the TDW masks shall be set using the methods described in SPI-5.

In order to include the effects of precompensation, driver slew rate, and cross talk the driver used for the signal integrity diagram tests shall meet the SCSI driver requirements and shall excite all signal lines in a manner that emulates a SCSI data phase transmission from an active SCSI port. The received signal on any signal line is compared to the requirements at the receiver stated in SPI-x to determine compliance. Signal integrity diagrams are not intended for determining compliance to signal to signal skew requirements.

Only far end cross talk is included in the received signal. Near end cross talk in a compliant SCSI interconnect in the REQ or ACK signal is small because the REQ and ACK signals are physically separated from the data signals.

Far end cross talk is produced by drivers located in the same chip with the result that all signals are driven with approximately the same amplitude. It is further assumed that all signals are substantially in phase at the SCSI signal driver board launch point. This allows a accurate scaling for cross talk without requiring a separate cross talk aggressor source. It is recognized that pair to pair skew during transmission may affect the far end cross talk but this skew is caused by the interconnect and is accurately included in the measured signal as part of the interconnect performance.

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

A significant practical consideration is procurement of a SCSI signal driver board that meets the requirements defined in Annex C. If a dedicated SSDB is not available then an active SCSI port, for example a commercial host bus adapter, may be used in place of the SSDB and the requirements at the receiver shall be scaled to account for the driven signal being better than allowed by the worst case specification. For example, if the host bus adapter delivers 1 000 mV peak to peak but the worst case driver is allowed to deliver 500 mV peak to peak then the requirements for the received signal are all doubled for amplitude properties.

Data patterns specified for interconnect assembly performance are the serial data patterns that exist on the signal line under test. The serial data pattern on a single signal line bears little relationship to the payload data transferred between SCSI ports in the data phase since the latter is constructed from bytes existing across all data bit lines at the same time. See figure 30.

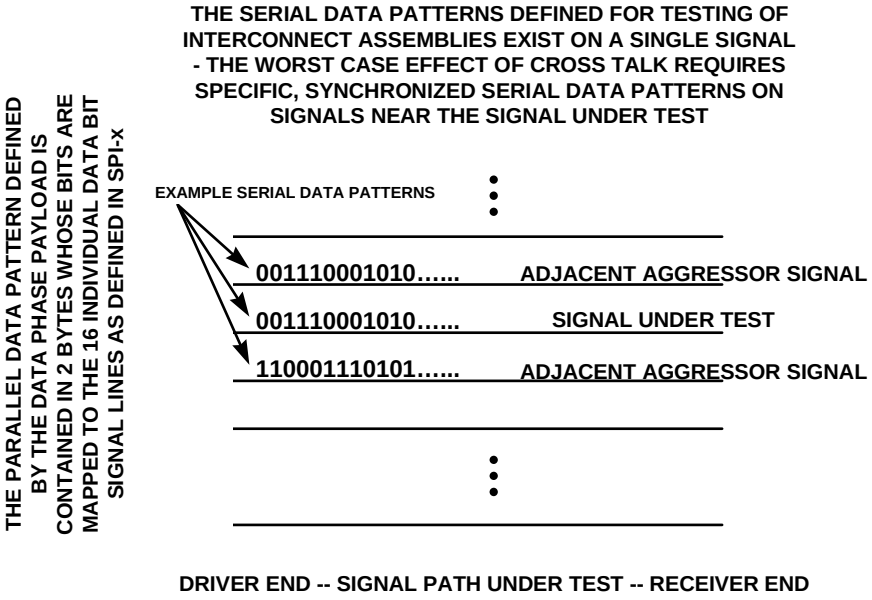


Figure 30 - Distinction between parallel and serial data in the same signal path

If a host bus adapter is used as the driver for interconnect assembly measurements the serial data pattern requirements for the signal under test and the neighboring aggressor signals shall be constructed from data phase payload data patterns. The data phase payload patterns shall produce the serial data pattern required by ordering the sequence of bytes such that the bit position in the byte sequence is transmitted on the required signal line and has the required serial data pattern for the signal line. Since a 2-byte parallel transfer is used, every other byte in the data phase payload contains the required bit position for the same signal.

When using SCSI devices as the driver, only the bits in the data phase shall be examined. This may be accomplished by gating the instrumentation by a logic analyzer programmed to detect data phases.

The cross talk performance is a result of the sum of all aggressor signals on the signal under test. PIP recognizes that the primary effect of cross talk comes from the signals that are physically adjacent in the connector to the signal under test and places the most stringent requirements on the adjacent signals. The physically adjacent signals are termed aggressor signal "A" and aggressor signal "B" in this document. Only data bits, clock, and parity signals are considered valid aggressor signals.

The polarity of the cross talk comes from the sense of the signal transition (i.e., 0 to 1 or 1 to 0) on the aggressor line and on the type of coupling between the aggressor signal and the signal line under test that causes the cross talk. If the aggressor signal has a 0 to 1 or a 1 to 0 transition when the signal under test also has a 0 to 1 or a 1 to 0 transition respectively the aggressor signal and the signal under test are 'in phase'. If the aggressor signal has a 0 to 1 or a 1 to 0 transition when the signal under test has a 1 to 0 or a 0 to 1 transition respectively the aggressor signal and the signal under test are 'out of phase'.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

PIP requires that all combinations of aggressor signal phases be examined for aggressor "A" and aggressor "B" but that the phase of more remote aggressors not be restricted. There are four possible aggressor signal phase relationships with respect to the data pattern on the signal under test: both aggressor signals in phase, both aggressor signals out of phase, aggressor A in phase / aggressor B out of phase, and aggressor "A" out of phase / aggressor "B" in phase. For the signals that have only a single adjacent aggressor signal only that aggressor signal need be considered.

10.3.2 Requirements for all constructions of interconnect assemblies

10.3.2.1 Test fixtures for all constructions of interconnect assemblies

The test fixtures described in 9.2.5 and 9.2.4 are used. FIX_ASY_2 is used on the receiver end and the driver end uses FIX_ASY_3 or a suitable SCSI device port.

10.3.2.2 Measurement equipment and setup for all constructions of interconnect assemblies

Use the set up described 9.3.4 with a terminated SCSI signal driver board (SSDB) described in Annex C. A host bus adapter or other SCSI port may also be used for the driver as described in 10.3.1. Signals shall be measured using a TEK 11801 oscilloscope or equivalent. If using an SSDB, a programmable bit pattern generator shall be used to create the required data patterns delivered to the SSDB. If a host bus adapter or other SCSI port is used as described in 10.3.1 the data phase payload shall be such that the serial data patterns specified below are delivered to the signal line under test. The data patterns that shall be available are:

a) 2^7-1 - pseudo random bit sequence (PRBS)
b) 16 zeros, 1 one, 16 zeros, 16 ones, 1 zero, 16 ones, repeat - driver calibration pattern (DCP)
c) 11000001010011111010110000010101 repeat - time domain waveform pattern (TDWP)
d) clock like data pattern meeting the non-precomp launch requirements specified in 10.3.2.3.2

The phase relationship of the signals physically adjacent to the signal under test shall be capable of meeting all of the following requirements at the driver:

a) data pattern on both adjacent signal "A" and adjacent signal "B" are in phase with the data pattern on the signal under test
b) data pattern on both adjacent signal "A" and adjacent signal "B" are out of phase with the data pattern on the signal under test
c) data pattern on adjacent signal "A" is in phase with the data pattern on the signal under test while adjacent signal "B" is out of phase
d) data pattern on adjacent signal "A" is out of phase with the data pattern on the signal under test while adjacent signal "B" is in phase

One may create an enhanced combination PRBS or TDWP for the SSDB or SCSI port used for the driver that includes the four different phase relationships for the aggressor signals.

10.3.2.3 Calibration and verification procedure for all constructions of interconnect assemblies

10.3.2.3.1 Overview

The calibration procedure shall be executed independently for non-precomp drivers and precomp drivers. The interconnect assembly shall meet the requirements for both non-precomp and precomp drivers.

10.3.2.3.2 Non-precomp driver requirements

Non-precomp drivers do not modify the driven signal based on the data pattern. The properties of the non-precomp driver signal shall conform to the requirements in this sub clause.

Calibration of the driver shall be done with the load specified in 4.10.3.1 attached to the driver connector.

It may not be practical to generate driven signals that meet all the worst case properties. In this case, the requirements on the received signal shall be modified in direct proportion to the difference between the actual driven signal and the worst case requirements.

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

The signal launched into the driven pair under test shall have 740 mV_{pp} with a rise time of (1,0 ± 0,1) s. If 740 mV is not achievable in the equipment available, then the requirements on the received signal shall be scaled by the same percentage as the percentage that the launch signal is different from 740 mV.

If the maximum allowed jitter is not present in the driven signal, the requirements on the received signal shall be adjusted by the difference between the actual jitter and the allowed worst case jitter.

The data pattern for the signal driven on the pair under test during calibration shall be the DCP which is in sequence: 16 zeros, 1 one, 16 zeros, 16 ones, 1 zero, 16 ones, repeat. The data pattern driven during calibration on the signal pairs not under test shall be clock-like at the same data rate as the data pattern on the pair under test.

10.3.2.3.3 Precomp driver requirements

Precomp drivers modify the driven signal as specified in SPI-4 by using cutback. The properties of the cutback driver signal shall conform to the requirements in this sub clause.

Calibration of the driver shall be done with the load specified in 4.10.3.1 attached to the driver connector.

The signal launched into the driven pair under test shall use 33 % cutback, that is the maximum amplitude less 33%, with a weak driver at 740 mV_{pp} ± 50 mV and a rise time of (1,0 ± 0,1) ns. If 740 mV is not achievable in the equipment available, then the requirements on the received signal shall be scaled by the same percentage as the percentage that the launch signal is different from 740 mV.

Maximum allowed jitter is present in launched signal - the receiver requirements shall be adjusted to account for maximum launch jitter if the maximum jitter is not present in launch signal used for the test.

Data pattern running during the testing during calibration shall be clock like on all data signals except for the signal under test. The signal under test shall be the DCP which is in sequence: 16 zeros, 1 one, 16 zeros, 16 ones, 1 zero, 16 ones, repeat. The data pattern driven by the SSDB on the signal pairs not under test shall be clock-like at the same data rate as the data pattern on the pair under test.

10.3.2.4 Test procedure and data output format for all constructions of interconnect assemblies

Connect the SSDB or SCSI device port used as the test driver to the driver port with the same calibration conditions determined in 10.3.2.3. Connect the receiver test fixture to the receiver port. Add the appropriate standard loads to all other ports. Measure the eye pattern of the signal at the receiver port for enough time to allow the extremes of the eye to develop. It is required that the eye be open (that is, not closed), so that a height and width of the eye is measurable. Change the data pattern if required and measure the TDW performance for enough time to allow the extremes of the waveform population to develop for all conditions of driver mode and data pattern required in SPI-x.

All four aggressor conditions shall be met in the data pattern used by the driver port (SSDB or other SCSI port) or each of the four aggressor conditions shall be independently measured for both eye diagram and TDW measurements. If each aggressor condition is measured independently the number of measurements required is increased by four times.

Repeat the eye and TDW measurements for both precomp (SPI-4 only) and non-precomp drivers and for all combinations of ports and loading that are intended for the interconnect assembly under test.

The data output format shall be any of the standard formats offered by manufacturers of the measurement equipment.

An example of the tests required for the simplest multi-drop interconnect assembly with three connectors, 1, 2, 3 where 1 is always the initiator device and 2 and 3 are always target devices is shown in . Connectors 1 and 3 are always terminated in this example. At least one of the connectors, 2 or 3, has a target device attached.

The requirements in are the formal requirements for the example cited. A large number of measurements are specified for complete coverage even in this very simple example. It is expected that implementers will practically execute only a small subset of the combinations required for complete coverage but rather will execute based on the known worst case positions in the interconnect assembly and previous experience with the loading and other conditions that are most likely to produce a failure.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

Table 12 - Test array example for a three port interconnect assembly

Driver condition: (Use 2^7-1 PRBS for eye diagrams and the TDWP for TDW)	Driver port (SSDB position)	Receiver port (eye measurement position)	Loading condition per 4.9.1
Precomp	Connector 1	Connector 3	Connector 1 load 'b' Connector 2 load 'i' Connector 3 load 'g'
Precomp	Connector 1	Connector 3	Connector 1 load 'b' Connector 2 open Connector 3 load 'g'
Precomp	Connector 1	Connector 2	Connector 1 load 'b' Connector 2 load 'i' Connector 3 load 'g'
Precomp	Connector 3	Connector 1	Connector 1 load 'g' Connector 2 load 'i' Connector 3 load 'b'
Precomp	Connector 3	Connector 1	Connector 1 load 'g' Connector 2 open Connector 3 load 'b'
Precomp (only if target to target communication is required)	Connector 3	Connector 2	Connector 1 load 'g' Connector 2 load 'i' Connector 3 load 'b'
Precomp	Connector 2	Connector 1	Connector 1 load 'g' Connector 2 load 'd' Connector 3 load 'g'
Precomp (only if target to target communication is required)	Connector 2	Connector 3	Connector 1 load 'g' Connector 2 load 'd' Connector 3 load 'g'
Repeat all above conditions for non-precomp driver.			

The following conditions apply to every driver-receiver connection:

[a] Every signal shall be measured according to the above 12 or 16 eye diagrams and 12 or 16 TDW plots. Assuming that a test port driver condition is used that sequences the four types of aggressor signal relationships to the signal under test in a single data pattern it requires 12 x 19 = 228 or 16 x 19 signals = 304 diagrams of each type (608 total) for this simple three connector assembly where all connectors are uniquely initiator or target. If any connector were to be used for both initiator and target mode then 20 signals would be required for that connector and additional driver-receiver connections would be need to be measured to account for the additional configurations that could exist.

[b] The aggressor signals used to produce the cross talk that is required to be present while making the signal integrity diagram measurements are supplied by the SSDB.

[c] When measuring the free running clock signals the free running clock data pattern shall be used on the signal under test.

10.3.2.5 Acceptable values for all constructions of interconnect assemblies

The acceptable values for the signal integrity diagrams are specified in SPI-3, SPI-4, and SPI-5 as receiver masks under different data pattern conditions and driver mode conditions. There are a different number of masks specified for the different speeds and driver modes in SPI-3, SPI-4, and SPI-5. For SPI-4, where both precomp and non-precomp drivers are specified, the interconnect assembly shall meet the requirements for both precomp and non-precomp drivers.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

10.4 Differential to common mode conversion

10.4.1 Overview

The differential to common mode conversion requirements are all measured exactly the same way as specified in 10.3 except that the signal measurement is done with the oscilloscope set to measure the sum of the + and - signals instead of the difference. This requires an instrument that is capable of measuring both legs independently. This means that differential probes may not be used.

There are no requirements on the TDW form of common mode.

10.4.2 Requirements for all constructions of interconnect assemblies

10.4.2.1 Test fixtures for all constructions of interconnect assemblies

The same text fixtures defined in 10.3.2.1 shall be used.

10.4.2.2 Measurement equipment and setup for all constructions of interconnect assemblies

The same measurement equipment and setup defined in 10.3.2.2 shall be used except that the oscilloscope shall be capable of detecting signals on both the + and - signals in the differential pair.

10.4.2.3 Calibration and verification procedure for all constructions of interconnect assemblies

The same calibration and verification procedures defined in 10.3.2.3 shall be used except that the driver signals shall be measured for common mode content and verified to be less than 100 mV above the level set by the terminators. If levels greater that this are measured then the SSDB shall either be adjusted or replaced. The common level set by the terminators is measured by setting all drivers to the high impedance state.

10.4.2.4 Test procedure and data output format for all constructions of interconnect assemblies

The same test procedures and data output formats defined in 10.3.2.4 shall be used except that the sum of the + and - signals in each signal shall be used. This sum is twice the common mode content. All requirements are on the eye diagram display.

There is no expectation that the common mode eye has an opening. The relevant property is the peak value measured from the level set by the terminators. There may be a small effect from common mode content in driven signals, however, the requirements for compliance take that into account.

10.4.2.5 Acceptable values for all constructions of interconnect assemblies

The common mode level in the received signal shall not be more than 355 mV different from the common mode level set by the terminators.

10.5 Differential insertion loss

10.5.1 Overview

Differential insertion loss measurement is useful as a diagnostic tool for point to point interconnect assemblies and for the signal path between the connectors that have the enabled SCSI termination and is a level 2 measurement. Due to impedance matching requirements for network analyzers the point of attachment effectively provides bus termination. Other termination on the bus segment causes excessive termination and should be avoided. The multidrop differential insertion loss is measured between the end connectors only.

For multidrop interconnect assemblies a standard load with no enabled termination shall be attached to the connectors not on the end of the assembly during the measurement.

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

It is known that sharp resonances and suckouts may exist in high performance copper interconnect systems, especially those that have periodic disturbances of the type that are expected in multi-drop architectures with loads attached. Annex B contains further information about the effects of periodic structures.

The differential insertion loss for interconnect assemblies may be significantly different from that measured in bulk cables. This difference is expected to be significant for multidrop assemblies. The insertion loss measurement methodology is essentially identical for both interconnect assemblies and bulk cables.

The finding of excessive suckouts at some frequencies may be useful in diagnosing the causes of signal integrity diagram problems.

10.5.2 Requirements for all constructions of interconnect assemblies

10.5.2.1 Test fixtures for all constructions of interconnect assemblies

Use FIX_ASY_4 (2 required) and unterminated standard loads specified in 9.2.6 and 4.9.3.1.

10.5.2.2 Measurement equipment and setup for all constructions of interconnect assemblies

Use SET_ASY_4 specified in 9.3.5.

10.5.2.3 Calibration, verification, and measurement procedure for all constructions of interconnect assemblies

Use the procedure specified in 7.6.2.4.

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

Annex A
(normative)

Single ended bulk cble requirements

A.1 Overview

This annex defines the electrical measurement methodology requirements to be used for single ended shielded and unshielded bulk cable. These requirements are intended to be identical to those defined in SPI-x for single ended applications. Some terminology has been changed to reflect the most current usage.

The methodologies are specified to extract parameters for each of the following performance requirements:

a) Transmission line impedance (Z_O),
b) capacitance,

A.2 Impedance

A.2.1 Local impedance for SE transmission

A.2.1.1 Local impedance for SE transmission overview

The impedance measurement produces a plot of transmission line impedance as recorded by a time domain reflectometer instrument. There is a direct mapping of the measurements to the physical position within the cable under test. The test shall be performed at the specified signal transition duration time for the signals being used in the end-user application.

The sample length is long enough to ensure no interference from the far end.

A.2.1.2 Sample preparation

This test requires samples prepared in the following way:

1) Cut sample length to 3 ± 0,025 m.
2) Remove 50 mm of outer jacket from one end.
3) Comb out braid wire strands to form a pigtail.
4) Trim filler and tape materials to the base of braid wire.
5) Strip 5 mm insulation from all conductors.
6) Connect one wire from each pair to the shield (for planar type cable, tie every other conductor to ground).

A.2.1.3 Test fixture and measurement equipment

Figure A.1 shows the test configuration for the local single ended impedance test.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

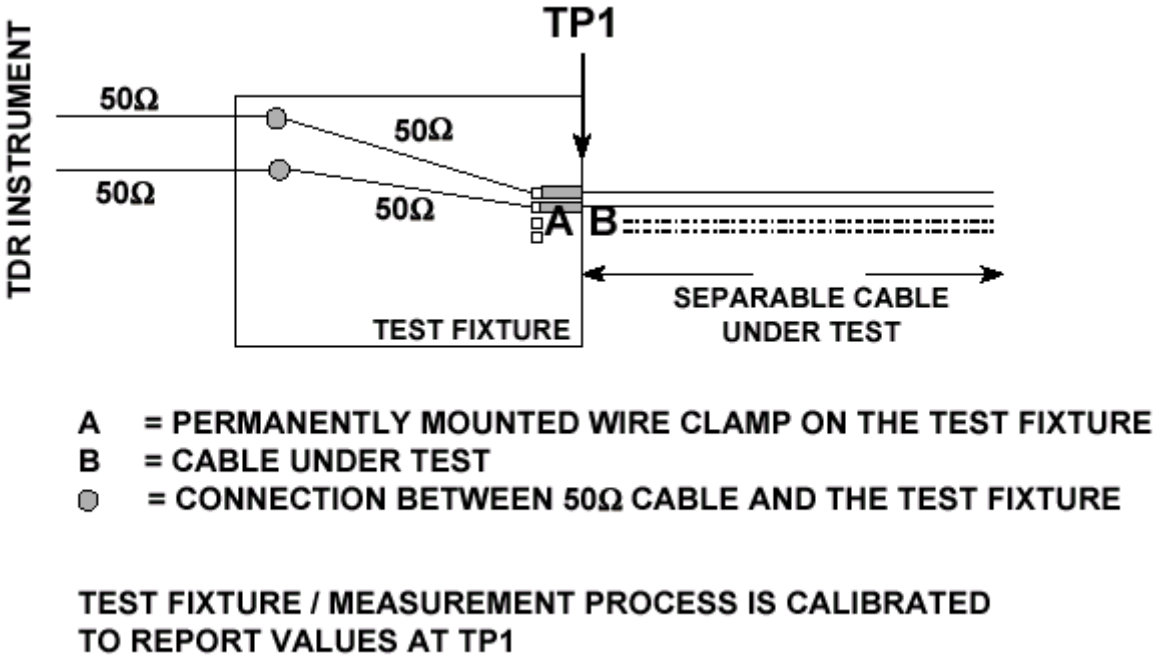


Figure A.1 - Test configuration for SE impedance

The test fixture may be constructed of semi-rigid coax, microstrip PCB, or stripline PCB. To be able to see the entire signal transition it is necessary that the length from the TDR to the DUT be long enough to contain the complete transition. For the 3 ns STD this minimum length is approximately 1,25 m for cables with solid polyethylene dielectric. For other dielectrics this length should be adjusted appropriately.

A.2.1.4 Calibration and verification procedure

A.2.1.4.1 Instrument verification

It is not necessary to perform a separate instrument verification for this test. The calibration in the following sub clause includes the instrument.

A.2.1.4.2 Measurement system (with test fixture) calibration

Connect the 50 Ω cable to the test fixture. In place of “B” in figure A.1, connect a 100 Ω ± 0,1 % (preferred) low inductance chip resistor (i.e., IMS style TPI-1206 or equivalent). Use an unfiltered trace and the TDR cursors to measure the resistance value, R100, approximately 4 ns (displayed) after the resistor discontinuity. See figure A.2.

In a similar manner, in place of “B” in figure A.1, connect a 75 Ω ± 0,1 % (preferred) low inductance chip resistor. Use an unfiltered trace and use the TDR cursors to measure the resistance value, R75, approximately 4 ns (displayed) after the resistor discontinuity.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

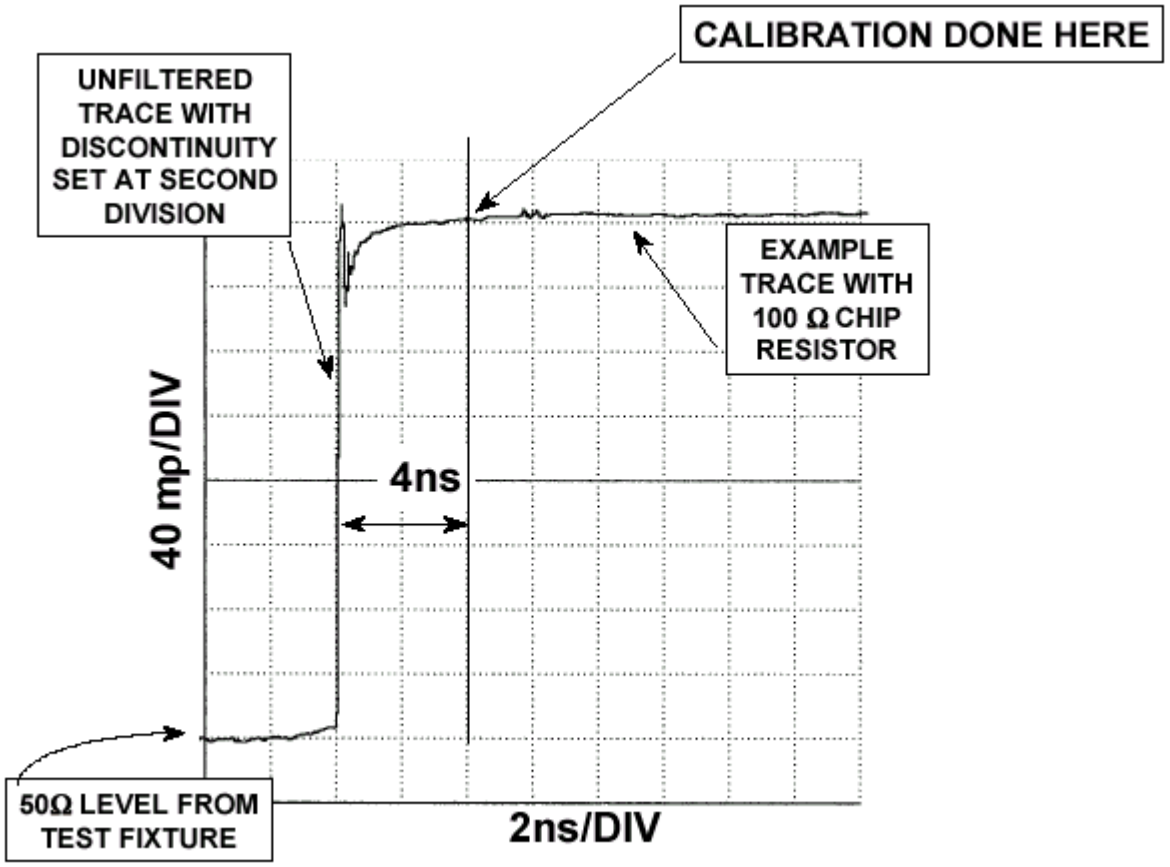


Figure A.2 - SE impedance calibration

For R100 and R75 the equation for determining the corrected (i.e., actual) impedance is:

$$Z_{corrected} = \frac{25 \times (((4 \times X_1) - (3 \times X_2)) - Z_{measured})}{X_1 - X_2}$$

Where:

a) X_1 is the measured value using the 75 Ω resistor
b) X_2 is the measured value using the 100 Ω resistor

A.2.1.4.3 Single ended signal transition duration (STD) calibration

This step ensures that the proper signal transition (STD) time is being presented to the DUT. Place a short on the test fixture where the cable would be attached in place of “B” in figure A.1. Use the filter function on the TDR to set the measured STD (20 % to 80 %) to the required value according to the detailed procedure described below. It may be desirable to use a separate test fixture that is nominally identical to the actual cable test fixture for this step.

Assuming a falling edge, set up the display on the TDR as shown in figure A.3. This display has the following properties:

a) The time scale on the display is 2,0 ns / div for the 3,0 ns STD.
b) Set the horizontal position such that the midpoint of the displayed curve is near the center of the display and the 100 % and 0 % baselines are clearly visible as shown in figure A.3.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

The STD is the time between the 20 % and 80 % values of the displayed signal amplitude (most instruments do this calculation automatically). When the instrument does not automatically measure STD, perform the following steps:

1) Measure the voltage at 100 % (V_{100}).
2) Measure the voltage at 0 % (V_0).
3) The voltage at 20 % is $V_{20} = V_0 + 0{,}2(V_{100} - V_0)$.
4) The voltage at 80 % is $V_{80} = V_0 + 0{,}8(V_{100} - V_0)$.
5) Set cursors at V_{20} and V_{80} and measure the time difference.

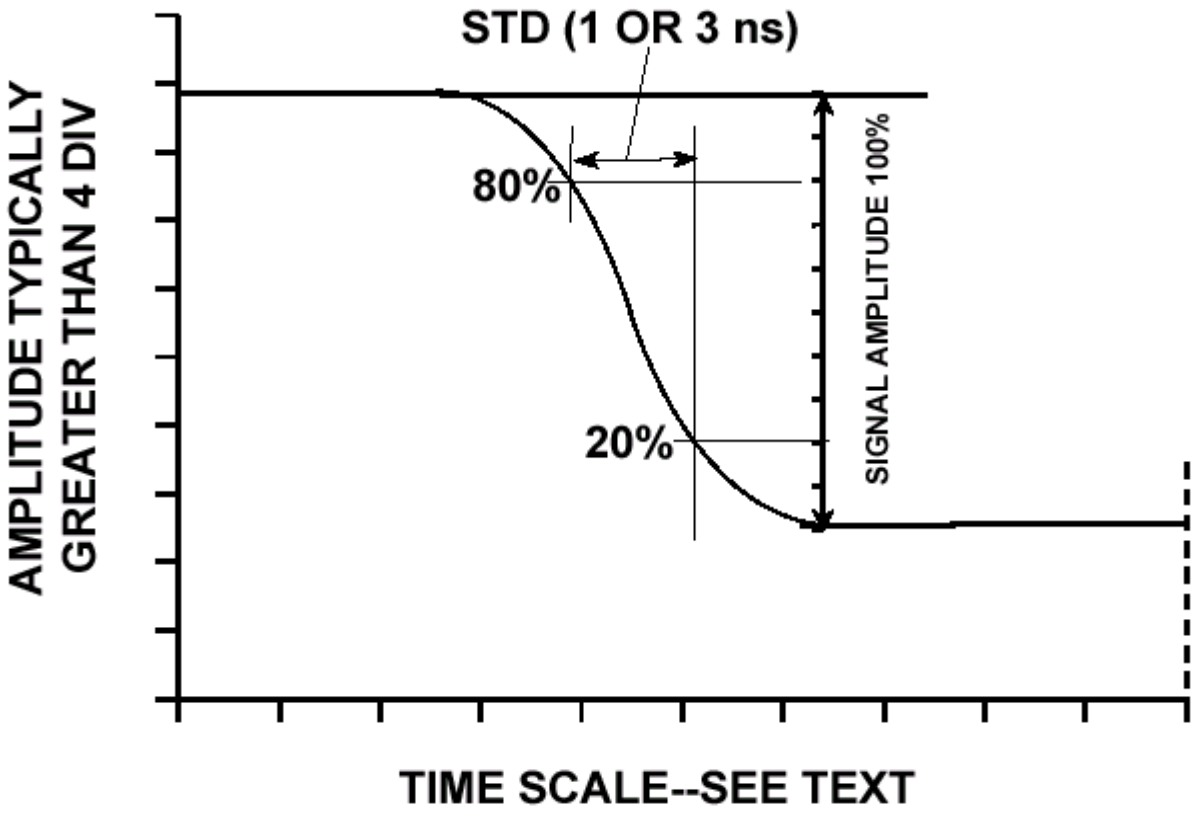


Figure A.3 - Signal transition duration calibration

A.2.1.5 Testing procedure

Connect the DUT to the test fixture wire clamp and record the TDR trace using the method described below.

a) Set the time scale to 2 ns / div (total time axis span of 20 ns).
b) Set the vertical scale (mρ) to 40 mρ / div.
c) With the DUT disconnected turn off the filtering.
d) Next, set the horizontal position such that the discontinuity is on the third division from the left.
e) Adjust the vertical position to approximately place the 50 Ω reference (cable from fixture to TDR) at the first vertical division from the bottom.
f) With the rise time filter adjusted to achieve 3 ns connect the DUT.
g) Unshielded DUT shall be suspended in air. No metallic supports should be used.
h) Set the TDR cursor to measure the minimum and maximum Ohms with cursors set on the trace as it crosses the 5^{th} and 6^{th} times divisions.

These measurements ignore the small error factor caused by losses in the cable which varies with gauge size. This error increases the measured impedance slightly.

--`,,```,,,,````-`-`,,`,,`,`,,`---

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

Figure A.4 shows the TDR display setup to use for this measurement.

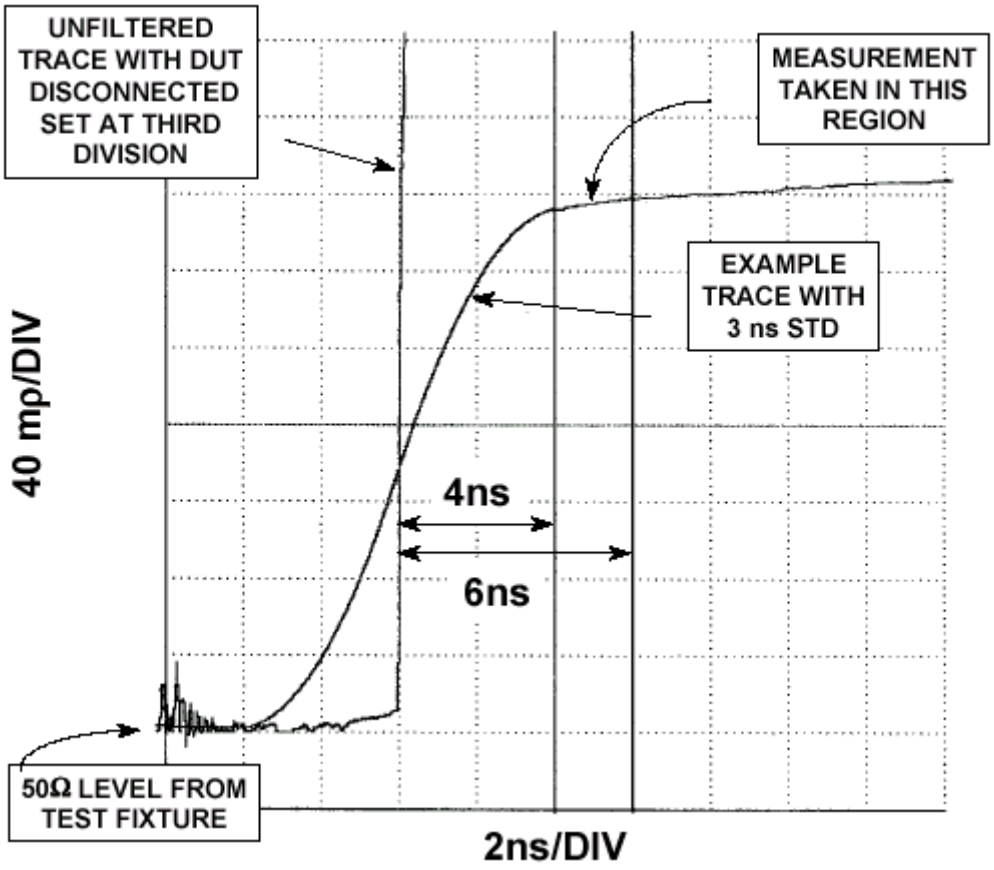


Figure A.4 - SE impedance measurement

A.3 Capacitance

A.3.1 Single ended capacitance

A.3.1.1 Sample preparation

This test requires samples prepared in the following way:

For planar cables:

1) Cut sample length to 3 m.
2) Separate conductors at one end.
3) Strip 5 mm insulation from all conductors.

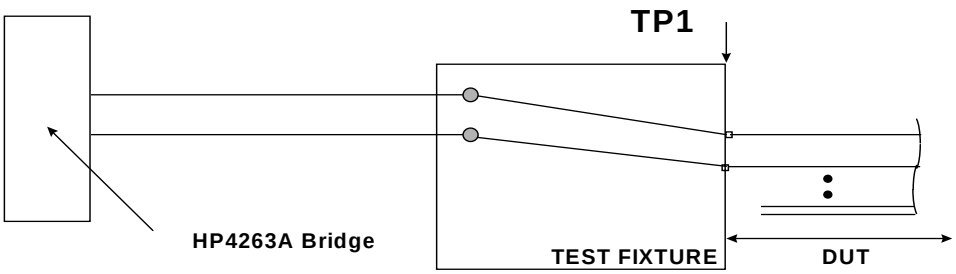
For round cables shield connected:

1) Cut sample length to 3 m.
2) Remove 50 mm of outer jacket from one end.
3) Comb out braid wire strands to form a pig tail.
4) Trim filler and tape materials to the base of braid wire.
5) Strip 5 mm insulation from all conductors.
6) Connect one (1) conductor of each pair to the shield.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

A.3.1.2 Test fixture for single ended capacitance

Figure A.5 shows the test configuration for the single ended capacitance tests.



TEST FIXTURE / MEASUREMENT PROCESS IS CALIBRATED TO REPORT AT TP1

Figure A.5 - Test fixture for single ended capacitance measurement

A.3.1.3 Calibration procedure

If using an HP4263A or equivalent bridge, calibration shall be as follows:

1) Connect fixture to meter and perform open calibration as specified by the bridge.
2) Connect a wire (short) to the sockets of the test fixture and perform a “short” calibration as specified by the bridge.

For other manufacture’s equipment, follow the calibration procedures specified by the manufacturer of the LCR bridge for reliable results.

A.3.1.4 Measurement procedure

A.3.1.4.1 Planar cables - G-S-G

With the bridge set at the required frequency, connect the two grounds together on one side of the test fixture and the signal to the other side of the test fixture, record the capacitance.

A.3.1.4.2 Round cables - shielded

With the bridge set at the required frequency, connect one conductor of the twisted pair to one side of the test fixture. Connect the common conductors and shield to the other side of the test fixture (ground). Record the capacitance.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

Annex B
(informative)

Periodic structure effects

Passive interconnect is subject to very significant performance effects due to features that repeat with length. Examples of periodic structures are twist period in pairs, foil wrap shield period, connector placement in multidrop interconnect assemblies, and flat sections of twisted flat constructions.

When the frequency of the signal is a small integral multiple of the inverse propagation time between the structures, resonant effects may occur. Since resonant effects allow the addition of responses from many signal periods the intensity of the effect may be much larger than in any one signal period alone. Comb filters are one common example of purposefully introduced periodic structures. These filters produce sharp pass and stop bands.

The intensity of the resonant effect is related to the degree of the disturbance and to the losses in the interconnect. The overall length of the interconnect assembly may also be important.

Swept frequency measurements are critical to determine the intensity, the center frequency and the resonant peak width for both bulk cable and interconnect assemblies.

Single pulse time domain measurements may not reveal key behaviors caused by periodic structures.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

Annex C
(informative)

SCSI signal driver boards (SSDB)

This annex describes the reasons for having a SCSI signal driver board, SSDB, and its desirable properties.

SCSI drivers are different from those available on present test instrumentation (due to issues such as fall back and slew rate control). Eye diagrams and differential to common mode conversion measurements on interconnect assemblies need to have all signals active in order to emulate the cross talk of a real application. When using a functional SCSI device full support of the SCSI protocol is required to achieve data phase activity. SCSI protocol contains many phases other than the data phase. Transmissions during these non-data phases produce signals that can increase the difficulty of capturing signal integrity diagram data in the data phase only. It is also desirable to have direct control over the serial data patterns that are driven by each signal driver so that a translation is not needed between the parallel data defined by SCSI protocol and the serial data stream needed on the signal.

Hardware to create the specified driver signals on all lines at the same time is desirable. This hardware is called a SCSI signal driver board or SSDB.

Desirable properties of an SSDB include:

a) Capable of up to Ultra640 data rates
b) Support for Ultra640, Ultra320, Ultra160, and Ultra2 LVD applications as native on the board.
c) Contains a programmable JTAG interface with a serial interface to a standard personal computer
d) Has either an SCA-2 or a VHDCI connector to enable attachment of passive SCSI interconnect - connector adapters are required if other connector types are needed
e) Has an external timing input to enable non-standard speeds to be used from an external timing source
f) Has an external inputs for the serial data patterns from a pattern generator e.g., PRBS
g) Ability to control the cutback levels, rise times, and signal amplitudes (all signals may change together - separate control of each signal is not required)
h) Software (both binary object and source code) that allows the user to control the SSDB
i) Standard four pin 5v power connector - a 5V / 1 amp external source
j) Coaxial connector for the JTAG mounted on the SSDB

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

Annex D
(informative)

Mirage effects in multi-drop subassembly TDR impedance measurement

D.1 Overview

The annex concerns TDR measurement of multi-drop bulk cable and extends to unpopulated backplanes. Multi-drop bulk cable presents measurement and specification problems. Such cable generally consists of sections composed of twisted pairs interspersed with transition regions, generally flat sections, intended for connector attachment. A typical representation is depicted in figure D.1.

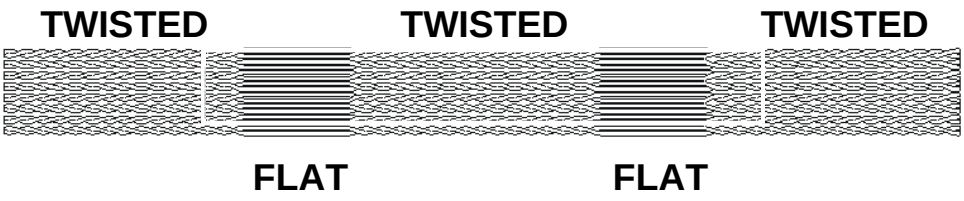


Figure D.1 - Typical multi-drop cable

For simplicity, the terms “twisted region” and “flat region” are used in this annex instead of "uniform" and "transition".

The flat region impedance, before connectors and loads are attached, is usually higher than the twisted region impedance. However, after connectors and loads are attached, the impedance of the combined flat, connector, and load is usually much lower than the twisted region impedance. The higher impedance of the flat region helps to compensate for the severe effects of loads.

Ideally, both regions could be measured to characterize a multi-drop bulk cable.

It is difficult to accurately measure the impedance in the flat region. The twisted region impedance is easy to measure on long twist sections but difficult on commonly used short sections.

D.2 Mirages

The flat poses special problems because it is physically short. Measurement fixtures cause aberrations and reflections near the launch point. Transitions from twist-to-flat and from flat-to-twist cause additional multiple reflections which obscure the features of interest. The flat is sometimes “lost” in the reflections as depicted in figure D.2. The actual location of the flat is determined by finger-pinching the beginning and end of the flat at shown in the lower two traces. Observe that the flat is completely lost in the upper trace.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

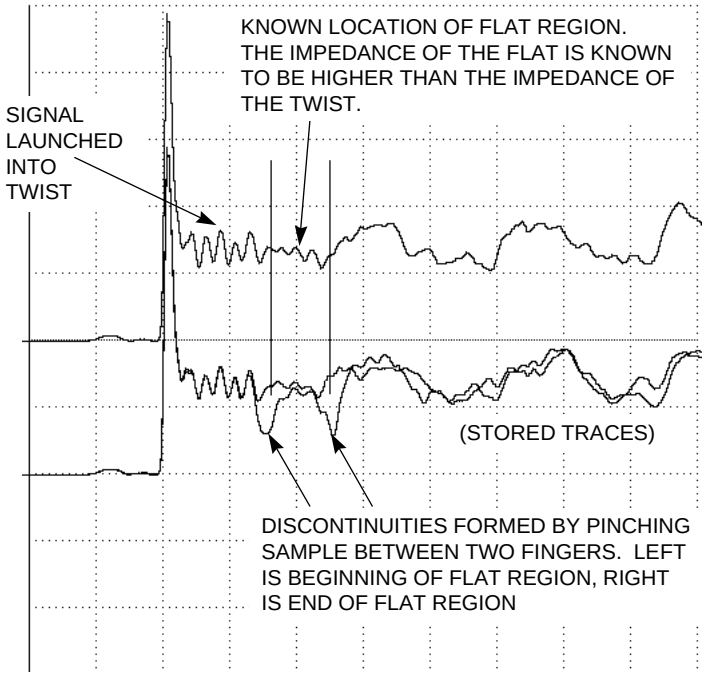


Figure D.2 - Mirage – missing flat

Figure D.2 shows that TDR readings may not be trustworthy for flats measured near the fixture. The impedance in the flat region is known to be significantly higher than for the twisted region. However, in figure D.2 on the lower trace the beginning and end of the flat region are indicated by discontinuities caused by pinching the flat region. In the upper trace there is no indication of the known higher impedance of the flat region. The display significantly misrepresents the actual impedance of the flat. This effect is termed "mirage" in this annex for convenience.

The response from a different sample shown in Figure D.3 shows that readings taken further into the cable may also not be trustworthy. In this case the peak impedance of the flat appears well before its actual location (again indicated by the finger-pinch method). Examples that have worse mirages are common .

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

.

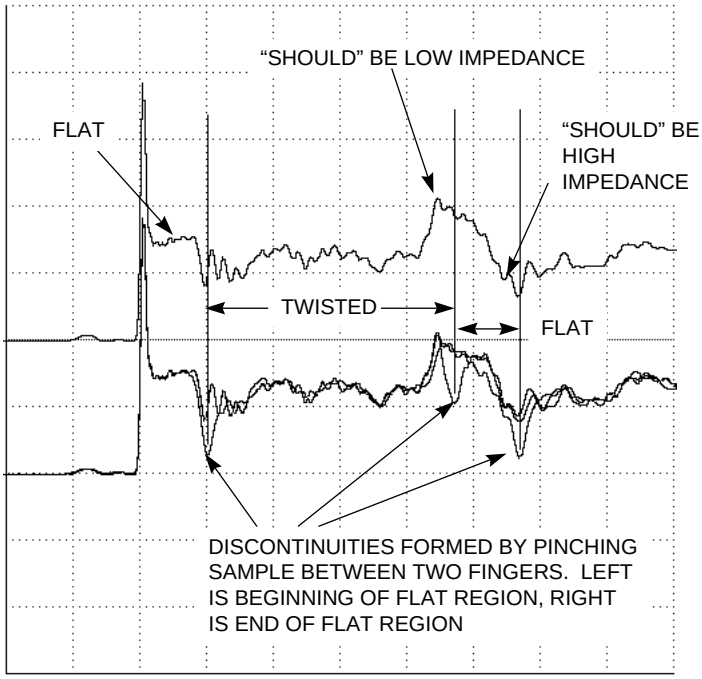


Figure D.3 - Mirage – obscured flat

Filtering the data does not remove the mirages, as shown in figure D.4. The impedance of the flat region is higher than that of the twist region.

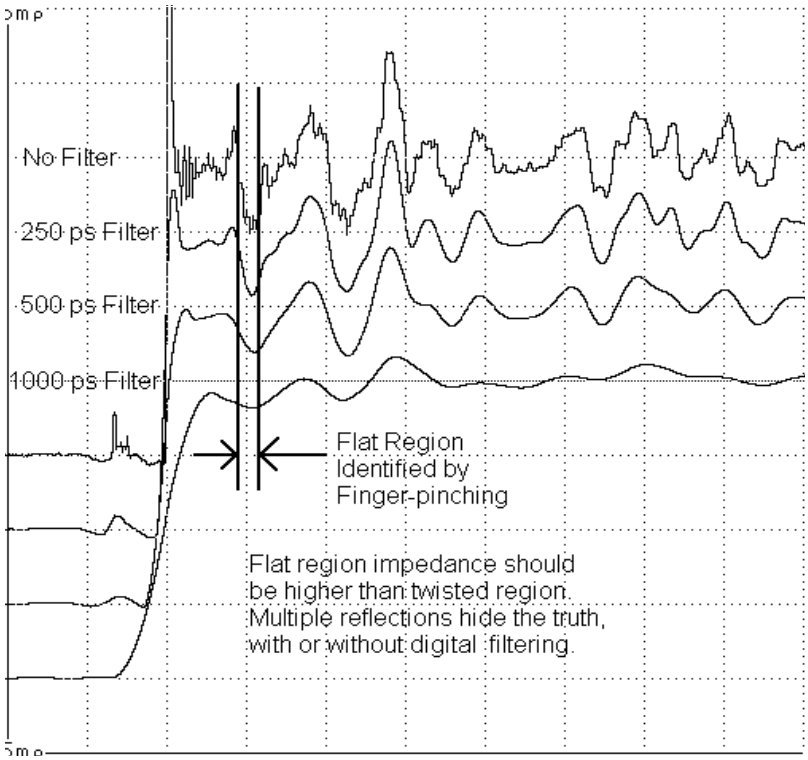


Figure D.4 - Filtered traces

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS
Not for Resale

D.3 Average impedance

Impedance averaged over the entire sample is frequently requested by users. This presents additional problems. Assuming the twisted region has different impedance than the flat region, the “average” impedance depends on the spacing of the twists and flats. For example, a cable having no flats (flats at infinite intervals) might measure 120 Ω. Another cable, having no twisted section (flats at zero intervals) might measure 135 Ω.

For this example, the “average” impedance would be near 120 Ω when transition regions are separated by a large distance, while the “average” impedance would be nearer to 135 Ω if the transition regions are very close.

The “average” impedance problem is even worse when we consider the case of a multi-drop cable having transition regions that are not equally separated. Consider the cases illustrated in figure D.5. The “average” impedance measured from Z1 is not equal to the “average” impedance from Z2 when measurements do not include the entire sample length.

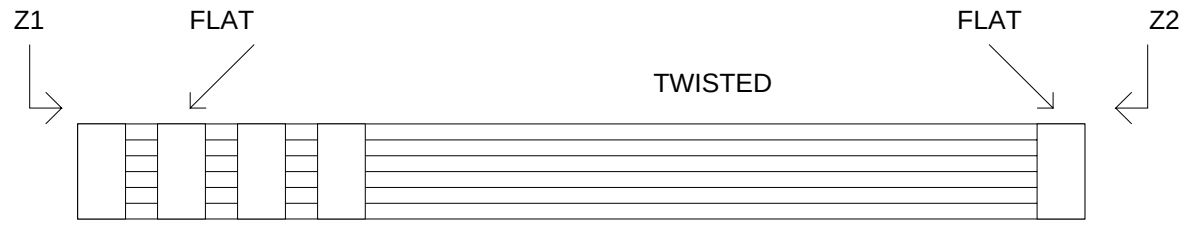


Figure D.5 - Average impedance conundrum

D.4 Recommendations:

D.4.1 Overview

Measurement ambiguities disqualify twist impedance and flat impedance as primary specifications. However, such measurements may be useful for analysis. Multi-drop cables permit infinite variations in design. Flats may be long or short, twist sections may be long or short, intervals between flats may be any length, intervals may be periodic or non-periodic.

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS Not for Resale

D.4.2 Fixture

Reflections from the test equipment may be minimized by using a longer than normal test fixture. The fixture shown in figure D.6 uses 250 mm of semi-rigid coax for each of the signals (instead of the 75 mm normally used).

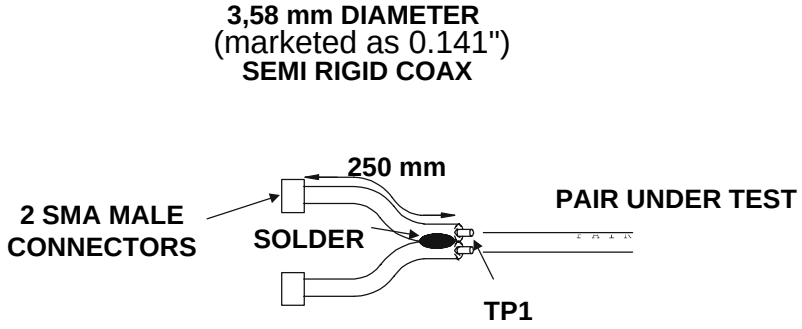


Figure D.6 - Long test fixture

D.4.3 Twisted region

To evaluate the properties of the twisted region measure the longest practical sample cut from a multi-drop sample. If evaluating a sample having very short twist regions, consider measuring the twist impedance of a very similar sample having a much longer twist region. It may be possible to procure a sample that is all twisted, i.e., having no flats.

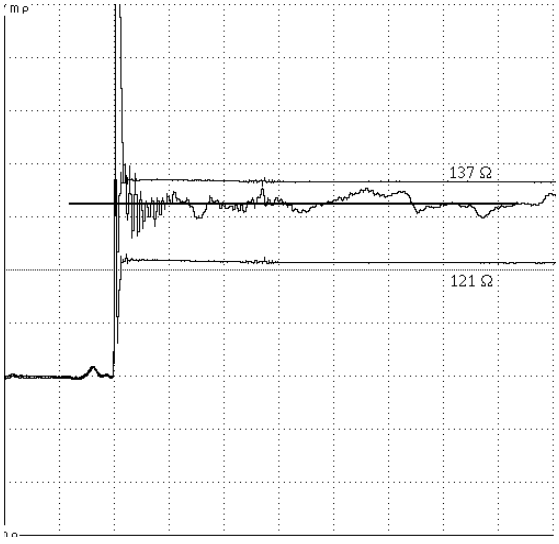


Figure D.7 - Long twist, no flats

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS
Not for Resale

When only very short twists are available for measurement, it is useful to attach known value high-frequency chip resistors to the far end of the sample to provide known reference points as shown in figure D.8.

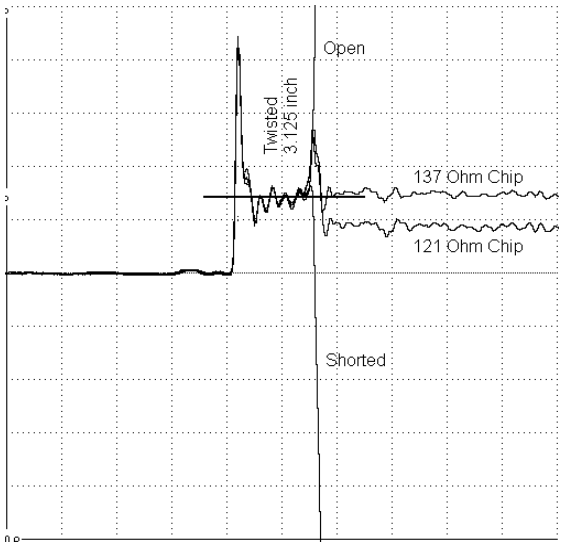


Figure D.8 - Short twist into various loads

D.4.4 Flat region

To evaluate the properties of the flat region measure the longest practical sample cut from a multi-drop sample. If evaluating a sample having very short flat regions, consider measuring the flat impedance of a very similar sample having somewhat longer flat. It is useful to attach known value high-frequency chip resistors to the far end of the sample to provide known reference points, as was shown above in figure D.9.



Figure D.9 - Flat

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS
Not for Resale

Bibliography

INCITS/TR-29:2002, SCSI Signal Modeling (SSM)

SFF-8451 - Specification for SCA-2 unshielded connections

SFF-8410 - Testing and performance requirements for high speed serial and parallel - serial copper links

SFF-8415 - Specification for Measurement Methodology Requirements for High Performance Electrical Interconnect-HPEI

Copyright International Organization for Standardization
Provided by IHS under license with ISO
No reproduction or networking permitted without license from IHS
Not for Resale