INTERNATIONAL STANDARD

ISO/IEC 9314-21

First edition
2000-10

Information technology – Fibre Distributed Data Interface (FDDI) –

Part 21: Abstract test suite for FDDI physical layer protocol conformance testing (PHY ATS)

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INFORMATION TECHNOLOGY –
FIBRE DISTRIBUTED DATA INTERFACE (FDDI) –
Part 21: Abstract test suite for FDDI physical layer protocol conformance testing (PHY ATS)

FOREWORD

1) ISO (International Organization for Standardization) and IEC (International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work.
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International Standard ISO/IEC 9314-21 was prepared by subcommittee 25: Interconnection of information technology equipment, of ISO/IEC joint technical committee 1: Information technology.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 3.

ISO/IEC 9314 consists of the following parts, under the general title *Information technology – Fibre distributed Data Interface (FDDI):*

Part 1: Token Ring Physical Layer Protocol (PHY)

Part 2: Token Ring Media Access control (MAC)

Part 3: Physical Layer Medium Dependent (PMD)

Part 4: Single-mode Fibre Physical Layer Medium Dependent (SMF-PMD)

Part 5: Hybrid Ring Control (HRC)

Part 6: Station Management (SMT)

Part 7: Physical Layer Protocol (PHY-2)

Part 8: Media Access Control-2 (MAC-2)

Part 9: Low-cost Fibre Physical Layer Medium Dependent (LCF-PMD)

Part 13: Conformance Test Protocol Implementation – Conformance Statement (CT-PICS) Proforma

Part 20: Abstract Test Suite for FDDI Physical Medium Dependent Conformance Testing (PMD-ATS)[1)]

Part 21: Abstract Test Suite for FDDI Physical Layer Protocol Conformance Testing

Part 25: Abstract Test Suite for FDDI – Station Management Conformance Testing (SMT-ATS)

Part 26: Media Access Control conformance Testing (MAC-ATS) (under consideration)

1) To be published.

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INTRODUCTION

The Fibre Distributed Data Interface (FDDI) is intended for use in a high performance general purpose multi-station network and is designed for efficient operation with a peak data rate of 100 Mbit/s. It uses a Token Ring Architecture with optical fibre as the transmission medium. FDDI provides for hundreds of stations operating over an extent of tens of kilometres.

FDDI Physical Layer Protocol (PHY) specifies the upper sublayer of the Physical Layer for the FDDI, including the data encode/decode, framing and clocking, as well as the elasticity buffer, smoothing and repeat filter functions. This Abstract Test Suite (ATS) provides a conformance test for FDDI PHY. FDDI PHY, however, does contain several state machines and implements a protocol at the level of FDDI code symbols. The only physical quantity that must be measured in this conformance test is frequency. The PHY ATS cannot use the Tree and Tabular Combined Notation (TTCN) language specified in ISO 7496 and a notation is developed in the PHY ATS for specifying test patterns and expected results in terms of FDDI code symbol strings.

Four other standards in conjunction with this standard provide a complete conformance test of an FDDI station:

a) An ATS for FDDI Physical Medium Dependent (PMD) that provides a conformance test for FDDI PMD. PMD specifies the optical interface of FDDI stations. PMD is not a protocol standard and this ATS requires the measurement of physical quantities such as optical power, wavelength and signal jitter. The PMD ATS differs from the methodology of higher level protocol conformance tests written using the TTCN, because the TTCN notation does not provide a suitable vehicle for Physical Layer testing, where there is no concept of a protocol data unit and where physical quantities must be measured.

b) An ATS for FDDI Media Access Control (MAC) that provides a conformance test for FDDI MAC. MAC specifies the lower sublayer of the Data Link Layer for FDDI. It specifies access to the medium, including addressing, data checking and data framing. MAC also specifies the receiver and transmitter state machines. Since MAC is a protocol that deals primarily with complete PDUs, the TTCN language is used to specify MAC protocol tests. Provisions of MAC, however, require high resolution timing that may be difficult to achieve in commercial protocol testers.

c) An ATS for FDDI Station Management (SMT) that provides a conformance test for FDDI SMT. SMT specifies the local portion of the system management application process for FDDI, including the control required for proper operation of an FDDI station in an FDDI ring. SMT provides services such as connection management, station insertion and removal station initialisation, configuration management and fault recovery, communications protocol for external authority, scheduling policies and the collection of statistics. SMT interacts with PMD, PHY and MAC. Therefore, an ATS for portions of SMT that use MAC PDUs can be specified in TTCN, while other portions require other approaches.

d) A Protocol Implementation Conformance Statement (PICS) proforma for FDDI that provides a statement of the mandatory and optional requirements of each of the four FDDI base standards. The PICS proforma is used to identify requirements for conformance testing and to specify optional functionality requirements, particularly by workshops for functional standards and profiles.

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INFORMATION TECHNOLOGY –
FIBRE DISTRIBUTED DATA INTERFACE (FDDI) –
Part 21: Abstract test suite for FDDI physical layer protocol conformance testing (PHY ATS)

1 Scope

This part of ISO/IEC 9314 defines a conformance test of the PHY functions in a path through an FDDI node. Figure 1 is a functional block diagram of an FDDI path. The path contains the necessary functions to repeat (that is decode and retransmit) frames through an FDDI node.

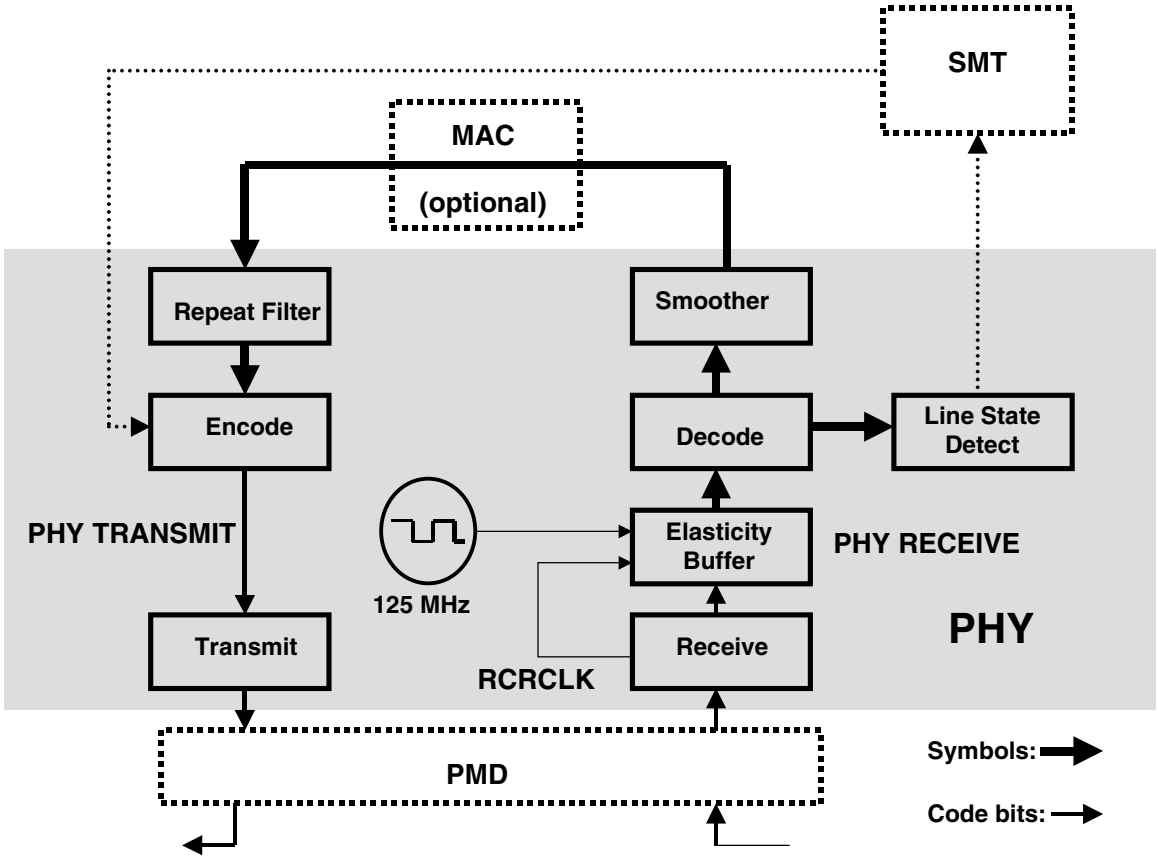

Figure 1 – FDDI Repeat Path and PHY Functions

The PHY Repeat Filter is optional when there is a MAC in the repeat path. If there is no MAC in the repeat path, then the function is implemented in PHY. This test standard makes no assumption about the presence or absence of MAC on the path and is intended to operate with or without a MAC. It tests the repeat filter function wherever it is located. However, the results of some tests may be slightly different if a MAC is present.

2 Conformance

This part of ISO/IEC 9314 defines a conformance test of the PHY functions in a path through an FDDI node.

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3 Normative references

The following standards contain provisions which, through reference in the text, constitute provisions of this part of ISO/IEC 9314. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this part of ISO/IEC 9314 are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies. Members of IEC and ISO maintain registers of currently valid International Standards.

ISO 9314-1:1989, *Information processing systems – Fibre Distributed Data Interface (FDDI) – Part 1: Token Ring Physical Layer Protocol (PHY)*

ISO 9314-2:1989, *Information processing systems – Fibre Distributed Data Interface (FDDI) – Part 2: Token Ring Media Access Control (MAC)*

ISO/IEC 9314-3:1990, *Information processing systems – Fibre Distributed Data Interface (FDDI) – Part 3: Physical Layer Medium Dependent (PMD)*

ISO/IEC 9314-6:1998, *Information technology – Fibre Distributed Data Interface (FDDI) – Part 6: Token Ring Station Management (SMT)*

4 Definitions and conventions

For the purposes of this part of ISO/IEC 9314, the definitions given in ISO 9314-1, ISO 9314-2, ISO/IEC 9314-3 and ISO/IEC 9314-6 apply.

The terms SMT, MAC, PHY and PMD, when set in roman type and used without modifiers, refer specifically to the local entities. When set in italic type they refer to the corresponding standard listed in clause 3.

5 Symbols and abbreviated terms

The following acronyms and abbreviations are used in this test specification:

AC	Alternating Current
ALS	Active Line State (PHY)
CMT	Configuration Management (SMT)
DC	Direct Current
FCS	Frame Check Sequence
FDDI	Fiber Distributed Data Interface
HLS	Halt Line State (PHY)
ILS	Idle Line State (PHY)
IUT	Implementation Under Test
MIC	Media Interface Connector (PMD)
MLS	Master Line State (PHY)
NLS	Noise Line State (PHY)
NRZI	Non-Return to Zero Inverted (PHY)
PCM	Physical Connection Management (SMT)
PHY	Physical Layer Protocol (PHY)
PMD	Physical Medium Dependent Layer (PMD)
PTA	PHY Test Apparatus
QLS	Quiet Line State (PHY)
RMT	Ring Management (SMT)
SD	Starting Delimiter (MAC)
SMT	Station Management (SMT)
SR	Symbol Recorder
SSG	Symbol Sequence Generator
TRT	Token Rotation Timer (MAC)

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6 Specification breakdown

Table 1 summarizes the requirements of PHY and identifies the specific test suite where requirements are tested. Certain requirements of the PHY standard (primarily the recognition of line states) are indirectly verified in the Station Management (SMT) Physical Configuration Management (PCM) verification test, because their effects are most directly manifest as a result of actions taken by PCM. Every PHY is controlled by an SMT entity, and the test of PCM provides the best test possible of these PHY requirements.

Table 1 – Specification breakdown

Item Name	PICS Item No.	PHY Ref.	Test Reference
Line State Detection and Transmission			
Quiet (Tx/Rx)	PHY 1.1	7.3.1	SMT PCM Test
Master (Tx/Rx)	PHY 1.2	7.3.2	SMT PCM Test
Halt (Tx/Rx)	PHY 1.3	7.3.2	SMT PCM Test
Idle (Tx/Rx)	PHY 1.4	7.3.4	8.4 & SMT PCM Test
Active (Tx/Rx)	PHY 1.5	7.4.5	8.4
Noise (Tx/Rx)	PHY 1.6	7.3.6	SMT PCM Test
Violation symbol / invalid code	PHY 1.7	7.2.4	8.8.4.3
Elasticity Buffer Functions			
Insertion of code bit ones	PHY 2.1	8.2.4	8.5
Deletion of code bit ones	PHY 2.2	8.2.4	8.5
Receive frame with RCRCLK = 125,000 MHz (–0,005 %)	PHY 2.3	8.2.4	8.5
Receive frame with RCRCLK = 125,000 MHz (+0,005 %)	PHY 2.4	8.2.4	8.5
Realignment of JK with ALS	PHY 2.5	8.2.4	not tested
Smoothing Function			
Reclaim fragments of stripped partials	PHY 3.1	8.3	not tested
Reclaim space from other partial frames	PHY 3.2	8.3	not tested
Insert Idles	PHY 3.3	8.3	8.6
Delete Idles	PHY 3.4	8.3	8.6
Repeat Filter Functions			
Symbol following I changed to I until JK	PHY 4.1	8.4	8.8.4.1
Detect Violation symbol (isolated J)	PHY 4.2	8.4	8.8.4.2
SD in ALS	PHY 4.3	8.4	
Replace invalid symbol with HHHH	PHY 4.4	8.4	8.8.4.3
Parameters			
SC_Max (ns)	PHY 5.1	8.5.2	8.7
Lcl-Clk Reew (MHz)	PHY 5.2	8.2.7	7
Phase jitter (deg)	PHY 5.3	8.2.7	not tested
Harmonic content (dB)	PHY 5.4	8.2.7	not tested
Path Latency			
Minimum latency with no MAC in path	PHY 6.1	8.5.1	8.7
Minimum latency with MAC in path	PHY 6.2	8.5.1	8.7

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7 General

7.1 Path establishment

This ATS is a conformance test of an FDDI PHY path. Figure 1 is a functional block diagram of an FDDI path. There is always at least one path through an FDDI node; there may be a MAC entity on a path and there is always a PHY receiver and a PHY transmitter. In the case of concentrators more than one PHY entity may be concatenated on one repeating path.

To test an FDDI PHY path it is first necessary to initialize at least one port and establish a path through the node. An FDDI node has one or more ports. A port consists of a PMD entity and an associated PHY entity. The input and output of a port use the same Media Interface Connector (MIC). A path is distinct from a PHY entity. A path may enter on the input of one port and its associated PHY entity receiver function and exit on the output of that same port and PHY entity transmitter function, or it can exit on the output of another port and its associated PHY entity transmitter function.

After the input enters through the connector input the signal level is interpreted by the PMD Receiver entity, which continually makes a decision about whether each received code bit signal level is a one or a zero. The PMD Receiver then passes the code bit stream onto the PHY Receive entity, which recovers the clock of the received signal. It then uses the recovered clock to determine whether a level transition has occurred in each code bit interval; in the NRZI code used by FDDI a transition is a code bit one and no transition is a code bit zero. PHY then aligns groups of five code bits into symbols, and decodes those symbols into one of 16 data values, eight control values or eight invalid values. A special unique symbol pair, called JK, is used to establish the symbol alignment and mark the start of a frame. The data symbols are reclocked from a local oscillator, and two FIFOs, called the Elasticity Buffer and Smoother provide compensation for the difference between the local oscillator and the recovered clock. PHY also determines input lines states for the SMT entity.

Input symbols are then passed to an optional MAC entity, which either repeats input frames or strips them. MAC may also originate new frames while stripping any received frames. During normal operation, when MAC is not repeating or originating frames it sources Idle symbols.

The PHY transmit function either repeats packets passed to it by the PHY receiver (through the MAC entity when a MAC is present on the path), transmits frames originated by the local MAC, or sends Idle symbols. If no MAC is present on a path a PHY Repeat Filter detects and corrects certain invalid input symbols. The Repeat Filter is optional if there is a MAC. The sixteen possible data values and eight possible control values are then encoded in the FDDI NRZI line code and passed to the PMD transmitter as a serial bit stream. This standard tests the PHY functions of a path as shown in Figure 1.

Any FDDI dual attachment node has at least 4 possible paths, some which enter and exit through the same port and others which enter at the input of one port and exit at the output of another port. Concentrators, in general, have more than four possible paths.

This ATS specifies a conformance test for any PHY path through a node. Figure 2 illustrates the four paths through a dual attachment station in three of its configuration states. A dual attachment station has two ports, one labeled A and the other B. In the THRU state (Figure 2 a)) each path enters through one port (and its PHY receiver entity) and exits through another port (and its PHY transmitter entity). In the WRAP B state (Figure 2 b)) a path enters and exits through the B port, while the A port is not active. In the WRAP A state (Figure 2 c)) a path enters and exits through the A port, while the B port is not active. It may be more convenient to test paths that enter and exit through the same port, because it is only necessary to initialize one link, while it is necessary to initialize two links before beginning the PHY test when the path tested enters one port and exits another.

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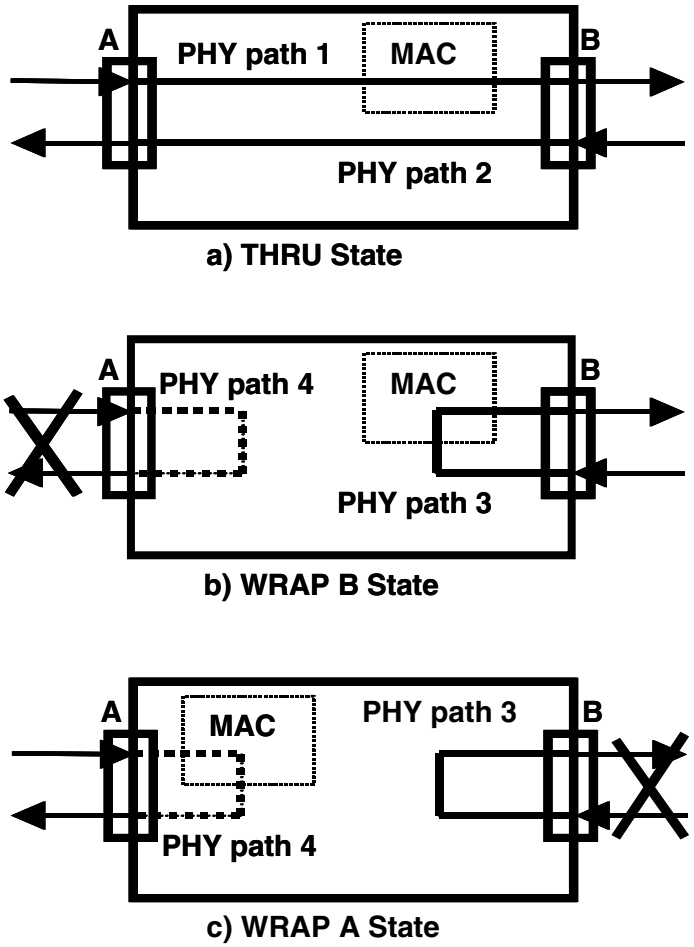

Figure 2 – Paths in a Dual attachment station

7.2 Test environment

The FDDI standards do not specify an operating environment. All tests specified in this document shall be performed with temperature, and atmospheric conditions consistent with the environmental operating specifications of the IUT.

For FDDI stations which are directly powered (either wholly or partly) from the AC power line, all tests shall be carried out within 5 % of the nominal operating voltage. If the equipment is powered by other means and those means are not supplied as a part of the apparatus (e.g. batteries, stabilized AC supplies, DC) all tests shall be carried out within the power supply limit declared by the supplier. If the power supply is AC, the tests shall be conducted within 4 % of the normal operating frequency.

7.3 Measurement error

Physical quantities are measured in this standard (particularly time and frequency). There are measurement errors associated with the calibration and tolerance of the measurement instruments. It is the burden of the conformance test laboratory to verify that an IUT does conform to the standard. Therefore these measurement errors are added to the requirement being tested so that the greater the error, the more difficult it becomes to pass the conformance test.

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8 Internal clock test

8.1 Purpose

A PHY transmits under control of a local clock. The maximum allowed frequency is 125,006 25 MHz and the minimum is 124,993 75 MHz. Note that, although the local clock is specified as a 125 MHz clock, implementations may use other crystal frequencies with appropriate circuits to generate the needed time base. A code bit is transmitted every 8 ns and the idle pattern output (a code bit one or an NRZI signal transition every 8 ns) is a 62,5 MHz square wave. This test measures accuracy of the local clock.

8.2 Equipment

The following equipment is required:

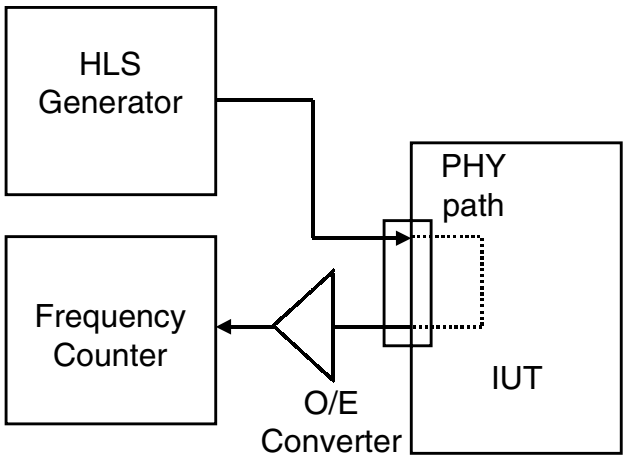

Figure 3 – Internal clock test set-up

HLS Generator. This apparatus generates Halt Line State (HLS). Any conforming FDDI station can serve as an HLS generator.
Optical/Electrical converter.
Frequency Counter.

8.3 Configuration

See Figure 3.

8.4 Procedure

The HLS Generator causes the PHY under test to transmit Idle Line State (ILS). ILS is a 62,5 MHz (nominal) square wave, driven by the node's local clock. The frequency counter measures the precise frequency of the signal.

8.5 Pass_fail criteria.

Let e be the measurement uncertainty due to the accuracy of the Frequency Counter. The IUT passes this test if the output signal is in the range (62,496 875 + e) MHz to (62,503 125 – e) MHz.

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9 Repeating tests

The test suites in this clause all test the ability of a PHY in an active link to correctly repeat a symbol stream under various conditions, including errors. In general, a PHY is required to repeat any sequence of up to 9 000 symbols beginning with JK and continuing until an I, V, Q, K or H symbol, or a J symbol not followed by a K symbol is received. When V, H, K or Q symbols are received, they are not repeated but are transformed according to certain rules by the Repeat Filter. When a PHY is not repeating a symbol sequence beginning with JK, it is sourcing I's.

This standard defines a sequence of tests to be performed to verify the conformance of a PHY entity on a repeat path. When the tests begin, the repeat path is already active. For a repeat path to be active the link on the path's entry and exit ports must be initialized. The link initialization process is defined in the Physical Connection Management (PCM) function of the Station Management (SMT) standard. This standard assumes that initialized links have been established between a PHY Test Apparatus and the PHY path to be tested, as necessary. This standard does not describe the process for initializing those links.

The normal operation of paths containing FDDI MACs is complex; in general it is necessary to maintain an active FDDI token ring to keep a path open indefinitely if that path contains a MAC. This standard does not attempt to define the tester functionality necessary to maintain operation of the token ring.

This standard frequently uses a special frame, the Beacon frame, to simplify the tests and bypass the normal token ring logic. A MAC which receives a Beacon frame ordinarily repeats that frame (unless it was the source of the Beacon frame), even if it is in the Beacon or Claim process when the Beacon is received. Note that the test sequences given in this standard do not necessarily satisfy the long term requirements of MAC since no token is sent to restart the TRT. The specified test sequences can be sent immediately after a path is created by initializing one or two ports and before the token ring is operational, or, if there is a MAC in the IUT path, after a token ring is initialized and operational. The effect of running any of these test sequences will be to interrupt ring operation, and, if the test sequence is repeated indefinitely and there is a MAC in the path, then the IUT MAC will eventually attempt to generate its own Beacon.

9.1 General Test Set-up

9.1.1 Equipment

The PHY Test Apparatus (PTA) required for most of the following tests of PHY conceptually consists of two separable functions, a Symbol Sequence Generator (SSG) and a Symbol Recorder (SR):

The SSG is capable of generating test sequences consisting of multiple repetitions of specified FDDI 5-bit code symbol patterns. The SSG outputs symbols under control of a clock within the tolerance specified in PMD. Additionally, it shall either make provision to output data under control of an external clock or contain internal clocks conforming to the requirements of 7.5.4. The SSG shall generate a Start signal to notify the SR to start recording.

The SR records a sequence of code symbols in response to a Start signal from the SSG. While awaiting the Start signal it recovers the bit clock from the IUT and maintains symbol alignment by aligning on starting delimiters. For every test except the path delay test (see 9.7) and the clock recovery and elasticity buffer test (see 9.5) the SR may optionally begin recording at the first starting delimiter (JK symbol pair) following the Start signal, so that data is recorded with symbol alignment. Data recorded may be processed off-line and compared to the expected values given in the Pass_fail criteria clause of each test to verify conformance. While it is expected that it will be more convenient to first capture output data then process it

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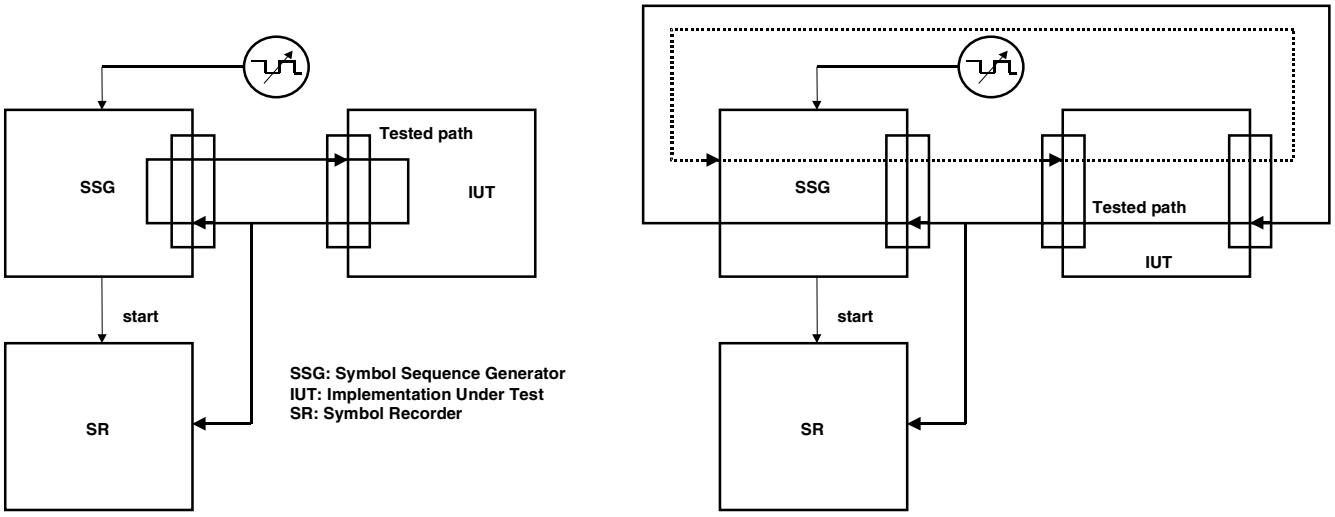
off line for verification, there is no intention to prohibit the use of an apparatus able to verify the output on line in real time.

In addition to the SSG and SR functions defined above, the PTA must include a means for initializing connections necessary to establish the repeat path which is to be tested in the IUT.

9.1.2 Test Configuration

See Figure 4. Two configurations are shown. Figure 4 a) shows the configuration to test a path which exits and enters through the same port. Figure 4 b) shows the configuration to test a path in a dual attachment station which is in the THRU configuration state. In this case the path enters through one port and exits from another. In addition to the two cases shown in Figure 4, a very large number of possible paths exist in concentrators.



a) Path enters and exits same port

b) Path enters and exits different port

Figure 4 – Configuration for repeating tests

9.2 Code symbols and line states

PHY defines a 4 of 5 bit code with symbols for 16 possible data values. The notation used for each 5 bit FDDI code symbol is defined in Table 2. This notation differs from the corresponding table in PHY only in that each of the eight Violation symbols is separately identified as V1, V2... in Table 2.

Eight out-of-band symbols are defined, which are used in the PHY and MAC levels to provide such functions as packet framing and the maintenance of clock synchronization during intervals between frames. Eight code violations are defined.

In addition, seven line states are defined in PHY. A PHY entity detects the current line state, based on the active input, and indicates the current line state to SMT. PHY determines the current line state from the PMD Signal_Detect indication and the input symbol stream.

The full ability of PHY to decode input symbols and detect line states can only be inferred indirectly from the tests of the operation of MAC, SMT and the PHY smoothing buffer, PHY elasticity buffer and PHY repeat filter. The verification of PHY conformance is simply the ability to pass the SMT, MAC and other PHY tests. Note that it is not necessarily possible to ascribe the failure of one of these tests to PHY, SMT or MAC. Wherever there is a PHY it is controlled by an SMT entity, however, there may not be a MAC associated with either the PHY or SMT.

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Table 2 – FDDI code symbol notation

Binary Value	Notation	Assignment	Binary Value	Notation	Assignment
00000	Q	Quiet	10000	V_8	Violation
00001	V_1	Violation	10001	K	Second symbol of JK pair
00010	V_2	Violation	10010	8	Data
00011	V_3	Violation	10011	9	Data
00100	H	Halt	10100	2	Data
00101	V_4	Violation	10101	3	Data
00110	V_5	Violation	10110	A	Data
00111	R	Reset	10111	B	Data
01000	V_6	Violation	11000	J	First symbol of JK pair
01001	1	Data	11001	S	Set
01010	4	Data	11010	C	Data
01011	5	Data	11011	D	Data
01100	V_7	Violation	11100	E	Data
01101	T	Ending Delimiter	11101	F	Data
01110	6	Data	11110	0	Data
01111	7	Data	11111	I	Idle

9.3 Symbol Sequence Notation

This clause defines the notation used in this standard to define sequences of 5 bit FDDI code symbols for tests.

The left bracket ,"[", is used to indicate the Starting Delimiter (JK pair) and to cause the FCS computation to begin following the JK. A right bracket, "]", is used to indicate an eight symbol FCS, computed on the data values of the symbols following a Starting Delimiter, followed by a T Symbol. An FDDI MAC packet may be indicated by “[xxxx...x]XXX”, where “x” may be any data symbol, 0 through F, while "X" is either the R symbol or the S symbol. Thus "[0123456789ABCDEFFFFF]RRR" is equivalent to “JK0123456789ABCDEFFFFFyyyyyyyyTRRR”, where “yyyyyyyy” is the data symbols whose value is the FDDI Frame Check Sequence for “0123456789ABCDEFFFFF”.

A number, n, enclosed in braces “{n}” means that the following symbol is repeated n times, For example “{7}I” is equivalent to IIIIIII. If the number enclosed in parentheses is preceded by a greater than ,">>", then it indicates more than that number of symbols. For example “{>>5}I” indicates six or more I symbols.

A bold face number enclosed in parentheses followed immediately by a symbol string enclosed in parentheses means that number of repetitions of the symbols. For example, “{3}(JKIV2)” is equivalent to “JKIV2JKIV2JKIV2”.

An expression of the form “{a:b}”, where a and b are integer numbers means at least a and not more than b. For example, {2:4}(JKT) is equivalent to “JKTJKT” or “JKTJKTJKT” or “JKTJKTJKTJKT”.

A lower case “x” is used to indicate any valid data symbol 0 through F. A lower case “v” is used to indicate any one of the 8 violation symbols. An upper case “Vn” is used to indicate all eight violation symbols, taken one at a time, and when used generates eight separate symbol sequences. For example “JKVnF” means the eight separate symbol sequences: “JKV1F”, “JKV2F”, ..., “JKV8F”. In other words, it means to repeat the sequence 8 times with each of the violation values; in most cases the expected output sequence from the IUT should be the same whichever violation symbol is used.

A“^” is used to represent the point at which the SSG generates a start signal and the SR then begins recording. The assertion of the start signal is simultaneous with the start of transmission of the next indicated symbol. A sequence of three periods, “...”, is used to indicate that subsequent recorded symbols are not considered in determining the test results.

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9.4 Symbol repetition test

9.4.1 Purpose

This test verifies that a PHY port can repeat all sixteen data symbols when they follow JK, as well as the T, S and R symbols. It does not require the presence of a MAC in the repeat path, however, it will function with a MAC in the path. Detection of invalid symbols is tested in 9.8.4.3.

9.4.2 Equipment

A PTA is required. See 9.1.1.

9.4.3 Configuration

See 9.1.2.

9.4.4 Procedure

The SSG transmits the following pattern:

{5}({20}I[C200000000000088FF88FF88FF00000000]RSR){24}I^{10}({16}I[C200000000000088FF88FF88FF0123456789ABCDEFFEDCBA9876543210]RSR){100}I

The SR captures the output of the IUT.

9.4.5 Pass_fail criteria

The recorded pattern shall be:

...I{10}({12:28}I[C2000000000000088FF88FF88FF123456789ABCDEFFEDCBA9876543210]RSR)...

9.5 Clock recovery and elasticity buffer

A PHY is required to recover the clock from the input data stream and transmits data using its local clock. The elasticity buffer function inserts or deletes bits (or symbols) in the idle pattern between packets to account for the difference between the two clocks. The elasticity buffer function ensures that a PHY can repeat any valid packet of maximum length or less without alteration, loss or addition of bits or symbols within the packet (except as required by MAC to strip packets or to set the trailing indicators when the MAC recognizes its address).

9.5.1 Purpose

This test verifies that the PHY path can recover the input clock and successfully repeat maximum length packets while the elasticity buffer compensates for the difference between the input clock and the transmit clock by inserting or removing idle bits or symbols in the preambles between frames. The elasticity buffer is required to be able to recenter after a preamble as small as four symbols. This test verifies the clock recovery and elasticity functions.

9.5.2 Equipment

A PTA is required. See 9.1.1.

9.5.3 Configuration

See 9.1.2.

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9.5.4 Procedure

9.5.4.1 High clock frequency

The SSG clock is set to ((twice the frequency measured in 8.4) + 12 500 Hz) ± 0,000 5 % and the SSG transmits the following patterns:

a) Low frequency data pattern;

{5}({20}I[C200000000000088FF88FF88FF00000000]RSR){24}I[C200000000000088FF88FF88FF{4478}(21)]^RSR{4}I[C200000000000088FF88FF88FF{4478}(21)]RSR{100}I

b) DC offset data pattern;

{5}({20}I[C200000000000088FF88FF88FF00000000]RSR){24}I[C200000000000088FF88FF88FF{4478}(77)]^RSR{4}I[C200000000000088FF88FF88FF{4478}(77)]RSR{100}I

c) Repeat up to 9 000 symbols from original entry to ALS while in ALS, including embedded JK, (part 1).

{5}({20}I[C200000000000088FF88FF88FF00000000]RSR){24}I[C200000000000088FF88FF88FF{4478}(21)^]RSR{4}I[80TT

{2}I[C200000000000088FF88FF88FF

{4466}(21)]RSR{100}I

The SR records the output of the IUT.

9.5.4.2 Low clock frequency

The SSG clock is set to ((twice the frequency measured in 8.4) – 12 500 Hz) ± 0,000 5 % and the procedure repeated.

9.5.5 Pass_fail criteria.

The essential criterion for passing all the clock recovery and elasticity buffer tests is that the 9 000 symbols following the start signal (the "^" in the test symbol sequence) of each test symbol sequence are properly repeated. The Idle symbol strings included in the 9 000 symbols may be reduced by up to two symbols or increased by up to 12 additional symbols by the operation of the elasticity and smoothing buffers.

The detailed criteria listed below in 9.5.5.1 and 9.5.5.2 assume that the SR is capable of capturing at least 9 000 symbols. In some cases practical SRs may not be able to record 9 000 symbols. If this is the case and if the path includes a MAC, the SR may be triggered to capture the FCS, Ending Delimiter, and the three Frame Status indicators of the long test frame. A loss of clock synchronism or a failure of the elasticity buffer will cause an FCS error. For the test patterns, the fail criterion is failure to receive TRRR.

For test case (c) the 9 000 symbols includes a token and a long test frame separated by two Idle symbols. In this case it is necessary to verify that both the token and the test frame are repeated. It may be possible to verify correct operation of the IUT by first triggering the SR before the token, as shown above, to verify that the token is repeated correctly, and then, repeating the test sequence, triggering the SR before the end of the long test frame, to verify that the frame is properly repeated.

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9.5.5.1 High clock frequency

The IUT repeats the patterns. The repeated pattern shall be:

a) Low frequency data pattern;

...RSR{2:14}I[C200000000000088FF88FF88FF{4478}(21)]RSRIII...

b) DC offset data pattern;

...RSR{2:14}I[C200000000000088FF88FF88FF{4478}(77)]RSRIII...

c) Repeat up to 9 000 symbols from original entry to ALS while in ALS, including embedded JK.

...RSR{2:14}I[80TT{0:14}I[C200000000000088FF88FF88FF{4466}(21)]RSRIII...

9.5.5.2 Low clock frequency

The IUT repeats the pattern. The results shall be as shown in 9.5.5.1.

9.6 Smoothing buffer

9.6.1 Purpose

Due to the action of the elasticity buffer it is possible that enough idle symbols might be removed from the preamble of a frame to cause a condition where a MAC is not required to be able to copy a frame addressed to it or to actually destroy the frame. This problem would be most severe with maximum length frames. The smoothing buffer function requires a PHY to add at least an idle symbol to short preambles (less than 14 idle symbols) and compensate for this by removing symbols from long preambles (more than 14 idle symbols) as necessary. Implementations might also be two symbols wide, and add or remove two symbols at a time. This test verifies that the short preambles are expanded.

9.6.2 Equipment

A PTA is required. See 9.1.1.

9.6.3 Configuration

See 9.1.2.

9.6.4 Procedure

The SSG transmits the following pattern:

{5}({20}I[C200000000000088FF88FF88FF00000000]RSR)^{10}({10}I[C200000000000088FF88FF88FF77777777]RSR{20}I[C200000000000088FF88FF88FFAAAAAAAA]RSR){100}I

9.6.5 Pass_fail criteria

The recorded pattern shall be:

...{>>10}I[C200000000000088FF88FF88FF77777777]RSR{9}({>>9}I[C200000000000088FF88FF88FF77777777]RSR{<<20}I[C200000000000088FF88FF88FFAAAAAAAA]RSR)...

9.7 Path Delay

9.7.1 Purpose

PHY requires a minimum path delay. This test measures the path delay.

9.7.2 Equipment

A PTA is required. See 9.1.1.

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9.7.3 Configuration

See Figure 4 for the test set-up and Figure 5 for the calibration set-up.

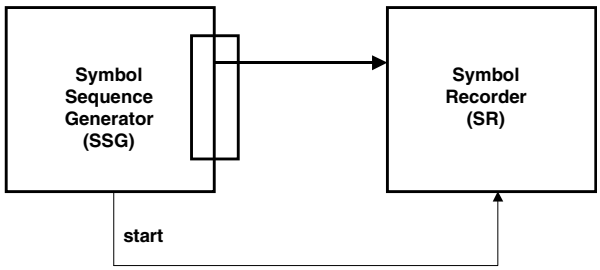

Figure 5 – Delay calibration set-up

9.7.4 Procedure

9.7.4.1 Measurement system delay

The purpose of this procedure is to determine the delay in turning on the recorder. The SSG is connected directly to the SR (see Figure 5). The SSG transmits the following pattern:

(5)({20}I[C200000000000088FF88FF88FF00000000]RSR){50}I[C200000000000088FF88FF88FF0000111122223333444455556666777788889999AAAABBBBCCCCDDDDEEEEFF^FFEEEEDDDDCCCCBBBBAAAA00009999888877776666555544443333222211110000]RSR{100}I

There may be some SR activation delay. Note that it is possible that the SR may have a negative activation delay, that is it may record a few symbols before the start signal is received, depending upon its design. Examine the recorded symbol string to determine the recorder activation delay, a, in symbols. If the recorded pattern is:

FFEEEEDDDDCCCCBBBB....

then activation delay, a, is zero symbols. If the recorded pattern is:

EEEDDDDCCCCBBBBAAAA....

then a is three symbols. If the recorded pattern is:

FFFFEEEEDDDDCCCCBBBB....

then a is minus two symbols.

Connect the IUT to the SSG and SR as shown in Figure 4. The SSG transmits the following pattern:

{5}({20}I[C200000000000088FF88FF88FF00000000]RSR){50}I[C200000000000088FF88FF88FF0000111122223333444455556666777788889999AAAABBBBCCCCDDDDEEEEFF^FFEEEEDDDDCCCCBBBBAAAA00009999888877776666555544443333222211110000]RSR{100}I

The number of symbols recorded before the Start signal is the total delay, d, which includes the SR activation delay. For example, if the recorded symbol string is:

AAABBBBCCCCDDDDEEEEEFF....

then d is 17 symbols.

Compute the IUT path delay as follows:

path delay (symbols) = a + d

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9.7.5 Pass_fail criteria

There are different minimum delay requirements depending upon whether or not there is a MAC in the path and depending on the number of PHY entities in the path. If n is the number of PHY entities in the repeat path, then the IUT passes:

a) if there is a MAC in the repeat path the path delay shall be at least six symbols;

b) if there is not a MAC in the repeat path the path delay shall be at least four symbols.

9.8 Repeat filter

9.8.1 Purpose

The Repeat Filter function prevents the propagation of invalid symbols and line states, permitting accurate error counts to be maintained. The Repeat Filter is required only when PHY is not implemented in-line with MAC. Its use in-line with MAC is allowed but not required, since MAC provides an equivalent function. This test is therefore appropriate for a PHY path whether MAC is in-line or not. If the IUT has PHY paths which do not include an in-line MAC, then this test should at a minimum be run on at least one of the paths without an in-line MAC as well as the path in-line with MAC.

9.8.2 Equipment

A PTA is required. See 9.1.1.

9.8.3 Configuration

See 9.1.2.

9.8.4 Procedure

The SSG transmits test sequences intended to test the separate rules for repeat filter action.

9.8.4.1 Rule 1

Following an I symbol, all subsequent symbols are changed into I symbols until another I or a J symbol is encountered.

a) test in ALS;

{5}({20}I[C200000000000088FF88FF88FF00000000]RSR)^{25}I[C200000000000088FF88FF88FF012345I789ABCDEF]RSR{100}I

b) test I in ALS then JK.

{5}({20}I[C200000000000088FF88FF88FF00000000]RSR)^{25}I[C200000000000088FF88FF88FF012345I789ABC[C200000000000088FF88FF88FF77777777]RSR{100}I

9.8.4.2 Rule 2

If a symbol immediately after a J is not a K, then the J shall be interpreted as a Violation symbol, i. e. changed to an I or H symbol, depending on the current state.

The SSG transmits the following patterns:

a) isolated J;

{5}({20}I[C200000000000088FF88FF88FF00000000]RSR)^{25}I[C200000000000088FF88FF88FF012345J789ABCDEF]RSR{100}I

b) isolated J while sourcing I's.

{5}({20}I[C200000000000088FF88FF88FF00000000]RSR)^{100}IJ{100}I

9.8.4.3 Rule 3

If a K is encountered following a JK sequence, the K is changed to an H; the next three symbols are also changed to H's, but after the fourth H all symbols are changed to I's (until a J or I is encountered). The above is also true when any of the possible H or V symbols or Q symbol is encountered.

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The SSG transmits the following patterns:

a) isolated K in ALS;
{5}({20}I[C200000000000088FF88FF88FF00000000]RSR)^{25}I[C200000000000088FF88FF88FF01K3456789A[C200000000000088FF88FF88FF77777777]RSR{100}I
b) H in ALS;
{5}({20}I[C200000000000088FF88FF88FF00000000]RSR)^{25}I[C200000000000088FF88FF88FF01H3456789A[C200000000000088FF88FF88FF77777777]RSR{100}I
c) Q in ALS;
{5}({20}I[C200000000000088FF88FF88FF00000000]RSR)^{25}I[C200000000000088FF88FF88FF01Q3456789A[C200000000000088FF88FF88FF77777777]RSR{100}I
d) V in ALS.

{5}({20}I[C200000000000088FF88FF88FF00000000]RSR)^{24}I[C200000000000088FF88FF88FFV10000000]RSR){24}I[C200000000000088FF88FF88FFV20000000]RSR){24}I[C200000000000088FF88FF88FFV30000000]RSR){24}I[C200000000000088FF88FF88FFV40000000]RSR){24}I[C200000000000088FF88FF88FFV50000000]RSR){24}I[C200000000000088FF88FF88FFV60000000]RSR){24}I[C200000000000088FF88FF88FFV70000000]RSR){24}I[C200000000000088FF88FF88FFV80000000]RSR){100}I

9.8.5 Pass_fail criteria

The IUT repeats the patterns modified by the repeat filter. The IUT shall pass this test if the repeated patterns captured by the SR are as follows:

9.8.5.1 Rule 1

a) test in ALS;

...JKC200000000000088FF88FF88FF012345IIIIIIIII...

b) test I in ALS then JK.

...JKC200000000000088FF88FF88FF012345{4:13}I[C200000000000088FF88FF88FF77777777]RSRII...

9.8.5.2 Rule 2

a) isolated J;

If there is no MAC in path:

...JKC200000000000088FF88FF88FF012345HHHHIIIII...

or,

...JKC200000000000088FF88FF88FF012345JHHHHIIIII...

or,

...JKC200000000000088FF88FF88FF012345JIIIII...

If there is a MAC in the path:

...JKC200000000000088FF88FF88FF012345IIIII...

b) isolated J while sourcing I's.

...{201}I...

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9.8.5.3 Rule 3

a) Isolated K in ALS;

If there is no MAC in the path then the following is valid:

...JKC200000000000088FF88FF88FF01HHHH{3:15}I...

If there is a MAC in the path:

...JKC200000000000088FF88FF88FF01{7:19}I...

b) H in ALS;

If there is no MAC in the path:

...JKC200000000000088FF88FF88FF01HHHH{3:15}I...

If there is a MAC in the path:

...JKC200000000000088FF88FF88FF01{7:19}I...

c) Q in ALS;

If there is no MAC in the path:

...JKC200000000000088FF88FF88FF01HHHH{3:15}I...

If there is a MAC in the path:

...JKC200000000000088FF88FF88FF01{7:19}I...

d) V in ALS.

If there is no MAC in the path:

...JKC200000000000088FF88FF88FFHHHH{26:50}IJKC200000000000088FF88FF88FFHHHH{26:50}IJKC200000000000088FF88FF88FFHHHH{26:50}IJKC200000000000088FF88FF88FFHHHH{26:50}IJKC200000000000088FF88FF88FFHHHH{26:50)IJKC200000000000088FF88FF88FFHHHH{26:50}I[C200000000000088FF88FF88FFHHHH{26:50}IJKC200000000000088FF88FF88FFHHHH{26:50}IJKC200000000000088FF88FF88FFHHHH{26:50}IJKC200000000000088FF88FF88FFHHHH{26:50}I

If there is a MAC in the path:

...JKC200000000000088FF88FF88FF{28:52}IJKC200000000000088FF88FF88FF{28:52}IJKC200000000000088FF88FF88FF{28:52}IJKC200000000000088FF88FF88FF{28:52}IJKC200000000000088FF88FF88FF{28:52}IJKC200000000000088FF88FF88FF{28:52}IJKC200000000000088FF88FF88FF{28:52}IJKC200000000000088FF88FF88FF{28:52}IJKC200000000000088FF88FF88FF{28:52}I...

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