INTERNATIONAL STANDARD

ISO/IEC 14443-4

Second edition
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Identification cards — Contactless integrated circuit cards — Proximity cards —

Part 4: Transmission protocol

Cartes d'identification — Cartes à circuit(s) intégré(s) sans contact — Cartes de proximité —

Partie 4: Protocole de transmission

Reference number
ISO/IEC 14443-4:2008(E)

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Foreword

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work. In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1.

International Standards are drafted in accordance with the rules given in the ISO/IEC Directives, Part 2.

The main task of the joint technical committee is to prepare International Standards. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75 % of the national bodies casting a vote.

ISO/IEC 14443-4 was prepared by Joint Technical Committee ISO/IEC JTC 1, *Information technology*, Subcommittee SC 17, *Cards and personal identification*.

This second edition cancels and replaces the first edition (ISO/IEC 14443-4:2001). It also incorporates the Amendment ISO/IEC 14443-4:2001/Amd.1:2006.

ISO/IEC 14443 consists of the following parts, under the general title *Identification cards — Contactless integrated circuit cards — Proximity cards*:

— *Part 1: Physical characteristics*

— *Part 2: Radio frequency power and signal interface*

— *Part 3: Initialization and anticollision*

— *Part 4: Transmission protocol*

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Introduction

ISO/IEC 14443 is one of a series of International Standards describing the parameters for identification cards as defined in ISO/IEC 7810, and the use of such cards for international interchange.

The protocol as defined in this part of ISO/IEC 14443 is capable of transferring the application protocol data units as defined in ISO/IEC 7816-4. Thus, application protocol data units may be mapped as defined in ISO/IEC 7816-4 and application selection may be used as defined ISO/IEC 7816-5.

ISO/IEC 14443 is intended to allow operation of proximity cards in the presence of other contactless cards conforming to ISO/IEC 10536 and ISO/IEC 15693 and Near Field Communication (NFC) devices conforming to ISO/IEC 18092 and ISO/IEC 21481.

The International Organization for Standardization (ISO) and International Electrotechnical Commission (IEC) draw attention to the fact that it is claimed that compliance with this document may involve the use of patents.

ISO and IEC take no position concerning the evidence, validity and scope of these patent rights.

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JP 2129209, JP 2561051, JP 2981517 Contactless Responding Unit	OMRON Intellectual Property Department Law & Intellectual Property H.Q. 20, Igadera Shimokaiinji Nagaokakyo City Kyoto 617-8510 Japan
Patent EP 0 492 569 B1 A system and method for the non-contact transmission of data	ON-TRACK INNOVATIONS Z.H.R. Industrial Zone P O Box 32 Rosh-Pina 12000 Israel

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US Patent No. 4, 661,691	JOHN W HALPERN C/O Vincent M DeLuca Rothwell, Figg, Ernst & Kurz, p.c. 555 Thirteenth Street, N.W. Suite 701 East Tower Washington, D.C. 20004
WO 89 05549 A	MAGELLAN CORPORATION 8717 Research Drive Irvine CA 92618 USA

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Identification cards — Contactless integrated circuit cards — Proximity cards —

Part 4: Transmission protocol

1 Scope

This part of ISO/IEC 14443 specifies a half-duplex block transmission protocol featuring the special needs of a contactless environment and defines the activation and deactivation sequence of the protocol.

This part of ISO/IEC 14443 is intended to be used in conjunction with other parts of ISO/IEC 14443 and is applicable to proximity cards or objects of Type A and Type B.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC 7816-3, *Identification cards — Integrated circuit cards — Part 3: Cards with contacts — Electrical interface and transmission protocols*

ISO/IEC 7816-4, *Identification cards — Integrated circuit cards — Part 4: Organization, security and commands for interchange*

ISO/IEC 14443-2, *Identification cards — Contactless integrated circuit cards — Proximity cards — Part 2: Radio frequency power and signal interface*

ISO/IEC 14443-3, *Identification cards — Contactless integrated circuit cards — Proximity cards — Part 3: Initialization and anticollision*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1
bit duration
one elementary time unit (etu), calculated by the following formula:

$$1 \text{ etu} = 128 / (D \times fc)$$

the initial value of the divisor D is 1, giving the initial etu as follows:

$$1 \text{ etu} = 128 / fc$$

where *fc* is the carrier frequency as defined in ISO/IEC 14443-2.

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3.2
block
special type of frame, which contains a valid protocol data format

NOTE A valid protocol data format includes I-blocks, R-blocks or S-blocks.

3.3
invalid block
type of frame, which contains an invalid protocol format

NOTE A time-out, when no frame has been received, is not interpreted as an invalid block.

3.4
frame
sequence of bits as defined in ISO/IEC 14443-3

NOTE The PICC Type A uses the standard frame defined for Type A and the PICC Type B uses the frame defined for Type B.

4 Symbols and abbreviated terms

ACK	positive ACKnowledgement
ATS	Answer To Select
ATQA	Answer To reQuest, Type A
ATQB	Answer To reQuest, Type B
CID	Card IDentifier
CRC	Cyclic Redundancy Check, as defined for each PICC Type in ISO/IEC 14443-3
CRC1	most significant byte of CRC (b16 to b9)
CRC2	least significant byte of CRC (b8 to b1)
D	Divisor
DR	Divisor Receive (PCD to PICC)
DRI	Divisor Receive Integer (PCD to PICC)
DS	Divisor Send (PICC to PCD)
DSI	Divisor Send Integer (PICC to PCD)
EDC	Error Detection Code
etu	elementary time unit
fc	carrier frequency
FSC	Frame Size for proximity Card
FSCI	Frame Size for proximity Card Integer
FSD	Frame Size for proximity coupling Device

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FSDI	Frame Size for proximity coupling Device Integer
FWI	Frame Waiting time Integer
FWT	Frame Waiting Time
FWT_{TEMP}	temporary Frame Waiting Time
HLTA	HALT command, Type A
I-block	Information block
INF	INformation Field
MAX	index to define a maximum value
MIN	index to define a minimum value
NAD	Node ADdress
NAK	Negative AcKnowledgement
OSI	Open Systems Interconnection
PCB	Protocol Control Byte
PCD	Proximity Coupling Device
PICC	proximity card or object
PPS	Protocol and Parameter Selection
PPSS	Protocol and Parameter Selection Start
PPS0	Protocol and Parameter Selection parameter 0
PPS1	Protocol and Parameter Selection parameter 1
R-block	Receive ready block
R(ACK)	R-block containing a positive acknowledge
R(NAK)	R-block containing a negative acknowledge
RATS	Request for Answer To Select
REQA	REQuest Command, Type A
RFU	Reserved for Future Use by ISO/IEC
S-block	Supervisory block
SAK	Select AcKnowledge
SFGI	Start-up Frame Guard time Integer
SFGT	Start-up Frame Guard Time
WUPA	Wake-UP command, Type A

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WTX Waiting Time eXtension

WTXM Waiting Time eXtension Multiplier

For the purposes of this document, the following notation applies:

— (xxxxx)b Data bit representation;

— 'XY' Hexadecimal notation, equal to XY to the base 16.

5 Protocol activation of PICC Type A

The following activation sequence shall be applied:

— PICC activation sequence as defined in ISO/IEC 14443-3 (request, anticollision loop and select).

— The SAK byte shall be checked for availability of an ATS. The SAK is defined in ISO/IEC 14443-3.

— The PICC may be set to HALT state, using the HLTA Command as defined in ISO/IEC 14443-3, if no ATS is available.

— The RATS may be sent by the PCD as next command after receiving the SAK if an ATS is available.

— The PICC shall send its ATS as answer to the RATS. The PICC shall only answer to the RATS if the RATS is received directly after the selection.

— If the PICC supports any changeable parameters in the ATS, a PPS request may be used by the PCD as the next command after receiving the ATS to change parameters.

— The PICC shall send a PPS Response as answer to the PPS request.

A PICC does not need to implement the PPS, if it does not support any changeable parameters in the ATS.

The PCD activation sequence for a PICC Type A is shown in Figure 1.

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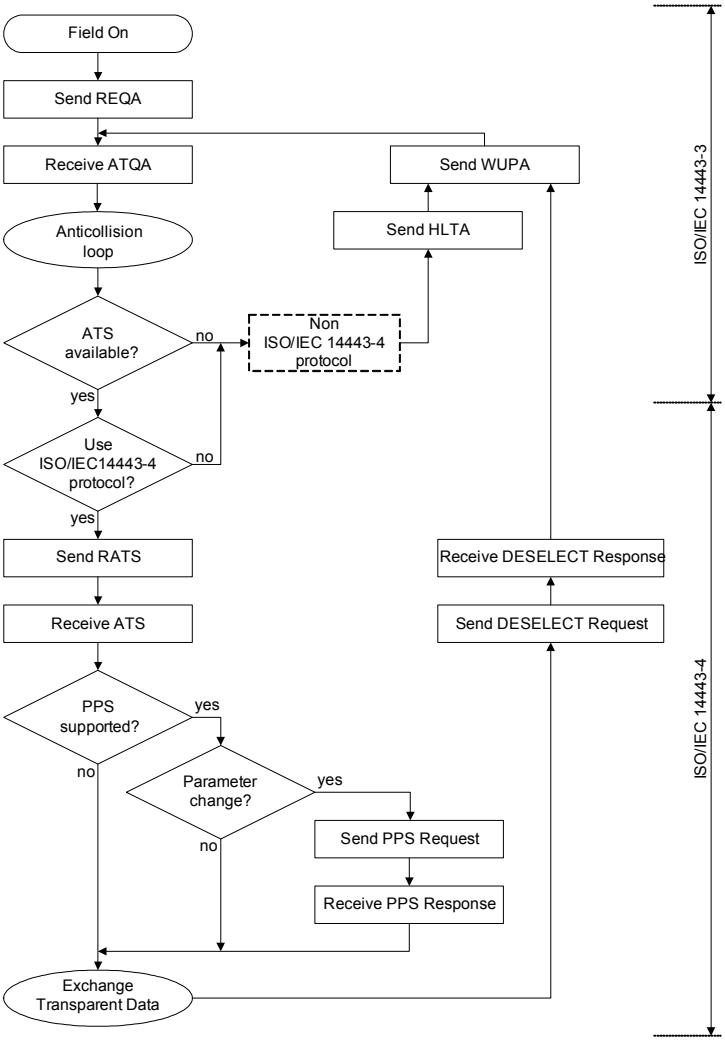

Figure 1 — Activation of a PICC Type A by a PCD

5.1 Request for answer to select

This clause defines the RATS with all its fields (see Figure 2).

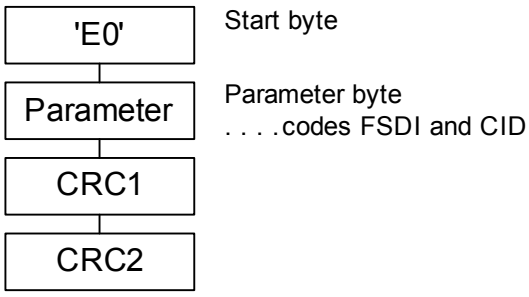

Figure 2 — Request for answer to select

The parameter byte consists of two parts (see Figure 3):

— The most significant half-byte b8 to b5 is called FSDI and codes FSD. The FSD defines the maximum size of a frame the PCD is able to receive. The coding of FSD is given in Table 1.

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— A PCD setting FSDI = '9'-'F' is not compliant with this standard. A received value of FSDI = '9'-'F' should be interpreted by the PICC as FSDI = '8' (FSD = 256 bytes).

— The least significant half byte b4 to b1 is named CID and it defines the logical number of the addressed PICC in the range from 0 to 14. The value 15 is RFU. The CID is specified by the PCD and shall be unique for all PICCs, which are in the ACTIVE state at the same time. The CID is fixed for the time the PICC is active and the PICC shall use the CID as its logical identifier, which is contained in the first error-free RATS received.

— A PCD setting CID = 15 is not compliant with this standard. For PICC behaviour see 5.6.1.2 (c).

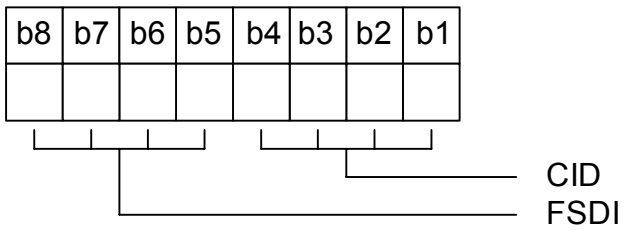

Figure 3 — Coding of RATS parameter byte

Table 1 — FSDI to FSD conversion

FSDI	‘0’	‘1’	‘2’	‘3’	‘4’	‘5’	‘6’	‘7’	‘8’	‘9’-‘F’
FSD (bytes)	16	24	32	40	48	64	96	128	256	RFU

5.2 Answer to select

This clause defines the ATS with all its available fields (see Figure 4).

In the case that one of the defined fields is not present in an ATS sent by a PICC the default values for that field shall apply.

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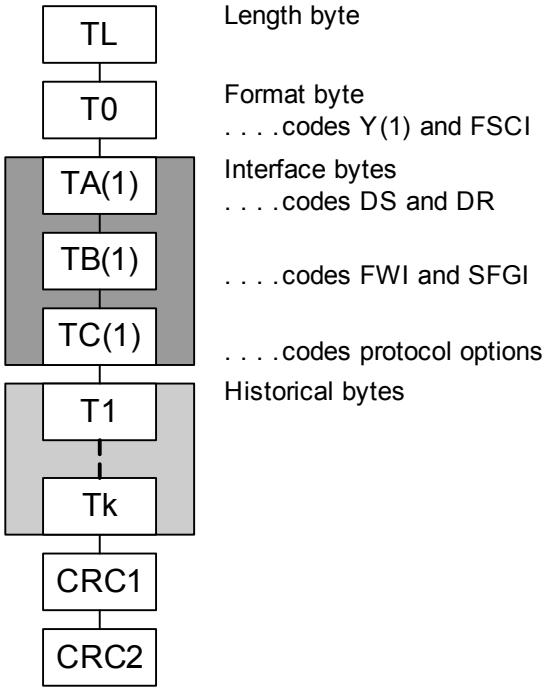

Figure 4 — Structure of the ATS

5.2.1 Structure of the bytes

The length byte TL is followed by a variable number of optional subsequent bytes in the following order:

— format byte T0,

— interface bytes TA(1), TB(1), TC(1) and

— historical bytes T1 to Tk.

5.2.2 Length byte

The length byte TL is mandatory and specifies the length of the transmitted ATS including itself. The two CRC bytes are not included in TL. The maximum size of the ATS shall not exceed the indicated FSD. Therefore the maximum value of TL shall not exceed FSD-2.

5.2.3 Format byte

The format byte T0 is optional and is present as soon as the length is greater than 1. The ATS can only contain the following optional bytes when this format byte is present.

T0 consists of three parts (see Figure 5):

— The most significant bit b8 shall be set to 0. The value 1 is RFU.

— The bits b7 to b5 contain Y(1) indicating the presence of subsequent interface bytes TC(1), TB(1) and TA(1).

— The least significant half byte b4 to b1 is called FSCI and codes FSC. The FSC defines the maximum size of a frame accepted by the PICC. The default value of FSCI is 2 and leads to a FSC of 32 bytes. The coding of FSC is equal to the coding of FSD (see Table 1).

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— A PICC setting FSCI = '9'-'F' is not compliant with this standard. A received value of FSCI = '9'-'F' should be interpreted by the PCD as FSCI = '8' (FSC = 256 bytes). A PICC not setting b8 to 0 is not compliant with this standard. The PCD should ignore b8 and its interpretation of any other field of the whole frame shall not change.

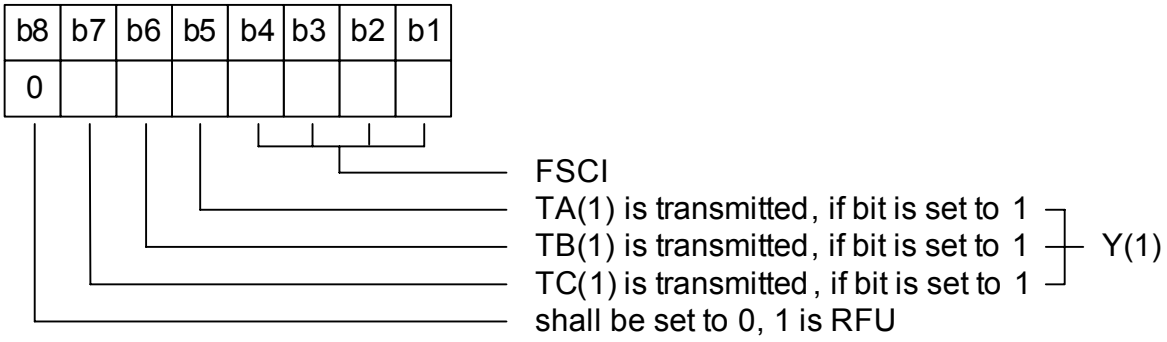

Figure 5 — Coding of format byte

5.2.4 Interface byte TA(1)

The interface byte TA(1) consists of four parts (see Figure 6):

— The most significant bit b8 codes the possibility to handle different divisors for each direction. When this bit is set to 1 the PICC is unable to handle different divisors for each direction.

— The bits b7 to b5 code the bit rate capability of the PICC for the direction from PICC to PCD, called DS. The default value shall be (000)b.

— The bit b4 shall be set to (0)b and the other value is RFU.

— The bits b3 to b1 code the bit rate capability of the PICC for the direction from PCD to PICC, called DR. The default value shall be (000)b.

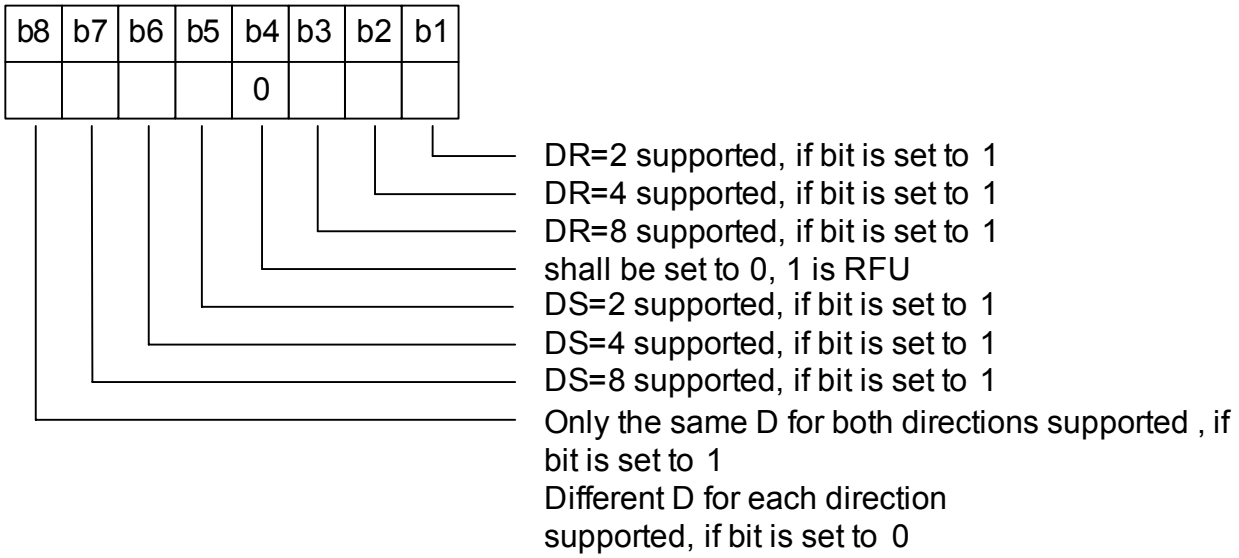

Figure 6 — Coding of interface byte TA(1)

The selection of a specific divisor D for each direction may be done by the PCD using a PPS.

A PICC setting b4 = 1 is not compliant with this standard. A received value of TA(1) with b4 = 1 should be interpreted by the PCD as (b8 to b1) = (00000000)b (only ~106 kbit/s in both directions).

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5.2.5 Interface byte TB(1)

The interface byte TB(1) conveys information to define the frame waiting time and the start-up frame guard time.

The interface byte TB(1) consists of two parts (see Figure 7):

— The most significant half-byte b8 to b5 is called FWI and codes FWT (see 7.2).

— The least significant half byte b4 to b1 is called SFGI and codes a multiplier value used to define the SFGT. The SFGT defines a specific guard time needed by the PICC before it is ready to receive the next frame after it has sent the ATS. SFGI is coded in the range from 0 to 14. The value of 15 is RFU. The value of 0 indicates no SFGT needed and the values in the range from 1 to 14 are used to calculate the SFGT with the formula given below. The default value of SFGI is 0.

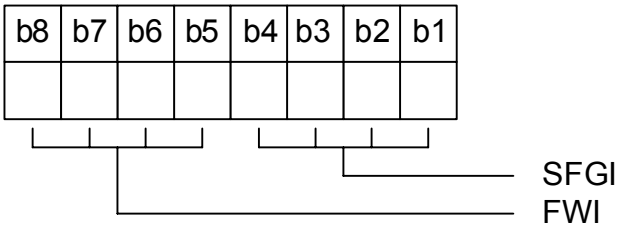

Figure 7 — Coding of interface byte TB(1)

SFGT is calculated by the following formula:

$SFGT = (256 \times 16 / fc) \times 2^{SFGI}$

$SFGT_{MIN}$ = minimum value of the frame delay time as defined in ISO/IEC 14443-3

$SFGT_{DEFAULT}$ = minimum value of the frame delay time as defined in ISO/IEC 14443-3

$SFGT_{MAX} = (256 \times 16 / fc) \times 2^{14}$ (~4949 ms)

A PICC setting SFGI = 15 is not compliant with this standard. Until the RFU value 15 is assigned by ISO/IEC, a PCD receiving SFGI = 15 should interpret it as SFGI = 0.

A PICC setting FWI = 15 is not compliant with this standard. Until the RFU value 15 is assigned by ISO/IEC, a PCD receiving FWI = 15 should interpret it as FWI = 4.

5.2.6 Interface byte TC(1)

The interface byte TC(1) specifies a parameter of the protocol.

The specific interface byte TC(1) consists of two parts (see Figure 8):

— The most significant bits b8 to b3 shall be (000000)b and all other values are RFU.

— The bits b2 and b1 define which optional fields in the prologue field a PICC does support. The PCD is allowed to skip fields, which are supported by the PICC, but a field not supported by the PICC shall never be transmitted by the PCD. The default value shall be (10)b indicating CID supported and NAD not supported.

— A PICC setting (b8 to b3) <> (000000)b is not compliant with this standard. The PCD should ignore (b8 to b3) and its interpretation of (b2,b1) or of any other field of the whole frame shall not change.

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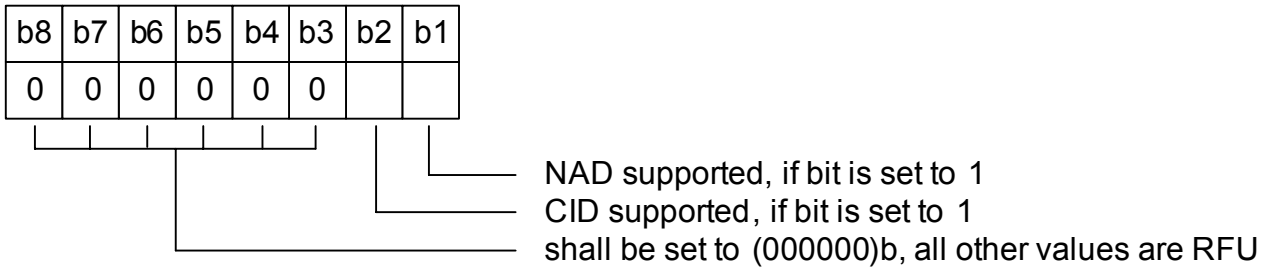

Figure 8 — Coding of interface byte TC(1)

5.2.7 Historical bytes

The historical bytes T1 to Tk are optional and designate general information. The maximum length of the ATS gives the maximum possible number of historical bytes. ISO/IEC 7816-4 specifies the content of the historical bytes.

5.3 Protocol and parameter selection request

PPS request contains the start byte that is followed by two parameter bytes (see Figure 9).

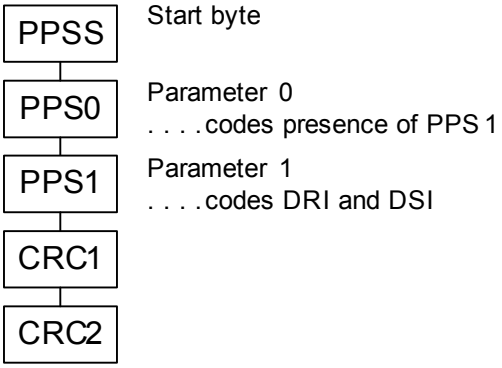

Figure 9 — Protocol and parameter selection request

5.3.1 Start byte

PPSS consists of two parts (see Figure 10):

— The most significant half byte b8 to b5 shall be set to (1101)b and identifies the PPS.

— The least significant half byte b4 to b1 is named CID and it defines the logical number of the addressed PICC.

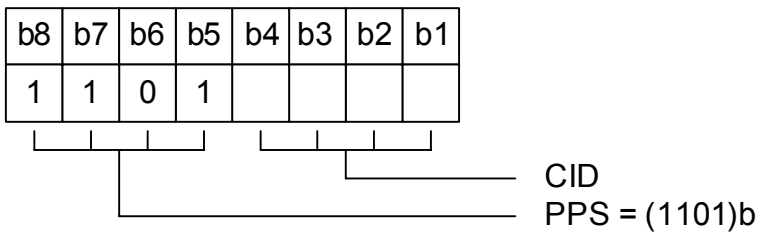

Figure 10 — Coding of PPSS

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5.3.2 Parameter 0

PPS0 indicates the presence of the optional byte PPS1 (see Figure 11).

A PCD setting (b4 to b1) <> (0001)b and/or setting (b8 to b6) <> (000)b is not compliant with this standard. A PICC receiving (b4 to b1) <> (0001)b and/or receiving (b8 to b6) <> (000)b shall apply 5.6.2.2 (b).

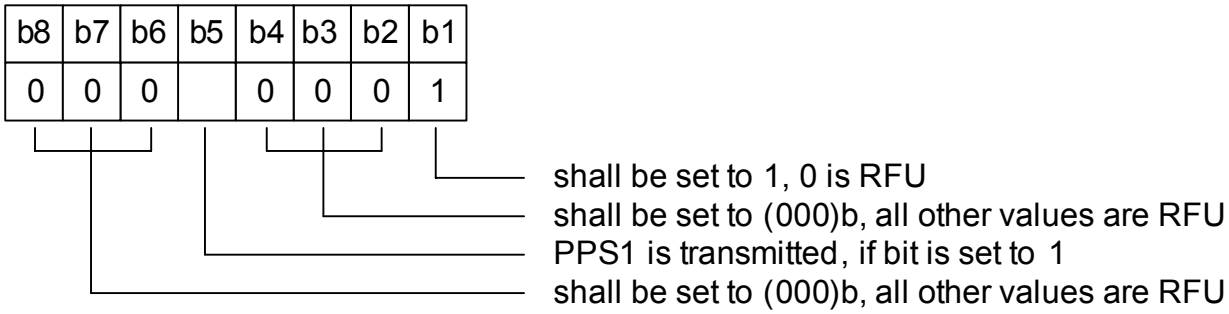

Figure 11 — Coding of PPS0

5.3.3 Parameter 1

PPS1 consists of three parts (see Figure 12):

— The most significant half byte b8 to b5 shall be (0000)b and all other values are RFU.

— The bits b4 and b3 are called DSI and code the selected divisor integer from PICC to PCD.

— The bits b2 and b1 are called DRI and code the selected divisor integer from PCD to PICC.

— A PCD setting (b8 to b5) <> (0000)b is not compliant with this standard. A PICC receiving (b8 to b5) <> (0000)b shall apply 5.6.2.2 (b).

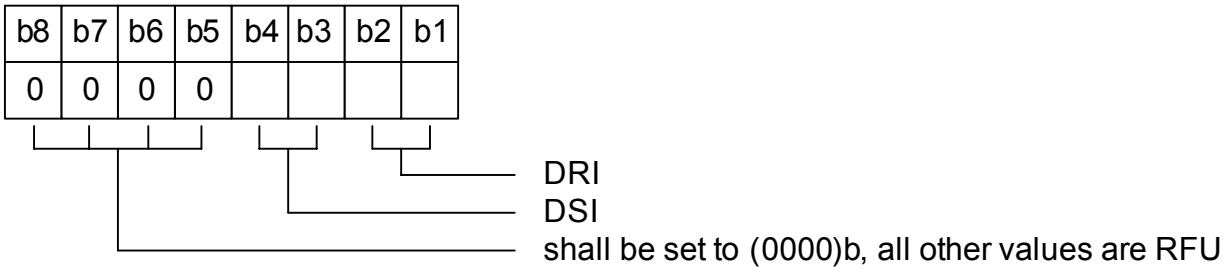

Figure 12 — Coding of PPS1

For the definition of DS and DR, see 5.2.4.

The coding of D is given in Table 2.

Table 2 — DRI, DSI to D conversion

DRI, DSI	(00)b	(01)b	(10)b	(11)b
D	1	2	4	8

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5.4 Protocol and parameter selection response

The PPS response acknowledges the received PPS request (see Figure 13) and it contains only the start byte (see 5.3.1).

The new bit rates shall become effective in the PICC immediately after it has sent the PPS response. A PCD that changes the bit rate when the PPS response is missing or invalid or when the PPSS returned by the PICC is not identical with the PPSS sent by the PCD is not compliant with this standard.

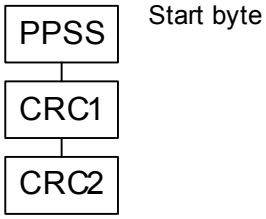

Figure 13 — Protocol and parameter selection response

5.5 Activation frame waiting time

The activation frame waiting time defines the maximum time for a PICC to start sending its response frame after the end of a frame received from the PCD and has a value of 65536/*fc* (~4833 µs).

NOTE The minimum time between frames in any direction is defined in ISO/IEC 14443-3.

5.6 Error detection and recovery

5.6.1 Handling of RATS and ATS

5.6.1.1 PCD rules

When the PCD has sent the RATS and receives a valid ATS the PCD shall continue operation.

In any other case the PCD may retransmit the RATS before it shall use the deactivation sequence as defined in clause 8. In case of failure of this deactivation sequence it may use the HLTA Command as defined in ISO/IEC 14443-3.

5.6.1.2 PICC rules

When the PICC has been selected with the last command and

a) receives a valid RATS, the PICC

   — shall send back its ATS and

   — shall disable the RATS (stop responding to received RATS).

b) receives a valid block (HLTA):

   — shall process the command and shall enter HALT state.

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c) receives an invalid block or RATS with CID = 15:

— shall not respond and shall enter IDLE state or HALT state as specified in Figure 6 “PICC Type A State Diagram” of ISO/IEC 14443-3.

5.6.2 Handling of PPS request and PPS response

5.6.2.1 PCD rules

When the PCD has sent a PPS request and received a valid PPS response the PCD shall activate the selected parameters and continue operation. In any other case the PCD may retransmit a PPS request and continue operation.

5.6.2.2 PICC rules

When the PICC has received a RATS, sent its ATS and

a) received a valid PPS request, the PICC

— shall send the PPS response,

— shall disable the PPS request (stop responding to received PPS requests) and

— shall activate the received parameter.

b) received an invalid block, the PICC

— shall disable the PPS request (stop responding to received PPS requests) and

— shall remain in receive mode.

c) received a valid block, except a PPS request, the PICC

— shall disable the PPS request (stop responding to received PPS requests) and

— shall continue operation.

5.6.3 Handling of the CID during activation

When the PCD has sent a RATS containing a CID=*n* not equal to 0 and

a) received an ATS indicating CID is supported, the PCD

— shall send blocks containing CID=n to this PICC and

— shall not use the CID=n for further RATS while this PICC is in ACTIVE state.

b) received an ATS indicating CID is not supported, the PCD

— shall send blocks containing no CID to this PICC and

— shall not activate any other PICC while this PICC is in ACTIVE state.

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When the PCD has sent a RATS containing a CID equal to 0 and

a) received an ATS indicating CID is supported, the PCD

   — may send blocks containing CID equal to 0 to this PICC and

   — shall not activate any other PICC while this PICC is in ACTIVE state.

b) received an ATS indicating CID is not supported, the PCD shall

   — send blocks containing no CID to this PICC and

   — not activate any other PICC while this PICC is in ACTIVE state.

6 Protocol activation of PICC Type B

The activation sequence for a PICC Type B is described in ISO/IEC 14443-3.

7 Half-duplex block transmission protocol

The half-duplex block transmission protocol addresses the special needs of contactless card environments and uses the frame format as defined in ISO/IEC 14443-3.

Other relevant elements of the frame format are:

— block format,

— maximum frame waiting time,

— power indication and

— protocol operation.

This protocol is designed according to the principle layering of the OSI reference model, with particular attention to the minimization of interactions across boundaries. Four layers are defined:

— Physical layer exchanges bytes according to ISO/IEC 14443-3.

— Data link layer exchanges blocks as defined in this clause.

— Session layer combined with the data link layer for a minimum overhead.

— Application layer processing commands, which involve the exchange of at least one block or chain of blocks in either direction.

NOTE Application selection may be used as defined in ISO/IEC 7816-4. Implicit application selection is not recommended to be used with multi-application PICCs.

7.1 Block format

The block format (see Figure 14) consists of a prologue field (mandatory), an information field (optional) and an epilogue field (mandatory).

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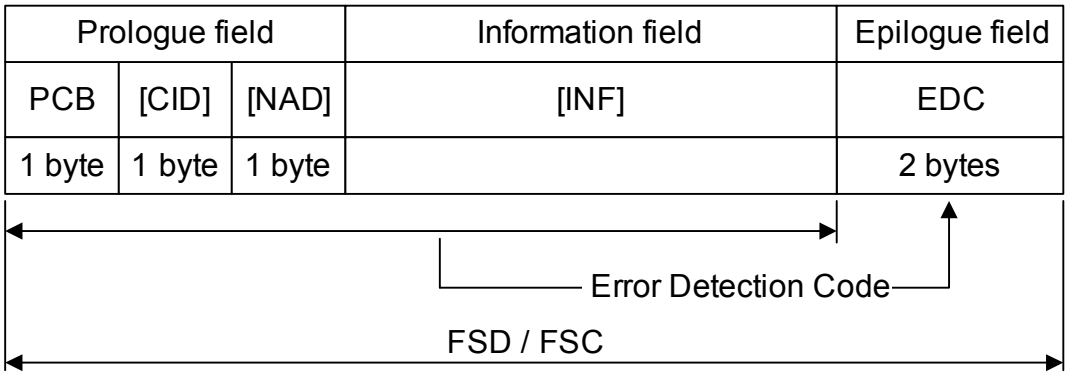

NOTE The items in brackets indicate optional requirements.

Figure 14 — Block format

7.1.1 Prologue field

The prologue field is mandatory and may be 1, 2 or 3 bytes with PCB mandatory and CID and NAD optional.

7.1.1.1 Protocol control byte field

The PCB is used to convey the information required to control the data transmission.

The protocol defines three fundamental types of blocks:

— I-block used to convey information for use by the application layer.

— R-block used to convey positive or negative acknowledgements. An R-block never contains an INF field. The acknowledgement relates to the last received block.

— S-block used to exchange control information between the PCD and the PICC. Two different types of S-blocks are defined:

1) Waiting time extension containing a 1 byte long INF field and

2) DESELECT containing no INF field.

The coding of the PCB depends on its type and is defined by the following figures. PCB coding not defined here are either used in other clauses of ISO/IEC 14443 or are RFU. The coding of I-blocks, R-blocks and S-blocks are shown in Figure 15, Figure 16 and Figure 17.

A PICC or PCD setting b6 <> 0 of an I-block is not compliant with this standard. A PICC or PCD setting b2 <> 1 of an R-block is not compliant with this standard. A PICC or PCD setting (b2,b1) <> (10)b of an S-block is not compliant with this standard.

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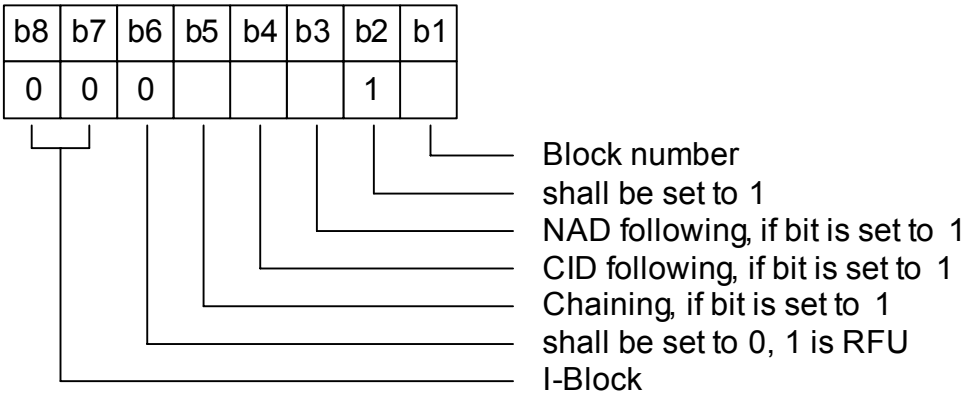

Figure 15 — Coding of I-block PCB

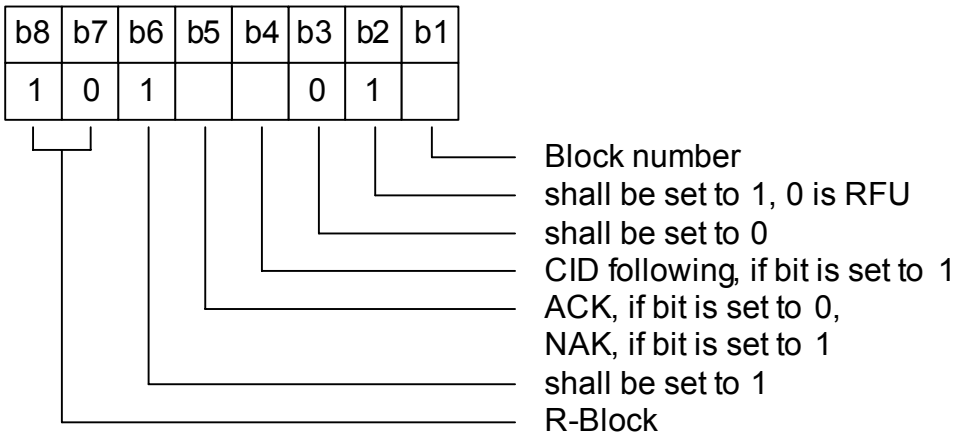

Figure 16 — Coding of R-block PCB

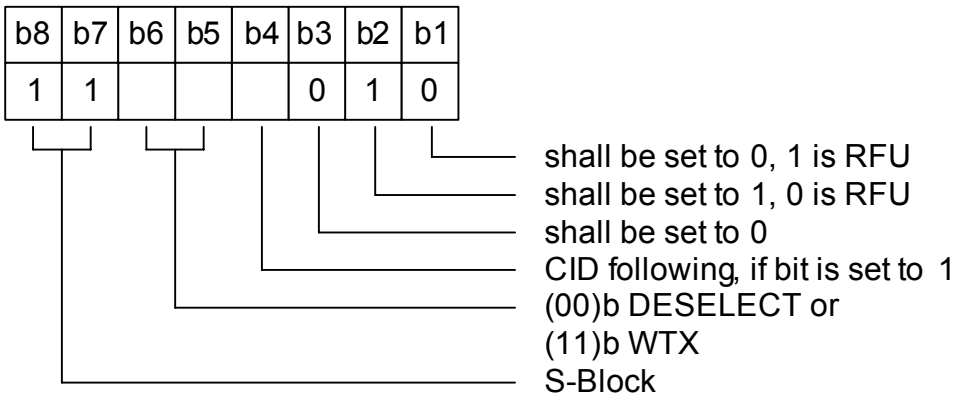

Figure 17 — Coding of S-block PCB

7.1.1.2 Card identifier field

The CID field is used to identify a specific PICC and consists of three parts (see Figure 18):

— The two most significant bits b8 and b7 are used to indicate the power level indication received by a PICC from a PCD. These two bits shall be set to (00)b for PCD to PICC communication. For a definition of power level indication, see 7.4.

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— The bits b6 and b5 are used to convey additional information, which are not defined and shall be set to (00)b and all other values are RFU.

— A PICC or PCD setting (b6,b5) <> (00)b is not compliant with this standard. (b6,b5) <> (00)b shall be treated as a protocol error.

— The bits b4 to b1 code the CID.

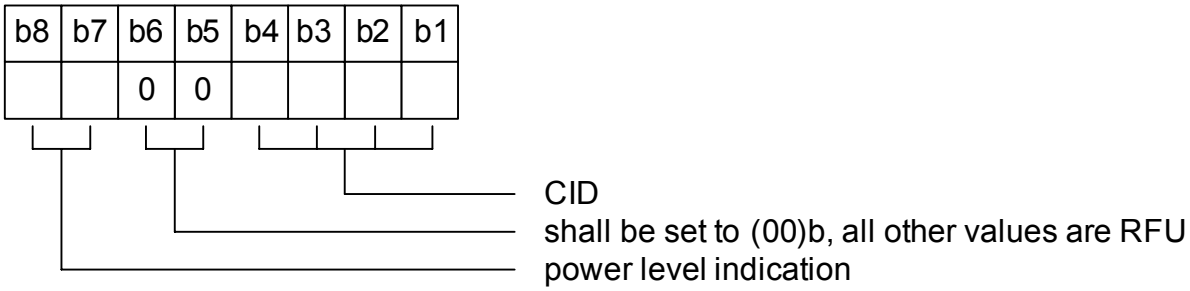

Figure 18 — Coding of card identifier

The coding of CID is given in 5.1 for Type A and ISO/IEC 14443-3 for Type B.

The handling of the CID by a PICC is described below:

A PICC, which does not support a CID

— shall ignore any block containing a CID.

A PICC, which does support a CID

— shall respond to blocks containing its CID by using its CID,

— shall ignore blocks containing other CIDs and

— shall, in case its CID is 0, respond also to blocks containing no CID by using no CID.

7.1.1.3 Node address field

The NAD in the prologue field is reserved to build up and address different logical connections. The usage of the NAD shall be compliant with the definition from ISO/IEC 7816-3, when the bits b8 and b4 are both set to 0. All other values are RFU.

A PICC or PCD setting b8 <> 0 and/or b4 <> 0 is not compliant with this standard. b8 <> 0 and/or b4 <> 0 shall be treated as a protocol error.

The following definitions shall apply for the usage of the NAD:

a) The NAD field shall only be used for I-blocks.

b) When the PCD uses the NAD, the PICC shall also use the NAD.

c) During chaining the NAD shall only be transmitted in the first block of chain.

d) The PCD shall never use the NAD to address different PICCs (The CID shall be used to address different PICCs).

e) When the PICC does not support the NAD, it shall ignore any block containing the NAD.

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7.1.2 Information field

The INF field is optional. When present, the INF field conveys either application data in I-blocks or non-application data and status information in S-blocks. The length of the information field is calculated by counting the number of bytes of the whole block minus length of prologue and epilogue field.

7.1.3 Epilogue field

The epilogue field contains the EDC of the transmitted block, which is the CRC defined in ISO/IEC 14443-3.

7.2 Frame waiting time

The FWT defines the time within which a PICC shall start its response frame after the end of a PCD frame (see Figure 19).

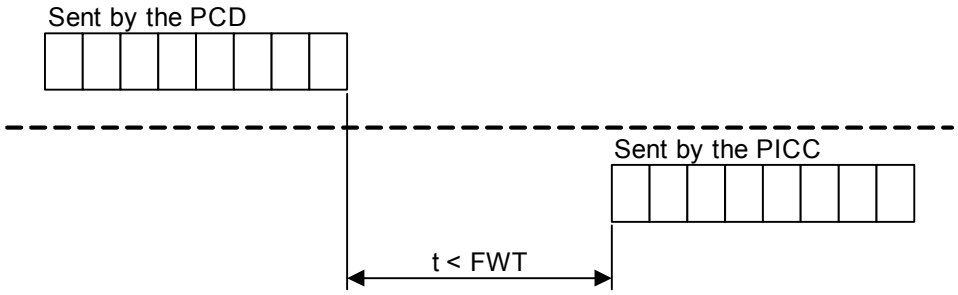

Figure 19 — Frame waiting time

NOTE 1 The minimum time between frames in any direction is defined in ISO/IEC 14443-3.

FWT is calculated by the following formula:

$$FWT = (256 \times 16 / fc) \times 2^{FWI}$$

where the value of FWI has the range from 0 to 14 and the value of 15 is RFU. For Type A, if TB(1) is omitted, the default value of FWI is 4, which gives a FWT value of ~ 4,8 ms.

For FWI = 0, FWT = FWT_{MIN} (~302 µs)

For FWI = 14, FWT = FWT_{MAX} (~4949 ms)

The FWT value shall be used by the PCD to detect a protocol error or an unresponsive PICC. The PCD obtains the right to re-transmit if the start of a response from the PICC is not received within FWT.

The FWI field for Type B is located in ATQB as defined in ISO/IEC 14443-3. The FWI field for Type A is located in the ATS (see 5.2.5).

The PICC shall not set FWI to the RFU value of 15. Until the RFU value 15 is assigned by ISO/IEC, a PCD receiving FWI = 15 should interpret it as FWI = 4.

NOTE 2 This clause is added for PCD's compatibility with future PICCs when ISO/IEC defines the RFU value 15.

7.3 Frame waiting time extension

When the PICC needs more time than the defined FWT to process the received block it shall use an S(WTX) request for a waiting time extension. An S(WTX) request contains a 1 byte long INF field that consists of two parts (see Figure 20):

— The two most significant bits b8 and b7 code the power level indication (see 7.4).

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— A PCD not setting (b8,b7) = (00)b is not compliant with this standard. The PICC shall treat (b8,b7) <> (00)b as protocol error.

— The least significant bits b6 to b1 code the WTXM. The WTXM is coded in the range from 1 to 59. The values 0 and 60 to 63 are RFU.

— A PICC setting WTXM = 0 or WTXM = 60-63 is not compliant with this standard. When receiving WTXM = 0 or WTXM = 60-63 the PCD shall treat it as a protocol error.

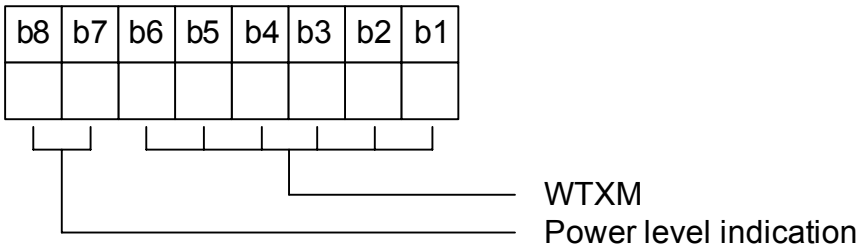

Figure 20 — Coding of INF field of an S(WTX) request

The PCD shall acknowledge by sending an S(WTX) response containing also a 1 byte long INF field that consists of two parts (see Figure 21) and contains the same WTXM as received in the request:

— The most significant bits b8 and b7 shall be (00)b and all other values are RFU.

— The least significant bits b6 to b1 codes the acknowledged WTXM value used to define a temporary FWT.

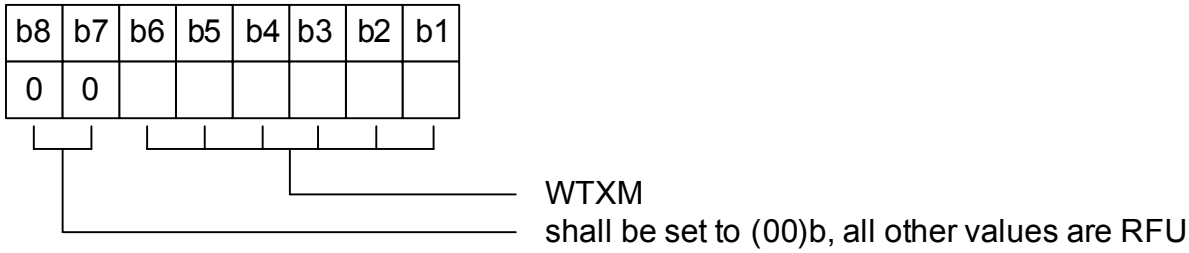

Figure 21 — Coding of INF field of an S(WTX) response

The corresponding temporary value of FWT is calculated by the following formula:

$FWT_{TEMP} = FWT \times WTXM$.

The time FWT_{TEMP} requested by the PICC, starts after the PCD has sent the S(WTX) response.

FWT_{MAX} shall be used, when the formula results in a value higher than FWT_{MAX}.

The temporary FWT applies only until the next block has been received by the PCD.

7.4 Power level indication

The power level indication is coded as shown in Table 3 using two bits embedded in the CID field (when present) and in the S-block sent by the PICC (see 7.1.1.2 and 7.3).

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Table 3 — Coding of power level indication

(00)b	PICC does not support the power level indication
(01)b	Insufficient power for full functionality
(10)b	Sufficient power for full functionality
(11)b	More than sufficient power for full functionality

NOTE Interpretation of the power level indication by the PCD is optional.

7.5 Protocol operation

After the activation sequence the PICC shall wait for a block as only the PCD has the right to send. After sending a block, the PCD shall switch to receive mode and wait for a block before switching back to transmit mode. The PICC may transmit blocks only in response to received blocks (it is insensitive to time delays). After responding, the PICC shall return to the receive mode.

The PCD shall not initiate a new pair of command/response until the current pair of command/response has been completed or if the frame waiting time is exceeded with no response.

7.5.1 Multi-Activation

The Multi-Activation feature allows the PCD to hold several PICCs in the ACTIVE state simultaneously. It allows switching directly between several PICCs without needing additional time for deactivation of a PICC and activation of another PICC.

For an example of Multi-Activation, see Annex A.

NOTE The PCD needs to handle a separate block number for each activated PICC.

7.5.2 Chaining

The chaining feature allows the PCD or PICC to transmit information that does not fit in a single block as defined by FSC or FSD respectively, by dividing the information into several blocks. Each of those blocks shall have a length less than or equal to FSC or FSD respectively.

The chaining bit in the PCB of an I-block controls the chaining of blocks. Each I-block with the chaining bit set shall be acknowledged by an R-block.

The chaining feature is shown in Figure 22 using a 16 bytes long string transmitted in three blocks.

Notation:

$I(1)_X$ I-block with chaining bit set and block number x

$I(0)_X$ I-block with chaining bit not set (last block of chain) and block number x

$R(ACK)_X$ R-block that indicates a positive acknowledge

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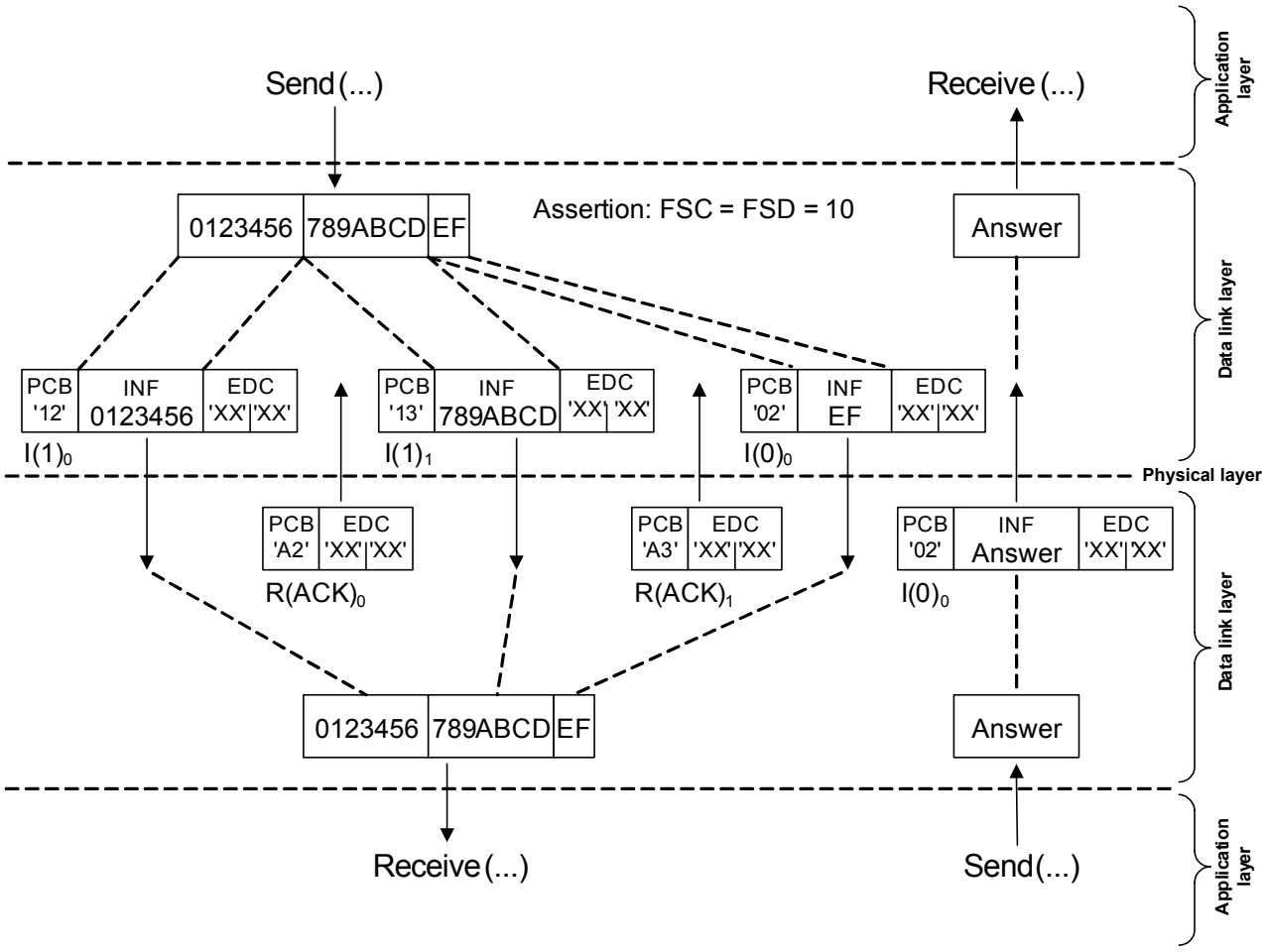

NOTE This example does not use the optional fields NAD and CID.

Figure 22 — Chaining

7.5.3 Block numbering rules

7.5.3.1 PCD rules

Rule A. The PCD block number shall be initialized to 0 for each activated PICC.

Rule B. When an I-block or an R(ACK) block with a block number equal to the current block number is received, the PCD shall toggle the current block number for that PICC before optionally sending a block.

7.5.3.2 PICC rules

Rule C. The PICC block number shall be initialized to 1 at activation.

Rule D. When an I-block is received, the PICC shall toggle its block number before sending a block.

NOTE 1 The PICC may check if the received block number is not in compliance with PCD rules to decide neither to toggle its internal block number nor to send a response block.

Rule E. When an R(ACK) block with a block number not equal to the current PICC's block number is received, the PICC shall toggle its block number before sending a block.

NOTE 2 There is no block number toggling when an R(NAK) block is received.

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7.5.4 Block handling rules

7.5.4.1 General rules

Rule 1. The first block shall be sent by the PCD.

Rule 2. When an I-block indicating chaining is received, the block shall be acknowledged by an R(ACK) block.

Rule 3. S-blocks are only used in pairs. An S(...) request block shall always be followed by an S(...) response block (see 7.3 and 8).

7.5.4.2 PCD rules

Rule 4. When an invalid block is received or a FWT time-out occurs, an R(NAK) block shall be sent (except in the case of PICC chaining or S(DESELECT)).

Rule 5. In the case of PICC chaining, when an invalid block is received or a FWT time-out occurs, an R(ACK) block shall be sent.

NOTE 1 An R(ACK) block may be sent by the PCD only in case of PICC chaining, as the PICC response when receiving an R(ACK) block in other cases is not defined.

Rule 6. When an R(ACK) block is received, if its block number is not equal to the PCD's current block number, the last I-block shall be re-transmitted.

NOTE 2 The last I-block re-transmission is not required out of PCD chaining. The PCD may determine the presence of a PICC by sending R(NAK) blocks at any time out of chaining (including before sending any I-block) and receiving R(ACK) from the PICC if present.

Rule 7. When an R(ACK) block is received, if its block number is equal to the PCD's current block number, chaining shall be continued.

Rule 8. If the S(DESELECT) request is not answered by an error-free S(DESELECT) response the S(DESELECT) request may be re-transmitted or the PICC may be ignored.

7.5.4.3 PICC rules

Rule 9. The PICC is allowed to send an S(WTX) block instead of an I-block or an R(ACK) block.

Rule 10. When an I-block not indicating chaining is received, the block shall be acknowledged by an I-block.

NOTE If the I-block received is empty then the mandatory I-block sent may either be empty or contain any applicative information (e.g. error code).

Rule 11. When an R(ACK) or an R(NAK) block is received, if its block number is equal to the PICC's current block number, the last block shall be re-transmitted.

Rule 12. When an R(NAK) block is received, if its block number is not equal to the PICC's current block number, an R(ACK) block shall be sent.

Rule 13. When an R(ACK) block is received, if its block number is not equal to the PICC's current block number, and the PICC is in chaining, chaining shall be continued.

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7.5.5 PICC presence check

The following methods may be used to check the presence of a PICC at any time including before any I-block exchange.

The PCD shall not check the presence of a PICC until the current pair of command / response has been completed or when the frame waiting time is exceeded with no response.

7.5.5.1 Method 1

The PCD may send an empty I-block and expect to receive an I-block from the PICC.

7.5.5.2 Method 2

Before the first I-block exchange, the PCD may send an R(NAK) block (with block number 0) and expect to receive an R(ACK) (with block number 1) block from the PICC (rule 12).

After the first I-block exchange, the PCD may either

a) send an R(NAK) block (with current block number) and expect to receive an R(ACK) block from the PICC (rule 12), in which case the PCD should not retransmit its last I-block as mentioned in the note in rule 6, or

b) toggle its block number then send an R(NAK) block and expect to receive the last I-block from the PICC (rule 11).

7.5.6 Error detection and recovery

When errors are detected the following recovery rules shall be attempted. The definitions made in this clause overrule the block handling rules (see 7.5.4).

7.5.6.1 Errors detected by the PCD

The following errors shall be detected by the PCD:

a) Transmission error (Frame error or EDC error) or FWT time-out

   The PCD shall attempt error recovery by the following techniques in the order shown:

   — Application of PCD rules (see 7.5.4.2),

   — Optionally apply PCD rules (see 7.5.4.2) once more,

   — Use of S(DESELECT) request,

   — Optionally use of S(DESELECT) request once more (as specified in Clause 8.2),

   — Ignore the PICC.

b) Protocol error (infringement of PCB coding or infringement of protocol rules)

   The PCD shall attempt error recovery by the following techniques in the order shown:

   — Use of S(DESELECT) request,

   — Ignore the PICC.

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7.5.6.2 Errors detected by the PICC

The following errors shall be detected by the PICC:

a) Transmission error (Frame error or EDC error),

b) Protocol error (infringement of the protocol rules).

The PICC shall attempt no error recovery. The PICC shall always return to receive mode, when a transmission error or a protocol error occurs and it shall accept an S(DESELECT) request at any time.

NOTE An R(NAK) block is never sent by the PICC.

8 Protocol deactivation of PICC Type A and Type B

The PICC shall be set to the HALT state, after the transactions between PCD and PICC have been completed.

The deactivation of a PICC is done by using a DESELECT Command.

The DESELECT Command is coded as an S-block of the protocol and consists of an S(DESELECT) request block sent by the PCD and an S(DESELECT) response sent as acknowledge by the PICC.

8.1 Deactivation frame waiting time

The deactivation frame waiting time defines the maximum time for a PICC to start sending its S(DESELECT) response frame after the end of the S(DESELECT) request frame received from the PCD and has a value of 65536/*fc* (~4,8 ms).

NOTE The minimum time between frames in any direction is defined in ISO/IEC 14443-3.

8.2 Error detection and recovery

When the PCD has sent an S(DESELECT) request and has received an S(DESELECT) response, the PICC has been set successfully to the HALT state and the CID assigned to it is released.

When the PCD fails to receive an S(DESELECT) response the PCD may retry the deactivation sequence.

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Annex A
(informative)

Multi-Activation example

The following table describes an example of the usage of Multi-Activation for three PICCs.

Table A.1 — Multi-Activation

PCD Action	Status PICC 1	Status PICC 2	Status PICC 3
Power On field			
Three PICCs enter the field.	IDLE	IDLE	IDLE
Activate PICC with CID=1	ACTIVE(1)	IDLE	IDLE
Any data transmission with CID=1	ACTIVE(1)	IDLE	IDLE
...			
Activate PICC with CID=2	ACTIVE(1)	ACTIVE(2)	IDLE
Any data transmission with CID=1,2	ACTIVE(1)	ACTIVE(2)	IDLE
...			
Activate PICC with CID=3	ACTIVE(1)	ACTIVE(2)	ACTIVE(3)
Any data transmission with CID=1,2,3	ACTIVE(1)	ACTIVE(2)	ACTIVE(3)
...			
S(DESELECT) Command with CID=3	ACTIVE(1)	ACTIVE(2)	HALT
S(DESELECT) Command with CID=2	ACTIVE(1)	HALT	HALT
S(DESELECT) Command with CID=1	HALT	HALT	HALT
...			

NOTE The number n in ACTIVE(n) represents the CID.

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Annex B
(informative)

Protocol scenarios

This annex gives some scenarios for an error-free operation as well as for error handling. These scenarios may be used to build test cases for compliance tests.

B.1 Notation

Any block	===>	correctly received
Any block	=≠=>	erroneously received
Any block	= =>	nothing received (FWT time-out)
Separator line	____	end of the smallest protocol operation

$I(1)_x$	I-block with chaining bit set and block number x
$I(0)_x$	I-block with chaining bit not set (last block of chain) and block number x
$R(ACK)_x$	R-block indicating a positive acknowledge
$R(NAK)_x$	R-block indicating a negative acknowledge
S(...)	S-block

The block numbering in a scenario always starts with the PCD's current block number for the destination PICC. For ease of presentation, scenarios start after the PICC activation sequence and hence the current block numbers start with 0 for the PCD and with 1 for the PICC.

B.2 Error-free operation

B.2.1 Exchange of I-blocks

Scenario 1 Exchange of I-blocks

Comment		**Block No. (0)**	**PCD**		**PICC**	**Block No. (1)**	**Comment**
1.	rule 1		$I(0)_0$	===>		0	rule D
2.	rule B	1		<===	$I(0)_0$		rule 10
3.			$I(0)_1$	===>		1	rule D
4.	rule B	0		<===	$I(0)_1$		rule 10

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B.2.2 Request for waiting time extension

Scenario 2 Waiting time extension

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1		$I(0)_0$	===>		0	rule D
2.				<===	S(WTX) request		rule 9
3.	rule 3		S(WTX) response	===>			
4.	rule B	1		<===	$I(0)_0$		rule 10
5.			$I(0)_1$	===>		1	rule D
6.	rule B	0		<===	$I(0)_1$		rule 10

B.2.3 DESELECT

Scenario 3 DESELECT

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1		$I(0)_0$	===>		0	rule D
2.	rule B	1		<===	$I(0)_0$		rule 10
3.			S(DESELECT) request	===>			
4.				<===	S(DESELECT) response		rule 3

B.2.4 Chaining

Scenario 4 PCD uses chaining

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1		$I(1)_0$	===>		0	rule D
2.	rule B	1		<===	$R(ACK)_0$		rule 2
3.	rule 7		$I(0)_1$	===>		1	rule D
4.	rule B	0		<===	$I(0)_1$		rule 10
5.			$I(0)_0$	===>		0	rule D
6.	rule B	1		<===	$I(0)_0$		rule 10

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Scenario 5 PICC uses chaining

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1		$I(0)_0$	===>		0	rule D
2.	rule B	1		<===	$I(1)_0$		rule 10
3.	rule 2		$R(ACK)_1$	===>		1	rule E
4.	rule B	0		<===	$I(0)_1$		rule 13
5.			$I(0)_0$	===>		0	rule D
6.	rule B	1		<===	$I(0)_0$		rule 10

B.2.5 PICC Presence check

Scenario 6 PICC presence check using method 1

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1 and method 1		$I(0)_0$	===>		0	rule D
2.	rule B	1		<===	$I(0)_0$		rule 10 note

Scenario 7 PICC presence check using method 2 (before the first I-block exchange)

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1 and method 2		$R(NAK)_0$	===>			rule E note
2.		no change		<===	$R(ACK)_1$		rule 12
3.	rule 6 note and method 2	$R(NAK)_0$	===>				rule E note
4.	rule 6 note	no change		<===	$R(ACK)_1$		rule 12
5.			$I(0)_0$	===>		0	rule D
6.	rule B	1		<===	$I(0)_0$		rule 10

Scenario 8 PICC presence check using method 2-a (after the first I-block exchange)

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1		$I(0)_0$	===>		0	rule D
2.	rule B	1		<===	$I(0)_0$		rule 10
3.	method 2-a		$R(NAK)_1$	===>			rule E note
4.	rule 6 note	no change		<===	$R(ACK)_0$		rule 12
5.			$I(0)_1$	===>		1	rule D
6.	rule B	0		<===	$I(0)_1$		rule 10

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Scenario 9 PICC presence check using method 2-b (after the first I-block exchange)

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1		$I(0)_0$	===>		0	rule D
2.	rule B	1		<===	$I(0)_0$		rule 10
3.	method 2-b	0	$R(NAK)_0$	===>			
4.	rule B	1		<===	$I(0)_0$		rule 11
5.			$I(0)_1$	===>		1	rule D
6.	rule B	0		<===	$I(0)_1$		rule 10

B.3 Error handling

B.3.1 Exchange of I-blocks

Scenario 10 Start of protocol

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1		$I(0)_0$	=≠=>			
2.	time-out			<= =	-		
3.	rule 4		$R(NAK)_0$	===>			
4.		no change		<===	$R(ACK)_1$		rule 12
5.	rule 6		$I(0)_0$	===>		0	rule D
6.	rule B	1		<===	$I(0)_0$		rule 10
7.			$I(0)_1$	===>		1	rule D
8.	rule B	0		<===	$I(0)_1$		rule 10

Scenario 11 Exchange of I-blocks

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1		$I(0)_0$	===>		0	rule D
2.	rule B	1		<===	$I(0)_0$		rule 10
3.			$I(0)_1$	=≠=>			
4.	time-out			<= =	-		
5.	rule 4		$R(NAK)_1$	===>			
6.		no change		<===	$R(ACK)_0$		rule 12
7.	rule 6		$I(0)_1$	===>		1	rule D
8.	rule B	0		<===	$I(0)_1$		rule 10
9.			$I(0)_0$	===>		0	rule D
10.	rule B	1		<===	$I(0)_0$		rule 10

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Scenario 12 Exchange of I-blocks

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1		$I(0)_0$	===>		0	rule D
2.				<=≠=	$I(0)_0$		rule 10
3.	rule 4		$R(NAK)_0$	===>			
4.	rule B	1		<===	$I(0)_0$		rule 11
5.			$I(0)_1$	===>		1	rule D
6.	rule B	0		<===	$I(0)_1$		rule 10

Scenario 13 Exchange of I-blocks

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1		$I(0)_0$	===>		0	rule D
2.				<=≠=	$I(0)_0$		rule 10
3.	rule 4		$R(NAK)_0$	=≠=>			
4.	time-out			<= =	-		
5.	rule 4		$R(NAK)_0$	===>			
6.	rule B	1		<===	$I(0)_0$		rule 11
7.			$I(0)_1$	===>		1	rule D
8.	rule B	0		<===	$I(0)_1$		rule 10

B.3.2 Request for waiting time extension

Scenario 14 Request for waiting time extension

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1		$I(0)_0$	===>		0	rule D
2.				<=≠=	S(WTX) request		rule 9
3.	rule 4		$R(NAK)_0$	===>			
4.				<===	S(WTX) request		rule 11
5.	rule 3		S(WTX) response	===>			
6.	rule B	1		<===	$I(0)_0$		rule 10
7.			$I(0)_1$	===>		1	rule D
8.	rule B	0		<===	$I(0)_1$		rule 10

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Scenario 15 Request for waiting time extension

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1		$I(0)_0$	===>		0	rule D
2.				<=≠=	S(WTX) request		rule 9
3.	rule 4		$R(NAK)_0$	=≠=>			
4.	time-out			<= =	-		
5.	rule 4		$R(NAK)_0$	===>			
6.				<===	S(WTX) request		rule 11
7.	rule 3		S(WTX) response	===>			
8.	rule B	1		<===	$I(0)_0$		rule 10
9.			$I(0)_1$	===>		1	rule D
10.	rule B	0		<===	$I(0)_1$		rule 10

Scenario 16 Request for waiting time extension

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1		$I(0)_0$	===>		0	rule D
2.				<===	S(WTX) request		rule 9
3.	rule 3		S(WTX) response	=≠=>			
4.	time-out			<= =	-		
5.	rule 4		$R(NAK)_0$	===>			
6.				<===	S(WTX) request		rule 11
7.	rule 3		S(WTX) response	===>			
8.	rule B	1		<===	$I(0)_0$		rule 10
9.			$I(0)_1$	===>		1	rule D
10.	rule B	0		<===	$I(0)_1$		rule 10

Scenario 17 Request for waiting time extension

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1		$I(0)_0$	===>		0	rule D
2.				<===	S(WTX) request		rule 9
3.	rule 3		S(WTX) response	===>			
4.				<=≠=	$I(0)_0$		rule 10
5.	rule 4		$R(NAK)_0$	===>			
6.	rule B	1		<===	$I(0)_0$		rule 11
7.			$I(0)_1$	===>		1	rule D
8.	rule B	0		<===	$I(0)_1$		rule 10

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Scenario 18 Request for waiting time extension

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1		$I(0)_0$	===>		0	rule D
2.				<===	S(WTX) request		rule 9
3.	rule 3		S(WTX) response	===>			
4.				<=≠=	$I(0)_0$		rule 10
5.	rule 4		$R(NAK)_0$	=≠=>			
6.	time-out			<= =	-		
7.	rule 4		$R(NAK)_0$	===>			
8.	rule B	1		<===	$I(0)_0$		rule 11
9.			$I(0)_1$	===>		1	rule D
10.	rule B	0		<===	$I(0)_1$		rule 10

B.3.3 DESELECT

Scenario 19 DESELECT

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1		$I(0)_0$	===>		0	rule D
2.	rule B			<===	$I(0)_0$		rule 10
3.			S(DESELECT) request	=≠=>			
4.	time-out			<= =	-		
5.	rule 8		S(DESELECT) request	===>			
6.				<===	S(DESELECT) response		rule 3

B.3.4 Chaining

Scenario 20 PCD uses chaining

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1		$I(1)_0$	===>		0	rule D
2.				<=≠=	$R(ACK)_0$		rule 2
3.	rule 4		$R(NAK)_0$	===>			
4.	rule B	1		<===	$R(ACK)_0$		rule 11
5.	rule 7		$I(1)_1$	===>		1	rule D
6.	rule B	0		<===	$R(ACK)_1$		rule 2
7.	rule 7		$I(0)_0$	===>		0	rule D
8.	rule B	1		<===	$I(0)_0$		rule 10
9.			$I(0)_1$	===>		1	rule D
10.	rule B	0		<===	$I(0)_1$		rule 10

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Scenario 21 PCD uses chaining

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1		$I(1)_0$	===>		0	rule D
2.	rule B	1		<===	$R(ACK)_0$		rule 2
3.	rule 7		$I(1)_1$	=≠=>			
4.	time-out			<= =	-		
5.	rule 4		$R(NAK)_1$	===>			
6.		no change		<===	$R(ACK)_0$		rule 12
7.	rule 6		$I(1)_1$	===>		1	rule D
8.	rule B	0		<===	$R(ACK)_1$		rule 2
9.	rule 7		$I(0)_0$	===>		0	rule D
10.	rule B	1		<===	$I(0)_0$		rule 10
11.			$I(0)_1$	===>		1	rule D
12.	rule B	0		<===	$I(0)_1$		rule 10

Scenario 22 PCD uses chaining

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1		$I(1)_0$	===>		0	rule D
2.				<=≠=	$R(ACK)_0$		rule 2
3.	rule 4		$R(NAK)_0$	=≠=>			
4.	time-out			<= =	-		
5.	rule 4		$R(NAK)_0$	===>			
6.	rule B	1		<===	$R(ACK)_0$		rule 11
7.	rule 7		$I(1)_1$	===>		1	rule D
8.	rule B	0		<===	$R(ACK)_1$		rule 2
9.	rule 7		$I(0)_0$	===>		0	rule D
10.	rule B	1		<===	$I(0)_0$		rule 10
11.			$I(0)_1$	===>		1	rule D
12.	rule B	0		<===	$I(0)_1$		rule 10

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Scenario 23 PICC uses chaining

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1		$I(0)_0$	===>		0	rule D
2.	rule B	1		<===	$I(1)_0$		rule 10
3.	rule 2		$R(ACK)_1$	=≠=>			
4.	time-out			<= =	-		
5.	rule 5		$R(ACK)_1$	===>		1	rule E
6.	rule B	0		<===	$I(1)_1$		rule 13
7.	rule 2		$R(ACK)_0$	===>		0	rule E
8.	rule B	1		<===	$I(0)_0$		rule 13
9.			$I(0)_1$	===>		1	rule D
10.	rule B	0		<===	$I(0)_1$		rule 10

Scenario 24 PICC uses chaining

	Comment	Block No. (0)	PCD		PICC	Block No. (1)	Comment
1.	rule 1		$I(0)_0$	===>		0	rule D
2.	rule B	1		<===	$I(1)_0$		rule 10
3.	rule 2		$R(ACK)_1$	===>		1	rule E
4.				<=≠=	$I(1)_1$		rule 13
5.	rule 5		$R(ACK)_1$	===>		no change	
6.	rule B	0		<===	$I(1)_1$		rule 11
7.	rule 2		$R(ACK)_0$	===>		0	rule E
8.	rule B	1		<===	$I(0)_0$		rule 13
9.			$I(0)_1$	===>		1	rule D
10.	rule B	0		<===	$I(0)_1$		rule 10

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Annex C
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Block and frame coding overview

This clause gives an overview of the different block and frame coding sent by the PCD. The type of a block respectively frame is indicated by the first byte.

Definitions made in ISO/IEC 14443-3:

REQA	(0100110)b (7 bit)
WUPA	(1010010)b (7 bit)
REQB / WUPB	(00000101)b
Slot-MARKER (Type B only)	(xxxx0101)b
SELECT (Type A only)	(1001xxxx)b
ATTRIB (Type B only)	(00011101)b
HLTA	(01010000)b
HLTB	(01010000)b

Definitions made in this part of ISO/IEC 14443:

RATS	(11100000)b
PPS	(1101xxxx)b
I-block	(00xxxxxx)b (not (00xxx101)b)
R-block	(10xxxxxx)b (not (1001xxxx)b)
S-block	(11xxxxxx)b (not (1110xxxx)b and not (1101xxxx)b)

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The following table describes the first byte of the defined block and frame coding.

Table C.1 — Block and frame coding

Bit	I-block PCB	R-block PCB	S-block PCB DESELECT	S-block PCB WTX	REQB / WUPB	Slot-MARKER	SELECT	ATTRIB	HLTA	HLTB	RATS	PPS
b8	0	1	1		0	X	1	0	0	0	1	1
b7	0	0	1		0	X	0	0	1	1	1	1
b6	0 (RFU)	1	0	1	0	X	0	0	0	0	1	0
b5	Chaining	ACK/NAK	0	1	0	X	1	1	1	1	0	1
b4	CID	CID	CID		0	0	X	1	0	0	0	X
b3	NAD	0 (no NAD)	0 (no NAD)		1	1	X	1	0	0	0	X
b2	1	1 (RFU)	1 (RFU)		0	0	X	0	0	0	0	X
b1	Block number	Block number	0 (RFU)		1	1	X	1	0	0	0	X

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[4] ISO/IEC 10536-2, *Identification cards — Contactless integrated circuit(s) cards — Part 2: Dimensions and location of coupling areas*

[5] ISO/IEC 10536-3, *Identification cards — Contactless integrated circuit(s) cards — Part 3: Electronic signals and reset procedures*

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[7] ISO/IEC 18092, *Information technology — Telecommunications and information exchange between systems — Near Field Communication — Interface and Protocol (NFCIP-1)*

[8] ISO/IEC 21481, *Information technology — Telecommunications and information exchange between systems — Near Field Communication Interface and Protocol -2 (NFCIP-2)*

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