C37.118™

IEEE Standard for Synchrophasors for Power Systems

IEEE Power Engineering Society

Sponsored by the
Power System Relaying Committee

IEEE
3 Park Avenue
New York, NY 10016-5997, USA

22 March 2006

IEEE Std C37.118™-2005
(Revision of
IEEE Std 1344™-1995)

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Recognized as an
American National Standard (ANSI)

IEEE Std C37.118™-2005
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IEEE Standard for Synchrophasors for Power Systems

Sponsor

Power System Relaying Committee
of the
IEEE Power Engineering Society

Approved 1 February 2006

American National Standards Institute

Approved 21 October 2005

IEEE-SA Standards Board

Abstract: This standard defines synchronized phasor measurements used in power system applications. It provides a method to quantify the measurement, tests to be sure the measurement conforms to the definition, and error limits for the test. It also defines a data communication protocol, including message formats for communicating this data in a real-time system. Explanation, examples, and supporting information are also provided.
Keywords: data concentrator, DC, GPS synchronization, IRIG, PDC, phasor, phasor measurement, phasor measurement unit, PMU, synchrophasor, total vector error, TVE

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Introduction

This introduction is not part of IEEE Std C37.118-2005, IEEE Standard for Synchrophasors for Power Systems.

The synchrophasor standard has been completely revised. The original standard was IEEE Std 1344-1995, which was reaffirmed in 2001. A working group was established in January 2001 to update the standard. This new synchrophasor standard, IEEE Std C37.118-2005, replaces the original.

Digital computer based measurement, protection, and control systems have become common features of electric power substations. These systems use sampled data to compute various quantities, such as voltage and current phasors. Phasors are used in many protection and data acquisition functions, and their utility is increased further by referencing them to a common time base. This can be accomplished by synchronizing the signal input processes at various measuring sites. Simultaneous measurement sets derived from synchronized phasors provide a vastly improved method for tracking power system dynamic phenomena for improved power system monitoring, protection, operation, and control.

In this standard, additional clarification is provided for the phasor and synchronized phasor definitions. The concepts of total vector error (TVE) and compliance tests have been introduced. The message formats have been updated from the original standard to improve information exchange with other systems, such as a master station. Specifically, the sync, frame size, and station identification fields have been added to the data frame, configuration frame, header frame, and command frame. The CRC-CCITT is the only valid check word. In the data frame, analog data can now be included, the fraction of second field has replaced the sample count field, and the status field has been significantly modified to include time quality.

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IEEE Standard for Synchrophasors for Power Systems

1. Overview

This standard covers synchronized phasor measurements used in electric power systems. It defines the measurement, provides a method of quantifying the measurements, and quality test specifications. It also defines data transmission formats for real-time data reporting. Clause 1 provides the scope and needs for the standard. Clause 2 references other standards that are related or may be useful in the study and application of this standard. Clause 3 defines terms and acronyms found in this standard. Clause 4 defines the measurement. Clause 5 defines measurement requirements, a method of quantifying the measurement, a test method, and accuracy limits. Clause 6 defines the real-time communication protocol and message formats.

Eight informative annexes are provided to clarify the standard and give supporting information. Annex A is a bibliography. Annex B gives information about cyclic redundancy check (CRC) codes and the CRC required by this standard. Annex C explores the effects of timetagging and transient response relevant to this measurement technique. Annex D illustrates the message formats defined in Clause 6 with complete message examples. Annex E provides background on time synchronization sources needed for this measurement. Annex F discusses time synchronization. Annex G provides examples of tests that can be made to characterize these measurements. Annex H explains the total vector error (TVE) concept of measurement quality and gives plots of error results. Annex I defines message mapping into standard communication protocols.

1.1 Scope

This is a standard for synchronized phasor measurement systems in power systems. It addresses the definition of a synchronized phasor, time synchronization, application of timetags, method to verify measurement compliance with the standard, and message formats for communication with a phasor measurement unit (PMU). In this context, a PMU can be a stand-alone physical unit or a functional unit within another physical unit. This standard does not specify limits to measurement response time, accuracy under transient conditions, hardware, software, or a method for computing phasors.

1.2 Purpose

This standard defines synchronized phasor measurements in substations so that the measurement equipment can be readily interfaced with associated systems. It specifies data formats and synchronization requirements to allow correlating phasors from various sources and compares them with similar data from different measurement systems.

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1.3 Need for this standard

Recent developments in the field of power system data acquisition provide users with the ability to calculate power system phasor quantities in real time. Different hardware and software approaches are being implemented to record, transmit, and analyze these measurements, both in real time and post event. A standard is needed for integrating measurement systems into power system environments, to specify data output formats, and to ensure that the measurement processes are producing comparable results. The synchrophasor standard will help ensure maximum benefits from the phasor measurements and allow interchange of data between a wide variety of systems for users of both real-time and off-line phasor measurements.

2. Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

IEEE Std 754™, IEEE Standard for Binary Floating-Point Arithmetic.[1, 2]

IEEE Std 1588™, IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems.

IRIG Standard 200, IRIG Serial Time Code Formats, Telecommunications and Timing Group, Range Commanders Council, U.S. Army White Sands Missile Range.[3]

3. Definitions, acronyms, and abbreviations

3.1 Definitions

For the purpose of this document, the following terms and definitions apply. *The Authoritative Dictionary of IEEE Standard Terms* [B4][4] should be referenced for terms not defined in this subclause.

3.1.1 anti-aliasing: The process of filtering a signal when converting to a sampled form to remove the components of that signal whose frequency is equal to or greater than one-half the Nyquist rate (sample rate). If not removed, these signal components would appear as a lower frequency component (an alias).

3.1.2 IEEE floating point: A 32-bit representation of a real number in accordance with IEEE Std 754.

3.1.3 Nyquist rate: A rate that is twice the highest frequency component in the input analog signal. The analog signal must be sampled at a rate greater than the Nyquist rate to be represented accurately in digital form.

3.1.4 phasor: A complex equivalent of a simple cosine wave quantity such that the complex modulus is the cosine wave amplitude and the complex angle (in polar form) is the cosine wave phase angle.

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[3]This standard is available at http://www.jcte.jcs.mil/RCC/manuals/200-04/TT-45.pdf.

[4]The numbers in brackets correspond to those of the bibliography in Annex A.

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3.1.5 synchronism: The state where connected alternating-current systems, machines, or a combination operate at the same frequency and where the phase-angle displacements between voltages in them are constant or vary about a steady and stable average value.

3.1.6 synchronized phasor: A phasor calculated from data samples using a standard time signal as the reference for the measurement. Synchronized phasors from remote sites have a defined common phase relationship. *Syn:* **synchrophasor.**

3.2 Acronyms and abbreviations

BCD	binary coded decimal
C/A code	coarse acquisition code
CRC-CCITT	16-bit cyclic redundancy check[5]
DC	data concentrator
DoD	U.S. Department of Defense
DoT	U.S. Department of Transportation
FRP	Federal Radionavigation Plan
GALILEO	Proposed European radionavigation system
GLONASS	Russian satellite-based radionavigation system
GOES	Geostationary Operational Environmental Satellite.
GPS	Global Positioning System
INMARSAT	International Maritime Satellite System
IRIG-B	InterRange Instrumentation Group Time Code Format B
Loran C	LOng RANge navigation system
NTP	network time protocol
PDC	phasor data concentrator
PMU	phasor measurement unit
PPS	pulse per second
ROM	read-only memory
rms	root-mean-square
SA	selective availability

[5]The CRC-CCITT is calculated using the generating polynomial $X^{16} + X^{12} + X^5 + 1$, seed value 0xFFFF (–1), no final mask.

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SBS	straight binary second
SCADA	Supervisory Control and Data Acquisition
SMPCNT	sample count
SOC	second of century
THD	total harmonic distortion
TVE	total vector error
UTC	Universal time coordinated
WWV	U.S. National Institute of Standards and Technology (NIST) time broadcast radio station

4. Synchrophasor measurement

4.1 Phasor definition

The pure sinusoidal waveform $x(t) = X_m \cos(\omega t + \phi)$ is commonly represented as a phasor $\boldsymbol{X} = X_r + jX_i = (X_m/\sqrt{2})(e^{j\phi})$, where ϕ depends on the definition of the time scale. For this standard, this basic concept is adapted as the representation of power system sinusoidal signals.

4.1.1 Off-nominal frequency signals

The phasor representation of a sinusoid is independent of its frequency. A sinusoid $x(t) = X_m \cos(2\pi f t + \phi)$ has a phasor representation $\boldsymbol{X} = (X_m/\sqrt{2})\, e^{j\phi}$. The phase angle ϕ of the phasor is determined by the starting time ($t = 0$) of the sinusoid.

Consider that such a sinusoid is observed at intervals $\{0, T_0, 2T_0, 3T_0, ..., nT_0, ...\}$, leading to corresponding phasor representations $\{\boldsymbol{X_0, X_1, X_2, X_3, \ldots}\}$. This is equivalent to having the time reference for observation initialized at the beginning of each interval.

If the observation interval T_0 is equal to an integer multiple of the period of the sinusoid $T = 1/f$, then a constant phasor is obtained at each observation. On the other hand, if the observation interval T_0 is not an integer multiple of T, the observed phasor has a constant magnitude, but the phase angles of the sequence of phasors $\{\boldsymbol{X_0, X_1, X_2, X_3, \ldots}\}$ will change uniformly at a rate $2\pi(f - f_0)T_0$, where $f_0 = 1/T_0$. This is illustrated in Figure 1.

4.2 Synchrophasor definition

The synchrophasor representation $\boldsymbol{X}$ of a signal $x(t)$ is the complex value given by Equation (1):

$$X = X_r + jX_i \tag{1}$$

$$= (X_m/\sqrt{2})e^{j\phi}$$

$$= X_m/\sqrt{2}\,(\cos\phi + j\sin\phi)$$

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where $X_m/\sqrt{2}$ is the rms value of the signal $x(t)$ and ϕ is its instantaneous phase angle relative to a cosine function at nominal system frequency synchronized to Universal time coordinated (UTC). This angle is defined to be 0° when the maximum of $x(t)$ occurs at the UTC second rollover [1 pulse per second (PPS) time signal], and –90° when the positive zero crossing occurs at the UTC second rollover. Figure 2 illustrates this relationship.

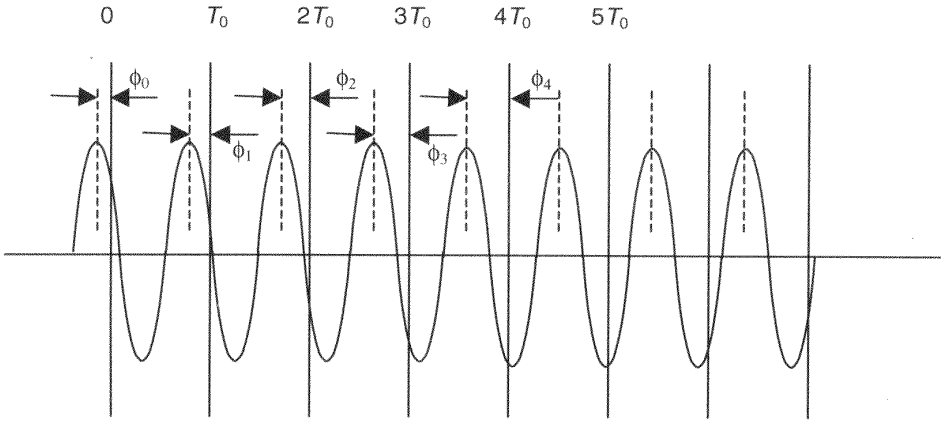

Figure 1—A sinusoid with a period of *T* observed at instants that are multiples of T_0 apart. T_0 is not an integer multiple of *T*.

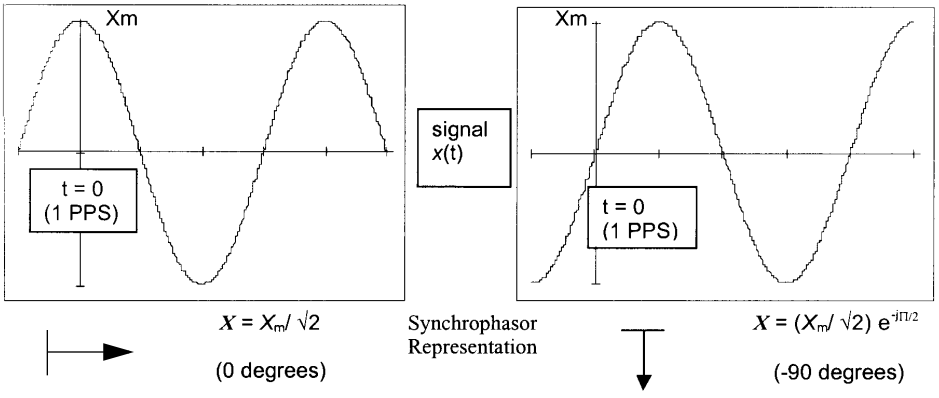

Figure 2—Convention for synchrophasor representation

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4.3 Measurement timetag for synchrophasors

Synchrophasor measurements shall be tagged with the UTC time corresponding to the time of measurement. This shall consist of three numbers: a second-of-century (SOC) count, a fraction-of-second count, and a time status value. The SOC count shall be a 4-byte binary count in seconds from midnight (00:00) of January 1, 1970, to the current second. Leap seconds shall be added to or deleted from this count as necessary to keep it synchronized with UTC. Insertion of a leap second results in two successive seconds having the same SOC count which are differentiated by the leap second bit in the FRACSEC word defined in 6.2.1. (With this convention, time count can always be determined from current time by multiplying the number of days since 1/1/70 by the number of seconds per day, 86 400). This SOC time stamp is the same as is used by the UNIX computer system, and similar to those used by other computer systems including DOS, MAC OS, and networks [network time protocol (NTP)].

The second shall be divided into an integer number of subdivisions by the TIME_BASE integer specified in Table 10. The fraction-of-second count shall be an integer representing the numerator of the fraction of second with TIME_BASE as the denominator. Compatibility with IEC 61850:2000 [B3] requires a TIME_BASE value of 2^24. The fraction-of-second count shall be 0 when it coincides with the 1 s rollover. This timetag shall be applied to all communication frames as described in Clause 6.

4.4 System time synchronization

Synchrophasor measurements shall be synchronized to UTC time with accuracy sufficient to meet the accuracy requirements of this standard (see 5.2). Note that a time error of 1 μs corresponds to a phase error of 0.022° for a 60 Hz system and 0.018° for a 50 Hz system. A phase error of 0.01 radian or 0.57° will by itself cause 1% TVE as defined in Equation (2). This corresponds to a maximum time error of ± 26 μs for a 60 Hz system, and ± 31 μs for a 50 Hz system.

The system must be capable of receiving time from a highly reliable source, such as the Global Positioning System (GPS), which can provide sufficient time accuracy to keep the TVE within the required limits and provide indication of loss of synchronization. The flag in the data output (see Table 8, STAT word Bit 13) is provided to indicate that a loss of time synchronization shall be asserted when loss of synchronization could cause the TVE to exceed the limit or within 1 min of actual loss of synchronization, whichever is less. The flag shall remain set until data acquisition is resynchronized to the required accuracy level.

Annex E and Annex F discuss time sources and distribution formats.

5. Synchrophasor measurement requirements and compliance verification

5.1 Synchrophasor estimation

Synchrophasor estimates shall be made and transmitted as data frames at a rate F_s that is an integer number of times per second or integer number of seconds per frame as specified by the DATA_RATE variable in the configuration frame (see Table 10). These estimates shall be equally spaced within the 1 s interval. Data frames may include multiple channels of phasor estimates, analog words, and digital words combined with a single timetag as defined in Clause 6.

5.1.1 Reporting rates

The PMU shall support data reporting (by recording or output) at submultiples of the nominal power-line (system) frequency. Required rates for 50 Hz and 60 Hz systems are listed in Table 1.

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Table 1—Required PMU reporting rates

System frequency	50 Hz		60 Hz				
Reporting rates (F_s—frames per second)	10	25	10	12	15	20	30

The actual rate to be used shall be user selectable. Inclusion of more rates, particularly up to system frequency is encouraged.

5.1.2 Reporting times

For a reporting rate N frames per second, the reporting times shall be evenly spaced through each second with frame number 0 (numbered 0 through N–1) coincident with the UTC second rollover (usually the 1 PPS provided by GPS). These reporting times (timetags) are to be used for determining the instantaneous values of the synchrophasor as defined in 4.2. This is illustrated in Figure 1, where the reporting times are at 0, T_0, $2T_0$, $3T_0$, $4T_0$, etc.

5.1.3 Example results

Table 2 gives the synchrophasor values as defined in Equation (1) for the waveforms shown in Figure 2. The values are derived for a 10 frame-per-second reporting rate with a system frequency of 60 Hz. Synchrophasor values are shown for base phase angles of 0° and –90° at the 1 PPS time mark as shown in Figure 2 for both 60 Hz and 61 Hz signals. The synchrophasor values at 50 Hz and 51 Hz for a 50 Hz system frequency are identical.

5.1.4 PMU response time

The PMU response time will be measured by applying a positive or negative 10% step in magnitude with the input signal at nominal magnitude and rated frequency. The response time is the interval of time between the instant the step change is applied and the timetag of the first phasor measurement for which the TVE enters and stays in the specified accuracy zone corresponding to the compliance level (1%).

5.2 Accuracy limits

Under the conditions where X_m, ω, and ϕ are fixed, and for the influence conditions shown in Table 3, the TVE shall not exceed the TVE limit given in Table 3 for the given compliance level.

TVE is defined as shown in Equation (2):

$$TVE = \sqrt{\frac{(X_r(n) - X_r)^2 + (X_i(n) - X_i)^2}{X_r^2 + X_i^2}} \quad (2)$$

where $X_r(n)$ and $X_i(n)$ are the measured values, given by the measuring device, and X_r and X_i are the theoretical values of the input signal at the instant of time of measurement, determined from Equation (1) and the known conditions of X_m, ω, and ϕ.

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Table 2—Table of synchrophasor values for 60 Hz system at a 10 frame-per-second reporting rate

Time	Fractional time		Synchrophasor—60 Hz		Synchrophasor—61 Hz	
Second	Frame number	Fractional second	Synchro-phasor (0°)	Synchro-phasor (–90°)	Synchro-phasor (0°)	Synchro-phasor (–90°)
k–1	9	0.900000	$X_m/\sqrt{2}, \angle 0^\circ$	$X_m/\sqrt{2}, \angle -90^\circ$	$X_m/\sqrt{2}, \angle -36^\circ$	$X_m/\sqrt{2}, \angle -126^\circ$
k	0	0.000000	$X_m/\sqrt{2}, \angle 0^\circ$	$X_m/\sqrt{2}, \angle -90^\circ$	$X_m/\sqrt{2}, \angle 0^\circ$	$X_m/\sqrt{2}, \angle -90^\circ$
k	1	0.100000	$X_m/\sqrt{2}, \angle 0^\circ$	$X_m/\sqrt{2}, \angle -90^\circ$	$X_m/\sqrt{2}, \angle 36^\circ$	$X_m/\sqrt{2}, \angle -54^\circ$
k	2	0.200000	$X_m/\sqrt{2}, \angle 0^\circ$	$X_m/\sqrt{2}, \angle -90^\circ$	$X_m/\sqrt{2}, \angle 72^\circ$	$X_m/\sqrt{2}, \angle -18^\circ$
k	3	0.300000	$X_m/\sqrt{2}, \angle 0^\circ$	$X_m/\sqrt{2}, \angle -90^\circ$	$X_m/\sqrt{2}, \angle 108^\circ$	$X_m/\sqrt{2}, \angle 18^\circ$
k	4	0.400000	$X_m/\sqrt{2}, \angle 0^\circ$	$X_m/\sqrt{2}, \angle -90^\circ$	$X_m/\sqrt{2}, \angle 144^\circ$	$X_m/\sqrt{2}, \angle 54^\circ$
k	5	0.500000	$X_m/\sqrt{2}, \angle 0^\circ$	$X_m/\sqrt{2}, \angle -90^\circ$	$X_m/\sqrt{2}, \angle 180^\circ$	$X_m/\sqrt{2}, \angle 90^\circ$
k	6	0.600000	$X_m/\sqrt{2}, \angle 0^\circ$	$X_m/\sqrt{2}, \angle -90^\circ$	$X_m/\sqrt{2}, \angle -144^\circ$	$X_m/\sqrt{2}, \angle 126^\circ$
k	7	0.700000	$X_m/\sqrt{2}, \angle 0^\circ$	$X_m/\sqrt{2}, \angle -90^\circ$	$X_m/\sqrt{2}, \angle -108^\circ$	$X_m/\sqrt{2}, \angle 162^\circ$
k	8	0.800000	$X_m/\sqrt{2}, \angle 0^\circ$	$X_m/\sqrt{2}, \angle -90^\circ$	$X_m/\sqrt{2}, \angle -72^\circ$	$X_m/\sqrt{2}, \angle -162^\circ$
k	9	0.900000	$X_m/\sqrt{2}, \angle 0^\circ$	$X_m/\sqrt{2}, \angle -90^\circ$	$X_m/\sqrt{2}, \angle -36^\circ$	$X_m/\sqrt{2}, \angle -126^\circ$
k+1	0	0.000000	$X_m/\sqrt{2}, \angle 0^\circ$	$X_m/\sqrt{2}, \angle -90^\circ$	$X_m/\sqrt{2}, \angle 0^\circ$	$X_m/\sqrt{2}, \angle -90^\circ$

When the input signal frequency is exactly equal to rated, the phasor will be time-invariant and its coordinates will be fixed and determined by the signal phase. When the input signal frequency is not equal to rated, the phasor will undergo a rotation in the complex plane as illustrated in Table 2. TVE is the magnitude of the vector difference between the theoretical phasor defined in Equation (1) and the phasor estimate given by the measuring device, expressed as a fraction of the magnitude of the theoretical phasor as shown in Equation (2).

5.3 Compliance verification

Compliance tests shall be performed by comparing the phasor estimates obtained under steady-state conditions to the corresponding theoretical values of X_r and X_i and calculating TVE, as defined in Equation (2). *Steady-state conditions* are where X_m, ω, and ϕ of the test signal, and all other influence quantities are fixed for the period of the measurement. (Note that for off-nominal frequencies, the measured phase angle will change even though the test signal phase ϕ is constant.)

A calibration device used to verify performance in accordance with this subclause shall be traceable to national standards and have a “test accuracy ratio” of at least four compared with these test requirements (for example, provide a TVE measurement within 0.25% where TVE is 1%). In cases where there is no national standard available for establishing traceability, a detailed error analysis shall be performed to demonstrate compliance with these requirements.

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All compliance tests are to be performed under steady-state conditions, with reference conditions and influence quantities as defined in Table 3. Effects of the influence quantities shall be considered cumulative, and the TVE shall not exceed the error listed for the given compliance level under any combination of influence quantities shown in Table 3. To evaluate compliance with this requirement, the effects of the influence quantities may be separately evaluated.

Documentation shall be provided by any vendor claiming compliance with this standard that shall include a statement of the compliance level being achieved and demonstrating this performance. In addition, if the verification system is based on an error analysis as called for previously, this analysis shall be provided as well.

Table 3—Influence quantities and allowable error limits for compliance levels 0–1

Influence quantity	Reference condition	Range of influence quantity change with respect to reference and maximum allowable TVE in percent (%) for each compliance level			
		Level 0		Level 1	
		Range	TVE (%)	Range	TVE (%)
Signal frequency	$F_{nominal}$	± 0.5 Hz	1	± 5 Hz	1
Signal magnitude	100% rated	80% to 120% rated	1	10% to 120% rated	1
Phase angle	0 radians	± π radians	1	± π radians	1
Harmonic distortion	<0.2% (THD)	1%, any harmonic up to 50th	1	10%, any harmonic up to 50th	1
Out-of-band interfering signal, at frequency f_i where $\|f_i - f_0\| > F_s/2$, F_s = phasor reporting rate, $f_0 = F_{nominal}$	<0.2% of input signal magnitude	1.0% of input signal magnitude	1	10% of input signal magnitude	1

NOTE 1—The required level of compliance shall be determined by the user. Level 1 is intended as the "standard" compliance level; level 0 is provided for applications with requirements that cannot be served with level 1.[6]

NOTE 2—The reference condition specifies the condition for that quantity when not being varied. For example, when testing signal magnitude, the magnitude will be varied but the frequency will be nominal, the phase-angle 0 radians, the harmonic distortion <0.2%, and all out-of-band interfering signals < 0.2%. The TVE must stay within the specified error range during all tests.

NOTE 3—An out-of-band interfering signal is any signal with frequency outside the frequency range determined as shown from the nominal system frequency and the phasor reporting rate. The test specified in 5.3 demonstrates the effectiveness of the PMU anti-aliasing filter. The test signal should include those frequencies outside of the bandwidth specified above which cause the greatest TVE.

NOTE 4—PMUs that are not compensated for group delay or other deficiencies are not likely to meet TVE compliance requirements (see Annex C).

NOTE 5—This standard does not impose any limitations to the use of PMUs under any conditions. PMUs are actually very good for making measurements under many transient conditions, and there have been many publications documenting this. The standard does not address the accuracy and response time under transient conditions, and so all testing is

[6]Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

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restricted to steady-state conditions. The problem with including transient performance requirements comes in stating requirements that are measurable, can be uniformly applied, and are not unduly restrictive on implementations. This is still an emerging technology and applying anticipated performance requirements could hamper development. Harmonizing a common set of dynamic performance requirements should be undertaken once the range of implementations and measurement applications has been more fully explored. At this time, dynamic performance under transient conditions should be specified and verified by the users to meet their application needs.

6. Synchrophasor message format

6.1 Message application

This subclause describes the format of messages to and from a PMU for use in real-time communication of phasor data. *Real-time data transmission* is defined here as taking place concurrently with the measurement process. If the PMU device is to be used with other systems where the phasor data information is to be transmitted in real time, implementation of this protocol is required for conformance with this standard. If the PMU device is used only for phasor data archiving or recording, then this protocol is not required. Implementation of additional protocols for phasor data communication is not restricted.

Any communication system or media may be used for data transmission. The message frames shall be transmitted in their entirety as they are specified. When used with a stacked protocol such as fieldbus message specification (FMS) or Internet protocol (IP), the entire frame including sync and CRC-CCITT shall be written into and read from the application layer interface. When used with more direct systems like raw Ethernet or RS-232, the entire frame will also be sent with the CRC-CCITT assuring data integrity.

This message protocol may be used for communication with a single PMU or a secondary system that receives data from several PMUs. The secondary system, here referred to as a data concentrator (DC, also called a *phasor data concentrator* or PDC in some references), shall have its own user assigned ID code. The protocol allows for necessary identifying information, such as the PMU IDCODE and status, to be imbedded in the data frame for proper interpretation of the measured data.

6.2 Message framework

Four message types are defined here: data, configuration, header, and command. The first three message types are transmitted from the PMU/DC and the last (command) is received by the PMU/DC. Data messages are the measurements made by a PMU. Configuration is a machine-readable message describing the data the PMU/DC sends and providing calibration factors. Header information is human-readable descriptive information sent from the PMU/DC but provided by the user. Commands are machine-readable codes sent to the PMU/DC for control or configuration. Information may be stored in any convenient form in the PMU/DC itself, but when transmitted it shall be formatted as frames described in the following subclauses.

Only data, configuration, header, and command frames are defined in this standard. Other types may be designated in the future. In normal operation, the PMU only sends data frames. Annex D contains examples of data, configuration, and command frames.

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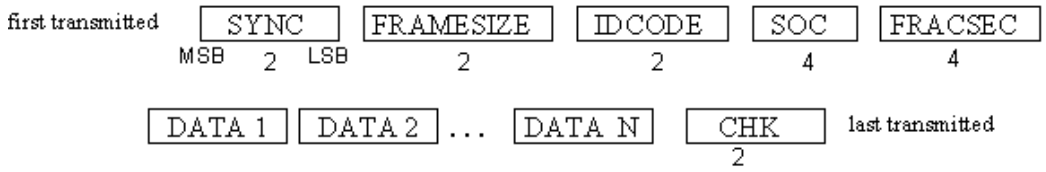

Figure 3—Example of frame transmission order

6.2.1 Overall message

All message frames start with a 2-byte SYNC word followed by a 2-byte FRAMESIZE word, a 2-byte IDCODE, and a time stamp consisting of a 4-byte SOC and 4-byte fraction of second (FRACSEC), which includes a 24-bit fraction-of-second integer and an 8-bit Time Quality flag described in 6.2.2. The SYNC word provides synchronization and frame identification. IDCODE positively identifies the unit sending or receiving the message. Bits 4–6 in the SYNC word designate the frame type. This word is detailed Table 4. All frames terminate in check word (CHK), which is a CRC-CCITT. This CRC-CCITT uses the generating polynomial $X^{16} + X^{12} + X^5 + 1$ with an initial value of –1 (hex FFFF) and no final mask. All frames are transmitted exactly as described with no delimiters. Figure 3 illustrates frame transmission order. The SYNC word is transmitted first and check word last. Two- and 4-byte words are transmitted most significant byte first (network or "big endian" order). All frame types use this same order and format. This first published edition of this standard shall be designated version 1 (binary 0001).

6.2.2 Time and Time Quality

The 32-bit (4-byte) FRACSEC is divided into two components: a 24-bit integer that is the actual Fraction-of-Second count and an 8-bit Time Quality flag. The time of measurement or data transmission for non-data frames is the SOC time stamp that fixes the integer second plus the fractional time. The fractional time is determined by dividing the 24-bit integer fraction of second by the TIME_BASE integer given in configuration frame, as shown in Equation (3):

$$\text{Time} = \text{SOC} + \text{Fraction-of-Second} / \text{TIME_BASE} \quad (3)$$

The bits of the Time Quality flag indicate the "quality" of the time being reported as well as indication of Leap Second status. Table 5 details these assignments. Bit 7 is reserved for future use. Bit 4 is the Leap Second Pending bit and shall be set as soon as it is known but no less than 1 s or more than 59 s before a leap second occurs. It shall be cleared in the first second after the leap second occurs. Bit 5 is the Leap Second Occurred bit and shall be set in the first second after the missing second and remains set for 24 h afterward. Bit 6 is the Leap Second Direction bit that is 0 for adding a leap second and 1 for deleting a leap second. It shall be set (to 0 or 1 as required) at the same time or before the leap second pending bit is set and remain the same for at least 24 h afterward. This will allow analysis programs to factor in a ± Leap Second in any analysis or time difference calculation.

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Table 4—Word definitions common to all frame types

Field	Size (bytes)	Comments
SYNC	2	Frame synchronization word. Leading byte: AA hex Second byte: Frame type and Version, divided as follows: Bit 7: Reserved for future definition Bits 6–4: 000: Data Frame 001: Header Frame 010: Configuration Frame 1 011: Configuration Frame 2 100: Command Frame (received message) Bits 3–0: Version number, in binary (1–15), version 1 for this initial publication.
FRAMESIZE	2	Total number of bytes in the frame, including CHK. 16-bit unsigned number. Range = maximum 65535.
IDCODE	2	PMU/DC ID number, 16-bit integer, assigned by user, 1 to 65 534 (0 and 65 535 are reserved). Identifies device sending and receiving messages.
SOC	4	Time stamp, 32-bit unsigned number, SOC count starting at midnight 01-Jan-1970 (UNIX time base). Ranges 136 yr, rolls over 2106 AD. Leap seconds are not included in count, so each year has the same number of seconds except leap years, which have an extra day (86 400 s).
FRACSEC	4	Fraction of Second and Time Quality, time of measurement for data frames or time of frame transmission for non-data frames. Bits 31–24: Time Quality as defined in 6.2.2. Bits 23–00: Fraction-of-second, 24-bit integer number. When divided by TIME_BASE yields the actual fractional second. FRACSEC used in all messages to and from a given PMU shall use the same TIME_BASE that is provided in the configuration message from that PMU.
CHK	2	CRC-CCITT, 16-bit unsigned integer.

Table 5—Time Quality flag bit definitions

Bit #	Description
7	Reserved.
6	Leap second direction—0 for add, 1 for delete.
5	Leap second occurred—Set in the first second after the leap second occurs and remains set for 24 h.
4	Leap Second Pending—Set before a leap second occurs and cleared in the second after the leap second occurs.
3–0	Time Quality indicator code—See Table 6.

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The Time Quality indicator code contained in the lowest 4 bits indicates the maximum time error as determined by the PMU clock function. Bits 0–3 shall be all cleared to 0 when the time function is locked onto its source (e.g., locked onto a satellite in the case of a GPS clock). Bits 0–3 shall be all set to 1 when there is either a clock error or the clock has never been initially set. Conditions of accuracy between these extremes are defined in Table 6. This table is the same as Table F.2, which details time and synchronization methods.

Table 6—Four-bit Time Quality indicator code

Binary	Hex	Value (worst-case accuracy)
1111	F	Fault—Clock failure, time not reliable
1011	B	Clock unlocked, time within 10 s
1010	A	Clock unlocked, time within 1 s
1001	9	Clock unlocked, time within 10^{-1} s
1000	8	Clock unlocked, time within 10^{-2} s
0111	7	Clock unlocked, time within 10^{-3} s
0110	6	Clock unlocked, time within 10^{-4} s
0101	5	Clock unlocked, time within 10^{-5} s
0100	4	Clock unlocked, time within 10^{-6} s
0011	3	Clock unlocked, time within 10^{-7} s
0010	2	Clock unlocked, time within 10^{-8} s
0001	1	Clock unlocked, time within 10^{-9} s
0000	0	Normal operation, clock locked

6.2.3 Leap second bit timing examples

The following examples show how the time count and leap second bits will actually appear for both a positive (added) leap second and a negative (deleted) leap second. The direction bit can be at any state before the Leap Second Pending bit is set and after the leap Second Occurred bit clears. When either of these bits is set, the direction bit shall be set in the state properly indicating insertion or deletion. The pending bit shall be set as soon as a leap second occurrence is known but not more than 59 s or less than 1 s before the change will occur.

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Added leap second:

SOC time	Time of day	Direction bit 6	Occurred bit 5	Pending bit 4	Comments
1114991939	23:58:59	X	0	0	Direction bit any state before pending.
1114991940	23:59:00	0	0	1	Pending can be set no earlier than here.
1114991941	23:59:01	0	0	1	
. . . . .					
1114991998	23:59:58	0	0	1	
1114991999	23:59:59	0	0	1	Pending and direction shall be set by here.
1114992000	23:59:60	0	0	1	Leap second occurs here.
1114992000	00:00:00	0	1	0	Occurred and direction remain set.
1114992001	00:00:01	0	1	0	
. . . . .					
1115078399	23:59:59	0	0	0	
1115078400	00:00:00	X	0	0	Occurred cleared, direction don't care.
. . . . .					

Deleted leap second:

SOC time	Time of day	Direction bit 6	Occurred bit 5	Pending bit 4	Comments
1114991939	23:58:59	X	0	0	Direction bit any state before pending.
1114991940	23:59:00	1	0	1	Pending can be set no earlier than here.
1114991941	23:59:01	1	0	1	
. . . . .					
1114991997	23:59:57	1	0	1	
1114991998	23:59:58	1	0	1	Pending and direction shall be set by here.
1114992000	00:00:00	1	1	0	Leap second occurs here.
1114992001	00:00:01	1	1	0	Occurred and direction remain set.
1114992002	00:00:02	1	1	0	
. . . . .					
1115078399	23:59:59	1	0	0	
1115078400	00:00:00	X	0	0	Occurred cleared, direction don't care.
. . . . .					

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6.3 Data frame

A data frame shall contain measured data and shall be identified by having Bits 4–6 in the SYNC word set to zero as shown in Table 4. The real-time phasor data frame shall consist of binary data ordered as shown in Table 7, and described in detail in Table 8. All fields shall be fixed length as described, and no delimiters shall be used. The frame starts with SYNC, FRAMESIZE, IDCODE, and SOC, and terminates with a CRC-CCITT as shown in 6.2.

Table 7—Data frame organization

No.	Field	Size (bytes)	Comment
1	SYNC	2	Sync byte followed by frame type and version number.
2	FRAMESIZE	2	Number of bytes in frame, defined in 6.2.
3	IDCODE	2	PMU/DC ID number, 16-bit integer, defined in 6.2.
4	SOC	4	SOC time stamp, defined in 6.2, for all measurements in frame.
5	FRACSEC	4	Fraction of Second and Time Quality, defined in 6.2, for all measurements in frame.
6	STAT	2	Bitmapped flags.
7	PHASORS	4 × PHNMR or 8 × PHNMR	Phasor estimates as defined in Clause 5. May be single-phase or 3-phase positive, negative, or zero sequence. Values are 4 or 8 bytes each depending on the fixed 16-bit or floating-point format used, as indicated by the configuration frame.
8	FREQ	2 / 4	Frequency (fixed or floating point).
9	DFREQ	2 / 4	Rate of change of frequency (fixed or floating point).
10	ANALOG	2 × ANNMR or 4 × ANNMR	Analog data, 2 or 4 bytes per value depending on fixed- or floating-point format used, as indicated by the configuration frame.
11	DIGITAL	2 × DGNMR	Digital data, usually representing 16 digital status points (channels).
	Repeat 6–11		Fields 6–11 are repeated for as many PMUs as in NUM_PMU field in configuration frame.
12+	CHK	2	CRC-CCITT

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Table 8—Word definitions unique to data frames

Field	Size (bytes)	Comments
STAT	2	Bitmapped flags. Bit 15: Data valid, 0 when PMU data is valid, 1 when invalid or PMU is in test mode. Bit 14: PMU error including configuration error, 0 when no error. Bit 13: PMU sync, 0 when in sync. Bit 12: Data sorting, 0 by time stamp, 1 by arrival. Bit 11: PMU trigger detected, 0 when no trigger. Bit 10: Configuration changed, set to 1 for 1 min when configuration changed. Bits 09–06: Reserved for security, presently set to 0. Bits 05–04: Unlocked time: 00 = sync locked, best quality 01 = Unlocked for 10 s 10 = Unlocked for 100 s 11 = Unlocked over 1000 s Bits 03–00: Trigger reason: 1111–1000: Available for user definition 0111: Digital 0110: Reserved 0101: *df/dt* high 0100: Frequency high/low 0011: Phase-angle diff 0010: Magnitude high 0001: Magnitude low 0000: Manual
PHASORS	4 / 8	16-bit integer values: Rectangular format: — Real and imaginary, real value first — 16-bit signed integers, range –32 767 to +32 767 Polar format: — Magnitude and angle, magnitude first — Magnitude 16-bit unsigned integer range 0 to 65 535 — Angle 16-bit signed integer, in radians × 10^4, range –31 416 to +31 416 32-bit values in IEEE floating-point format: Rectangular format: — Real and imaginary, in engineering units, real value first Polar format: — Magnitude and angle, magnitude first and in engineering units — Angle in radians, range –π to +π
FREQ	2 / 4	Frequency deviation from nominal, in millihertz (mHz) Range—nominal (50 Hz or 60 Hz) –32.767 to +32.767 Hz 16-bit integer or 32-bit floating point. 16-bit integer:16-bit signed integers, range –32 767 to +32 767. 32-bit floating point: actual frequency value in IEEE floating-point format.
DFREQ	2 / 4	Rate-of-change of frequency, in Hz per second times 100 Range –327.67 to +327.67 Hz per second Can be 16-bit integer or IEEE floating point, same as FREQ above.
ANALOG	2 / 4	Analog word. 16-bit integer. It could be sampled data such as control signal or transducer value. Values and ranges defined by user. Can be 16-bit integer or IEEE floating point.
DIGITAL	2	Digital status word. It could be bitmapped status or flag. Values and ranges defined by user.

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6.3.1 Explanation for STAT word in the data frame

The data frame consists of time and data sections with framing. The data can be one block from a single PMU or multiple blocks from multiple PMUs. Each PMU data block is headed by a STAT word that has complete status for that block; this STAT applies to that block only. Bits are set in this STAT flag initially by the PMU that generates the data and can be altered by other processors in the data chain, such as by a DC. The STAT word gives a complete status for the data in its data block within the bounds of this standard.

Bits 15 and 12 are normally only used by the DC and should be set to 0 by a PMU except when Bit 15 is used to indicate the PMU is in test mode and outputting test data. Bits 14, 13, and 11 will normally be set by the PMU making the measurement, but may be altered as required

Bit 15—Data Valid: Set to 1 when PMU data block contains invalid data. It will normally be 0 (when the block contains valid data). In order to retransmit a consistent data frame, a DC shall continue to forward data in the same format even when the input from a single PMU fails. The data block for the failed input will be present, but contain either filled-in data or invalid data indications; in this case the bit will be set to 1.

Bit 14—PMU Error: A catchall that the PMU will set to indicate an internal error such as analog-to-digital (A/D) out of calibration, memory error, processor error, etc. Since the PMU will normally only send data frames, this bit shall indicate an error that may invalidate all or part of the data; the exact conditions shall be defined by the manufacturer. Bit 14 will normally be 0.

Bit 13—PMU Sync Error: Set to 1 to indicate the PMU has detected a loss of external time synchronization such as a loss of satellite tracking or an IRIG-B input connection failure. It shall be used both when the time synchronization input fails and when the source of time synchronization loses time lock. The measuring PMU shall set this bit to 1 when any bit in the 4-bit time quality field in the FRACSEC field becomes nonzero. A DC may also set Bit 13 to 1 if it detects a synchronization error in the data stream from a particular PMU. The length of time between detecting a sync error and setting Bit 13 to 1 shall not exceed the time estimated for the time error to exceed the TVE limit or 1 min, whichever is less.

Bit 12—Data Sorting Type: Set to 1 when the data for the particular PMU is not integrated into the data frame by using its timetag. A concentrator will normally integrate data from a number of PMUs into a single frame by the timetags provided by the PMUs. If a PMU in the group loses external time sync for an extended period of time, timetag provided by the PMU may prevent this integration or make time alignment worse than using another integration method. As an alternative to simply discarding all the data, the concentrator can include the data in the frame using a “best guess” as to which frame it goes in, and warn of lack of precise time correlation by setting Bit 12. The simplest approach for the concentrator in a real-time system is to include the unsynchronized data with the most current synchronized data, using the assumption that data communication delays are equal. This “sort-by-arrival” method is a simple best-guess data alignment. Other methods can be used. In all cases, Bit 12 will be set to 1 when data is not correlated into its frame by timetag and cleared to 0 when data is correlated by timetag.

Bit 11—PMU Trigger pick-up: Set to indicate a trigger condition has been detected for PMUs that have trigger capability. The bit shall be set for at least one data frame or 1 s, whichever is longer, and shall remain set as long as the trigger condition is detected.

Bit 10—Configuration changed bit shall be set to a 1 to indicate that the PMU configuration has been changed. This bit is to be reset to 0 after 1 min. This serves as an indication that the receiving device should request the configuration file to be sure configuration data is up-to-date. To be certain of having a valid configuration file, the receiving device should request a configuration file whenever it has been off-line for more than a minute.

Bits 4–5—Unlocked time: Indicates a range of seconds since loss of synch was detected.

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Bits 0–3—Trigger reason: A 4-bit code indicating the initial cause of a trigger. See Table 8 for encoding.

6.4 Configuration frame

A configuration frame is a machine-readable BINARY data set containing information and processing parameters for the PMU and the current real-time data set. It is identified by Bits 4–6 of the SYNC word as shown in Table 4. Two configuration types are identified, CFG-1 with SYNC bit 4 set to 0 and CFG-2 with Bit 4 set to 1. CFG-1 denotes the PMU capability indicating measurements that the PMU is capable of making. CFG-2 indicates measurements currently being made and transmitted in the data frame. This may be only a subset of available data. Both frames have all 19 fields, with 7–16 repeated as necessary. All fields shall be fixed length as described, and no delimiters shall be used. The frame contents are shown in Table 9 and described in Table 10.

Table 9—Configuration frame organization

No.	Field	Size (bytes)	Short Description
1	SYNC	2	Sync byte followed by frame type and version number.
2	FRAMESIZE	2	Number of bytes in frame, defined in 6.2.
3	IDCODE	2	PMU/DC ID number, 16-bit integer, defined in 6.2.
4	SOC	4	SOC time stamp, defined in 6.2.
5	FRACSEC	4	Fraction of Second and Time Quality, defined in 6.2.
6	TIME_BASE	4	Resolution of fraction-of-second time stamp.
7	NUM_PMU	2	The number of PMUs included in the data frame.
8	STN	16	Station Name—16 bytes in ASCII format.
9	IDCODE	2	PMU ID number as above, identifies source of each data block.
10	FORMAT	2	Data format within the data frame.
11	PHNMR	2	Number of phasors—2-byte integer (0 to 32 767).
12	ANNMR	2	Number of analog values—2-byte integer.
13	DGNMR	2	Number of digital status words—2-byte integer.
14	CHNAM	16 × (PHNMR + ANNMR + 16 × DGNMR)	Phasor and channel names—16 bytes for each phasor, analog, and each digital channel (16 channels in each digital word) in ASCII format in the same order as they are transmitted. For digital channels, the channel name order will be from the least significant to the most significant. (The first name is for Bit 0 of the first 16-bit status word, the second is for Bit 1, etc., up to Bit 15. If there is more than 1 digital status, the next name will apply to Bit 0 of the 2nd word and so on).
15	PHUNIT	4 × PHNMR	Conversion factor for phasor channels.
16	ANUNIT	4 × ANNMR	Conversion factor for analog channels.
17	DIGUNIT	4 × DGNMR	Mask words for digital status words.
18	FNOM	2	Nominal line frequency code and flags.

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Table 9—Configuration frame organization *(continued)*

No.	Field	Size (bytes)	Short Description
19	CFGCNT	2	Configuration change count.
	Repeat 8–19		Fields 8–18, repeated for as many PMUs as in field 7 (NUM_PMU).
20+	DATA_RATE	2	Rate of data transmissions.
21+	CHK	2	CRC-CCITT

Table 10—Word definitions unique to configuration frame

Field	Size (bytes)	Description
TIME_BASE	4	Resolution of the fractional second time stamp (FRACSEC) in all frames. Bits 31–24: Reserved for flags (high 8 bits). Bits 23–0: 24-bit unsigned integer that is the subdivision of the second that the FRACSEC is based on. The actual "fractional second of the data frame" = FRACSEC / TIME_BASE.
NUM_PMU	2	The number of PMUs included in the data frame. No limit specified. The actual limit will be determined by the limit of 65 535 bytes in one frame ("FRAMESIZE" field).
STN	16	Station Name—16 bytes in ASCII format.
IDCODE	2	PMU/DC ID number, 16-bit integer, defined in 6.2. Here it identifies the source of data in each PMU field. If only 1 PMU is the source of the data, this ID will be the same as the third field in the frame.
FORMAT	2	Data format in data frames, 16-bit flag. Bits 15–4: Unused Bit 3: 0 = FREQ/DFREQ 16-bit integer, 1 = floating point Bit 2: 0 = analogs 16-bit integer, 1= floating point Bit 1: 0 = phasors 16-bit integer, 1 = floating point Bit 0: 0 = phasor real and imaginary (rectangular), 1 = magnitude and angle (polar)
PHNMR	2	Number of phasors—2-byte integer
ANNMR	2	Number of analog values—2-byte integer
DGNMR	2	Number of digital status words—2-byte integer. Digital status words are normally 16-bit Boolean numbers with each bit representing a digital status channel measured by a PMU. A digital status word may be used in other user designated ways.
CHNAM	16	Phasor and channel names—16 bytes for each phasor, analog, and digital status word in ASCII format in the same order as they are transmitted
PHUNIT	4	Conversion factor for phasor channels. Four bytes for each phasor. Most significant byte: 0 = voltage; 1 = current. Least significant bytes: An unsigned 24-bit word in 10^{-5} V or amperes per bit to scale 16-bit integer data. (If transmitted data is in floating-point format, this 24-bit value should be ignored.)

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Table 10—Word definitions unique to configuration frame *(continued)*

Field	Size (bytes)	Description
ANUNIT	4	Conversion factor for analog channels. Four bytes for each analog value. Most significant byte: 0 = single point-on-wave, 1 = rms of analog input, 2 = peak of analog input, 5–64 = reserved for future definition; 65–255 = user definable. Least significant bytes: A signed 24-bit word, user-defined scaling.
DIGUNIT	4	Mask words for digital status words. Two 16-bit words are provided for each digital word. The first will be used to indicate the normal status of the digital inputs by returning a 0 when exclusive ORed (XOR) with the status word. The second will indicate the current valid inputs to the PMU by having a bit set in the binary position corresponding to the digital input and all other bits set to 0.[a]
FNOM	2	Nominal line frequency code (16-bit unsigned integer) Bits 15–1: Reserved Bit 0: 1: Fundamental frequency = 50 Hz 0: Fundamental frequency = 60 Hz
DATA_RATE	2	Rate of phasor data transmissions—2-byte integer word (–32 767 to +32 767) If DATA_RATE > 0, rate is number of frames per second. If DATA_RATE < 0, rate is negative of seconds per frame. For example: DATA_RATE = 15 is 15 frames per second and DATA_RATE = –5 is 1 frame per 5 s.
CFGCNT	2	Configuration change count is incremented each time a change is made in the PMU configuration. 0 is the factory default and the initial value.

[a]If digital status words are used for something other than Boolean status indications, the use of masks is left to the user, such as min/max settings.

6.5 Header frame

This frame shall be human readable information about the PMU, the data sources, scaling, algorithms, filtering, or other related information. The frame has the same SYNC, FRAMESIZE, SOC, and CHK as the other frames, and is identified by Bits 4–6 the SYNC word as shown in Table 4. The data section has no fixed format (see Table 11).

Table 11—Header frame organization

No.	Field	Size	Comment
1	SYNC	2	Sync byte followed by frame type and version number.
2	FRAMESIZE	2	Number of bytes in frame, defined in 6.2.
3	IDCODE	2	PMU/DC ID number, 16-bit integer, defined in 6.2
4	SOC	4	SOC time stamp, defined in 6.2.
5	FRACSEC	4	Fraction of Second and Time Quality, defined in 6.2.
6	DATA 1	1	ASCII character, 1st byte
K+6	DATA k	1	ASCII character, Kth byte, K>0 is an integer.
K+7	CHK	2	CRC-CCITT check

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6.6 Command frame

A PMU shall be able to receive commands from a control system and take appropriate actions. This Command Frame uses the same SYNC, FRAMESIZE, SOC, FRACSEC, and CHK words as all other messages and is identified by Bits 4–6 of the SYNC word as shown in Table 4. The command message frame is shown in Table 12. IDCODE shall be a 2-byte identification code assigned to a PMU/DC and is the same as field 3 in the configuration frame. The CHK is the 16-bit CRC-CCITT described previously. The PMU shall match the IDCODE with one stored internally before accepting and executing the command. The IDCODE shall be user settable. CMD shall be a 2-byte command code as defined in Table 13.

Table 12—Command frame organization

No.	Field	Size	Comment
1	SYNC	2	Sync byte followed by frame type and version number.
2	FRAMESIZE	2	Number of bytes in frame, defined in 6.2.
3	IDCODE	2	PMU/DC ID number, 16-bit integer, defined in 6.2.
4	SOC	4	SOC time stamp, defined in 6.2.
5	FRACSEC	4	Fraction of Second and Time Quality, defined in 6.2.
6	CMD	2	Command being sent to the PMU/DC.
7	EXTFRAME	0–65518	Extended frame data, 16-bit words, 0 to 65 518 bytes as indicated by frame size, data user defined.
8	CHK	2	CRC-CCITT check

Table 13—Commands sent to the PMU

Command word bits	Definition
Bits 15–4	Reserved for future use
Bits 3–2–1–0:	
0001	Turn off transmission of data frames.
0010	Turn on transmission of data frames.
0011	Send HDR file.
0100	Send CFG-1 file.
0101	Send CFG-2 file.
1000	Extended frame.

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Annex A

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[B5] IEEE Std 1012™-2004, IEEE Standard for Software Verification and Validation.

[B6] IEEE Std C37.111™-1999, IEEE Standard for Common Format for Transient Data Exchange (COMTRADE) for Power Systems.

[B7] ITU-T Recommendation V.41-1988, Code-independent Error-Control System.[11]

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[7]NTIS publications are available from the National Technical Information Service, U. S. Dept. of Commerce, 5285 Port Royal Rd., Springfield, VA 22161 (http://www.ntis.org/).

[8]IEC publications are available from the Sales Department of the International Electrotechnical Commission, Case Postale 131, 3, rue de Varembé, CH-1211, Genève 20, Switzerland/Suisse (http://www.iec.ch/). IEC publications are also available in the United States from the Sales Department, American National Standards Institute, 25 West 43rd Street, 4th Floor, New York, NY 10036, USA (http://www.ansi.org/).

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[11]ITU-T publications are available from the International Telecommunications Union, Place des Nations, CH-1211, Geneva 20, Switzerland/Suisse (http://www.itu.int/).

[12]RFC standards are available from Global Engineering Documents, 15 Inverness Way East, Englewood, CO 80112, USA (http://global.ihs.com/).

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Annex B

(informative)

Cyclic redundancy check codes

B.1 General

Cyclic redundancy check (CRC) codes are used to verify (or at least indicate) that a set of data has not been corrupted. They are specified by a polynomial, the initial value of the shift registers, the direction the bits are shifted, and optionally a mask to be XORed with the finial register values. The CRC code commonly referred to as CRC-CCITT is illustrated in Figure B.1.

B.2 CRC-CCITT

This annex describes the CRC calculation used in this standard and commonly referred to as CRC-CCITT. It should be noted, however, that the CRC-CCITT described here, and which is in common usage, does not seem to be specified in any CCITT/ITU standard. ITU-T Recommendation V.41-1988 [B7] describes a very similar CRC calculation; however that document proscribes a different initial value than is used in the common implementation of CRC-CCITT. Other ITU documents describe CRC calculations using the same polynomial and initial conditions, but require a final XOR mask not used in CRC-CCITT.

B.3 B.3 CRC-CCITT definition

Since no CCITT/ITU document could be found to describe the CRC calculation commonly referred to as CRC-CCITT, it is defined as follows, in conjunction with Figure B.1.

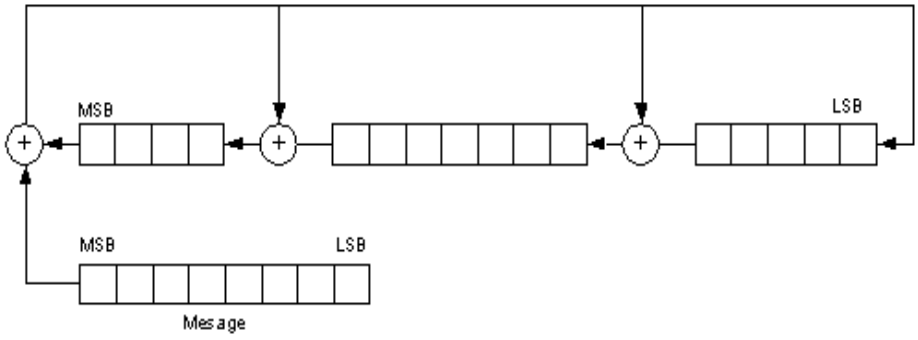

Figure B.1—CRC-CCIT encoder

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B.3.1 Polynomial

See Equation (B.1).

$$g(x) = x^{16} + x^{12} + x^5 + 1 \quad \text{(B.1)}$$

B.3.2 Initial condition

The Shift registers of Figure B.1 are initialized to 1.

B.3.3 Final mask

No final mask is XORed with the final register values.

B.3.4 CRC-CCITT properties

Three important properties of CRC codes are often discussed, their error pattern coverage, their burst error detection capability, and the probability of an undetected error occurring.

B.3.5 Error pattern coverage

Error pattern coverage λ is defined as the ratio of the number of invalid bit patterns over the number of valid bit patterns, as show in Equation (B.2):

$$\lambda = \frac{2^n - 2^k}{2^n} = 1 - 2^{k-n} = 0.999985 \quad \text{(B.2)}$$

where k is the number of bits in the message excluding the CRC value, and n is the number of bits including the CRC value. Therefore, the error pattern coverage is solely a function of the size of the CRC value.

B.4 Burst error detection

Another important property of CRC codes is their ability to detect burst errors. Burst errors are transient or intermittent corruptions of several symbols in a transmitted data stream. By definition, there can be no more than one burst error per message. For binary data, the burst spans all corrupted bits and is bounded by ones. In the following example, let V be an uncorrupted bit, 1 be a nonzero bit and X be a corrupted bit, a zero, or a one with corrupted bits to both its left and right.

…VVV1XXXX1VVV…

Therefore, the burst error length of the above message is 6.

B.4.1 Burst error detection probability of CRC-CCITT

Both Wells [B11] and Wicker [B12] show that the burst error detection probability of a 16-bit binary CRC code is as follows:[13]

[13]These burst error detection probabilities are valid when the order of transmitted data machines matches the order of the data during CRC calculation.

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a) 100% of all bursts less <17 bits long

b) 99.997% of all bursts which are 17 bits long

c) 99.9985% of all bursts that are greater than 17 bits long

B.4.2 Probability of an undetected error

The lower bound for the probability of an undetected error, over a noisy binary symmetric channel is given in Wicker [B12] as follows:

> "For any CRC code of length p used for error detection on the binary symmetric channel, the undetected error probability approaches 2^{-p} as the crossover probability and the dimension k of the code increases."

B.4.3 Sample "C" code calculation example

A number of algorithms are available for calculating the CRC-CCITT. Common and probably the fastest are look-up table routines. The following example is very compact, simple, and does not need a look-up table.

```
/* Compute CRC-CCITT. *Message is a pointer to the first character in the
message; MessLen is the number of characters in the message (not counting
the CRC on the end) */

uint16_t ComputeCRC(unsigned char *Message, unsigned char MessLen)
{
      uint16_t crc=0xFFFF;
      uint16_t temp;
      uint16_t quick;
      int     i;

      for(i=0;i<MessLen;i++)
      {
            temp = (crc>>8) ^ Message[i];
            crc <<= 8;
            quick = temp ^ (temp >> 4);
            crc ^= quick;
            quick <<=5;
            crc ^= quick;
            quick <<= 7;
            crc ^= quick;
      }
   return crc;
}
```

B.4.4 Examples

Table B.1 contains example data, shown both as ASCII characters and as hexadecimal values, and the resulting CRC value.

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Table B.1—Example data

ASCII data	Equivalent hexadecimal data	Resultant CRC value
ABCD	0x41 0x42 0x43 0x44	0xBFFA
123456	0x31 0x32 0x33 0x34 0x35 0x36	0x2EF4
abc	0x61 0x62 0x63	0x514A

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Annex C

(informative)

Timetagging and transient response

C.1 Transient response

As defined in 1.2, the primary purpose of this standard is to ensure PMU interoperability under steady-state conditions with two PMUs of different brands being expected to yield the same phasor measurements. *Steady state* is a condition defined here as one where the frequency, magnitude, and phase angle of the observed signal are constant. Identical PMUs (defined as having identical hardware and algorithms) should yield the same phasor measurement under all conditions. However, two PMUs with different algorithms and/or different analog circuitry can be expected to yield different results for the same phasor measurement in a transient state (defined here as the time during which a change in magnitude, phase angle, or frequency takes place).

PMU measurement accuracy under steady-state conditions is defined in 5.2, with compliance verification tests defined in 5.3. Behavior under transient conditions is not mandated, but can be measured by using benchmark tests defined in Annex G and reported using the TVE concept defined in 5.2.

C.2 Timetags

Phasor measurements are the estimation of the phasor representation of a sinusoidal signal. The estimation is made for the signal at a particular instant of time, and that time represented by the phasor timetag. The process of making a phasor estimate will require sampling the waveform over some interval of time which can lead to some confusion as to which time within that window is the correct timetag for the phasor. In the previous synchrophasor standard, IEEE Std 1344-1995, this was defined as the last sample in the window. While this yields a measurement that appears causal, it also yields ambiguity in response due to the length of the window. Further investigation also showed that this provides an undesirable phase-angle measurement error with change in frequency. Consequently, in this standard the timetag is defined as the time of the theoretical phasor that the estimated phasor represents. This will normally be a time near the center of the estimation window. It is up to the designer to create a conversion process that assures that the magnitude and phase angle are properly represented according to the TVE and verification tests defined in 5.2 and 5.3.

As long as input signal frequency is exactly equal to the nominal power system frequency, phase angles will be calculated correctly. However, if the power system frequency is different from its nominal value, the phasor will rotate as illustrated in 5.1.3. While this does represent a steady-state condition, it is easy to show that the instantaneous value of the phasor phase angle will be determined by the choice of the timetag and the inherent group delay associated with the actual measurement algorithm. This behavior is illustrated in Figure C.1 (frequency step test performed in accordance with G.3, with three different algorithms without group delay compensation).

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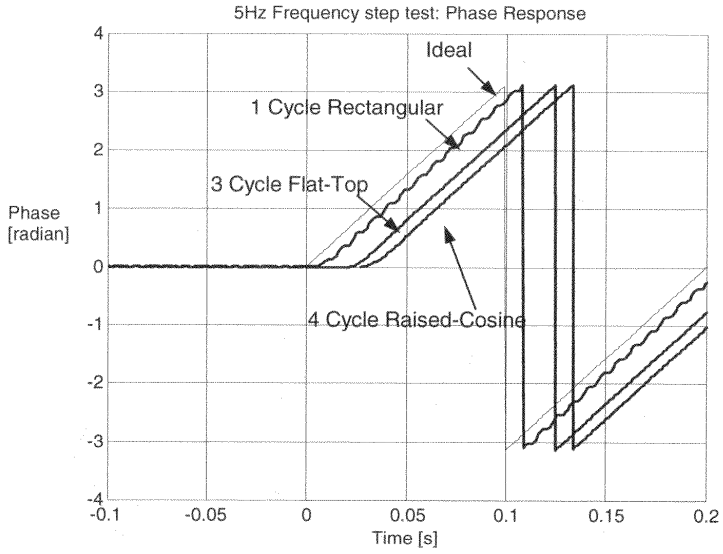

Figure C.1—Frequency step test phase response without group delay compensation

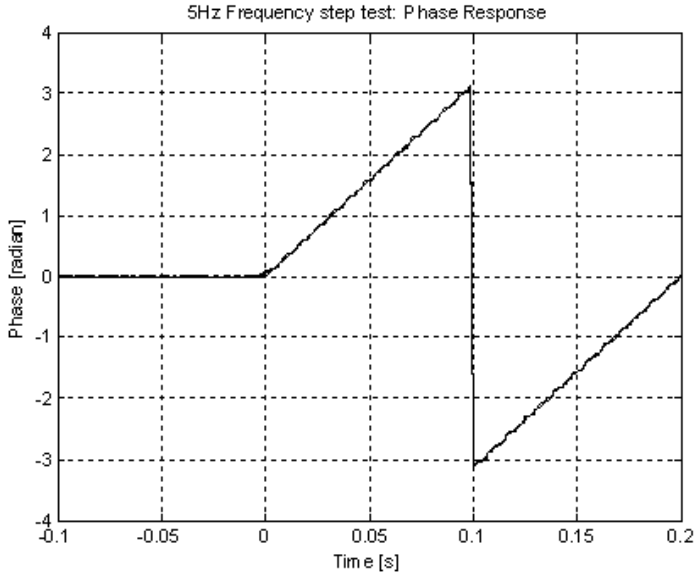

Figure C.2—Frequency step test phase response after group delay compensation (Ideal+3 algorithms, corresponding to Figure C.1)

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By relying on the TVE concept defined in 5.2, this standard eliminates the off-nominal frequency phase-angle ambiguity and ensures the compatibility between different PMUs. All compensation for group delay or other deficiencies of the estimation shall be compensated by the manufacturer. Figure C.2 shows multiple device output (from Figure C.1) after group delay compensation. It is easy to see that devices closely track each other, with four traces virtually indistinguishable from each other.

Figure C.3 shows the results of the magnitude step test (see G.1) for the three different algorithms from Figure C.2 (compensated group delay). This shows there will be differences in responses even though the steady-state response is compensated.

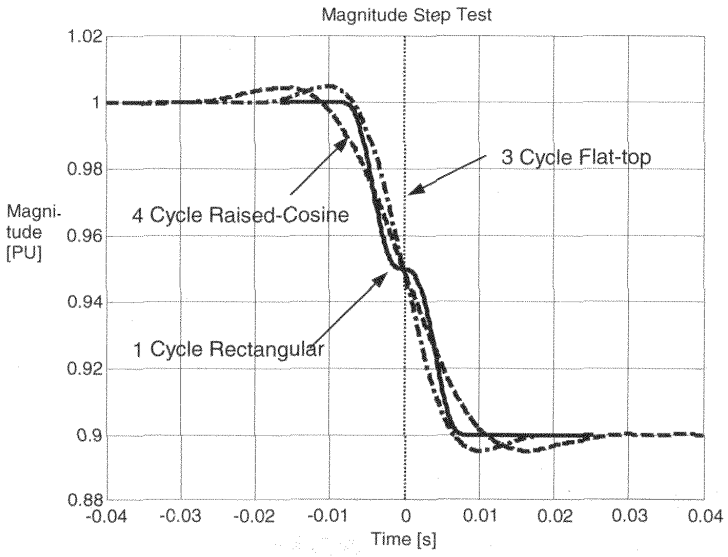

Figure C.3—Magnitude step test results for three different algorithms (group delay compensated, corresponding to Figure C.2). Per unit (PU) voltage or current is normalized to the reference (V/V_{ref} or I/I_{ref}).

Group delay of a finite impulse response (FIR) filter-based algorithm with symmetric coefficients is equal to one-half of the window length (timetag in the center of the window). Infinite impulse response (IIR) filters, asymmetric FIR filters, and optimization-based algorithms may stretch the trailing edge, making the time response asymmetrical. Furthermore, as indicated in Figure C.3, the "transient" behavior will vary depending on the type of algorithm used for phasor estimation. Transient behavior differences are therefore permitted under the current standard. Instead of mandating a single measurement algorithm, this standard defines *total vector error* as a primary tool for device performance comparison and describes applicable benchmark tests (see Annex G).

C.3 Phase-angle measurement errors caused by rapid frequency changes

PMUs that conform to this IEEE standard are expected to produce a stream of accurate, synchronized phasor measurements. The question arises as to how PMUs can be expected to respond during major power system frequency disturbances. The concern is that rapid changes in frequency could lead to errors in the measured phase angle. The following analysis shows that within reasonable disturbances, the effect is negligible.

Consider a PMU that computes phasors centered on a one-cycle window, based on the frequency at the center of the window. (There may be some error in the estimate of the frequency that can cause some error in

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the computation of phasors, but that is not considered here.) We will assume that the PMU has an accurate estimate of the frequency at the center of the window, and that the rate of change of frequency is constant over the window. In that case, the frequency relative to the center of window is given by Equation (C.1):

$$f(t) = f_0 + \frac{df}{dt} \cdot (t - t_0) \tag{C.1}$$

where

$f(t)$ = power system frequency, in cycles per second

t = time, in seconds

$\frac{df}{dt}$ = rate of change of frequency, in cycles per second per second

f_0 = power system frequency at the center of the window

t_0 = time, in seconds, at the center of the window = phasor timetag

The phase angle relative to phase angle and frequency at the center of the window is the integral of the frequency deviation, as shown in Equation (C.2):

$$\theta(t) - \theta_0 = \frac{1}{2} \cdot \frac{df}{dt} \cdot (t - t_0)^2 \tag{C.2}$$

where

$\theta(t) - \theta_0$ = phase-angle deviation, in cycles

The phase-angle deviation relative to the center value is quadratic. The largest value is at the beginning and the end of the time window, given by Equation (C.3):

$$\Delta\theta = \frac{1}{8} \cdot \frac{df}{dt} \cdot T^2 \tag{C.3}$$

where

$\Delta\theta$ = accumulated phase-angle shift, in cycles

$\frac{df}{dt}$ = rate of change of frequency, in Hz per second

T = width of the sampling window, in seconds

The phase-angle deviation is not much, even under extreme conditions. For example, during a very extreme disturbance of 0.36 Hz per second, the phase-angle shift from the center of a one-cycle window to the edge due to *df/dt* is equal to 1.25E-5 cycles, or 0.0045°, which can be ignored for all practical purposes.

The conclusion is that a properly designed PMU conforming to this standard will not incur phasor measurement errors during major power system disturbances due to power system frequency changing over the computation window.

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Annex D

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Message examples

D.1 General

This standard, IEEE Std C37.118-2005, describes four message types: data, configuration, header, and command. The configuration, data and command messages are binary message; the header message is in a human-readable format. This annex provides examples of the three binary message types. Command messages control the operation of the synchrophasor measurement device. Data messages contain the actual measurements and configuration messages that contain information required to decode the data messages.

In general, the data communication structure is designed to support the following requirements:

a) Only measured and computed data should be transmitted in real time. Informational data should be transmitted only on request.

b) All real-time data must be traceable to an absolute time reference. This data should be in the most compact form possible to fit the available channel bandwidth. However, consideration shall be given to optimization of host computer hardware and software.

c) A wide range of data transmission rates shall be supported.

d) The format should support bi-directional real-time control functions in a full-duplex communication mode.

e) A mechanism to transmit bi-directional status information should be provided.

f) Data integrity checks should be provided.

g) The amount and type of data transmitted shall be user definable to adjust to the wide range of data requirements.

D.2 Data message

Table D.1 contains an example data frame. Each row of the table contains a field of the message described in 6.2 and 6.3. The first column contains the field name and the second a brief description of the data contained in the field (see Clause 6 for details). Column three contains specific example data. Column four contains the number of 8-bit bytes of data in the field, and column five contains the hexadecimal equivalent of the example data.

The time of this example is 9:00.016667 a.m. (UTC) on June 6, 2006. The data frame indicates a balanced 3-phase phase-to-neutral voltage of 134 000 V and a constant system frequency of 62.5 Hz. There are no triggers and the measurement was made referenced to a high-quality time source.

Use the information contained in the configuration frame, shown in Table D.2, to decode this data frame. For example, the PHUNIT fields of the configuration frame indicate the scaling of the voltage phasors is 9.15527 (0xDF847) V per bit. The real part of the A phase voltage has a magnitude of 14 635 (0x392B) counts. Multiply 9.15527 V per count by 14 635 counts to get 13 3987 V.

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Table D.1—Data message example

Field	Short description	Example entry	Size (bytes)	Hexadecimal value
SYNC	Synchronization and Frame Format Field.	Data Frame, Version 1	2	AA 01
FRAMESIZE	Total number of bytes in this frame.	52 bytes in this frame	2	00 34
IDCODE	PMU/DC ID number, 16-bit integer, 1 to 65534	7734	2	1E 36
SOC	Second count (UNIX time, starting midnight 01-Jan-1970 neglecting leap seconds).	9:00 a.m. on 6/6/2006 = 1 149 580 800	4	44 85 36 00
FRACSEC	Time of phasor measurement in microseconds with Time Quality.	Not a leap second, none pending; time locked. 16 817 μs after the second mark	4	00 00 41 B1
STAT	Bitmapped flags: Data valid?, PMU OK?, PMU sync?, Data align by time?, PMU Trigger?, Reserved, Time Error, Trigger Cause.	Data valid, no PMU error, PMU sync, data sorted by time stamp, no PMU trigger, best time quality	2	00 00
PHASORS	Phasor data, 16-bit integer, rectangular format. The first two bytes contain the real part of the phasor and the second two contain the imaginary part.	VA = 14,635 ∠0° (= 134.0 kV ∠0°)	4	39 2B 00 00
		VB = 14,635 ∠–120° (= 134.0 kV ∠–120°)	4	E3 6A CE 7C
		VC = 14,635 ∠120° (= 134.0 kV ∠120°)	4	E3 6A 31 83
		I1 = 1,092 ∠0° (= 500 A ∠0°)	4	04 44 00 00
FREQ	16-bit signed integer. Frequency deviation from nominal in millihertz.	+2500 mHz (Nominal 60 Hz with measured 62.5 Hz)	2	09 C4
DFREQ	Rate of change of frequency		2	00 00
ANALOG	32-bit floating point	ANALOG1 = 100	4	42 C8 00 00
		ANALOG2 = 1000	4	44 7A 00 00
		ANALOG3 = 10000	4	46 1C 40 00
DIGITAL	Digital data, 16-bit fields	0011 1100 0001 0010	2	3C 12
CHK	CRC-CCITT		2	D4 3F

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D.3 Configuration message

Use the configuration frame described in Table D.2 to decode the data frame of Table D.1. Subclauses 6.2 and 6.4 describe the format of the fields listed in each row of Table D.2. As in Table D.1, the first column of Table D.2 contains the field names, the second column contains brief descriptions of the data in the fields, the third column contains example data, the fourth column indicates the number of bytes of data, and the last column shows the hexadecimal values of the example data.

Table D.2—Configuration message example

Field	Short description	Example	Size (bytes)	Hexadecimal value
SYNC	Synchronization byte and version number.	Configuration Frame 2 Version 1	2	AA 31
FRAMESIZE	Number of bytes in frame.	This frame contains 454 bytes	2	01 C6
IDCODE	PMU/DC ID number, 16-bit integer, 1–65534.	7734	2	1E 36
SOC	Second-of-century time stamp (UNIX time, starting midnight 01-Jan-1970).	8:00 a.m. on 6/6/2006 = 1 149 577 200	4	44 85 27 F0
FRACSEC	Fraction of Second with Time Quality.	Leap second pending, to be deleted, clock unlocked but within 100 μs. Fractional time is 0.463 s.	4	56 07 10 98
TIME_BASE	Flag and divisor for time stamping the data.	1 000 000 μs	4	00 0F 42 40
NUM_PMU	The number of PMUs included in the data frame.	Data from 1 PMU	2	00 01
STN	Station Name—16 bytes in ASCII format.	The station name for this example is: “Station A ”	16	53 74 61 74 69 6F 6E 20 41 20 20 20 20 20 20 20
IDCODE	PMU/DC ID number, 16-bit integer, 1–65534.	7734	2	1E 36
FORMAT	Data format within the data frame.	Phasors are represented using rectangular coordinates and 16-bit integers. Analogs are 32-bit floating-point numbers.	2	00 04
PHNMR	Number of phasors—2-byte integer (0 to 32 767).	This example contains four phasors.	2	00 04
ANNMR	Number of analog values—2-byte integer.	This example contains three analog values.	2	00 03
DGNMR	Number of digital status words—2-byte integer.	This example contains one set of binary data.	2	00 01

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Table D.2—Configuration message example *(continued)*

Field	Short description	Example	Size (bytes)	Hexadecimal value
CHNAM	Phasor and channel names—16 bytes for each phasor, analog, and digital channel in ASCII format in the same order as they are transmitted.	The first phasor name is: "VA "	16	56 41 20 20 20 20 20 20 20 20 20 20 20 20 20 20
		The second phasor name is: "VB "	16	56 42 20 20 20 20 20 20 20 20 20 20 20 20 20 20
		The third phasor name is: "VC "	16	56 43 20 20 20 20 20 20 20 20 20 20 20 20 20 20
		The fourth phasor name is: "I1 "	16	49 31 20 20 20 20 20 20 20 20 20 20 20 20 20 20
		The first analog name is: "ANALOG1 "	16	41 4E 41 4C 4F 47 31 20 20 20 20 20 20 20 20 20
		The second analog name is: "ANALOG2 "	16	41 4E 41 4C 4F 47 32 20 20 20 20 20 20 20 20 20
		The third analog name is: "ANALOG3 "	16	41 4E 41 4C 4F 47 33 20 20 20 20 20 20 20 20 20
		Digital channel 1 label is: "BREAKER 1 STATUS "	16	42 52 45 41 4B 45 52 20 31 20 53 54 41 54 55 53
		Digital channel 2 label is: "BREAKER 2 STATUS"	16	42 52 45 41 4B 45 52 20 32 20 53 54 41 54 55 53
		Digital channel 3 label is: "BREAKER 3 STATUS"	16	42 52 45 41 4B 45 52 20 33 20 53 54 41 54 55 53
		Digital channel 4 label is: "BREAKER 4 STATUS"	16	42 52 45 41 4B 45 52 20 34 20 53 54 41 54 55 53
		Digital channel 5 label is: "BREAKER 5 STATUS"	16	42 52 45 41 4B 45 52 20 35 20 53 54 41 54 55 53

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Table D.2—Configuration message example *(continued)*

Field	Short description	Example	Size (bytes)	Hexadecimal value
		Digital channel 6 label is: "BREAKER 6 STATUS"	16	42 52 45 41 4B 45 52 20 36 20 53 54 41 54 55 53
		Digital channel 7 label is: "BREAKER 7 STATUS"	16	42 52 45 41 4B 45 52 20 37 20 53 54 41 54 55 53
		Digital channel 8 label is: "BREAKER 8 STATUS"	16	42 52 45 41 4B 45 52 20 38 20 53 54 41 54 55 53
		Digital channel 9 label is: "BREAKER 9 STATUS"	16	42 52 45 41 4B 45 52 20 39 20 53 54 41 54 55 53
		Digital channel 10 label is: "BREAKER A STATUS"	16	42 52 45 41 4B 45 52 20 41 20 53 54 41 54 55 53
		Digital channel 11 label is: "BREAKER B STATUS"	16	42 52 45 41 4B 45 52 20 42 20 53 54 41 54 55 53
		Digital channel 12 label is: "BREAKER C STATUS"	16	42 52 45 41 4B 45 52 20 43 20 53 54 41 54 55 53
		Digital channel 13 label is: "BREAKER D STATUS"	16	42 52 45 41 4B 45 52 20 44 20 53 54 41 54 55 53
		Digital channel 14 label is: "BREAKER E STATUS"	16	42 52 45 41 4B 45 52 20 45 20 53 54 41 54 55 53
		Digital channel 15 label is: "BREAKER F STATUS"	16	42 52 45 41 4B 45 52 20 46 20 53 54 41 54 55 53
		Digital channel 16 label is: "BREAKER G STATUS"	16	42 52 45 41 4B 45 52 20 47 20 53 54 41 54 55 53

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Table D.2—Configuration message example *(continued)*

Field	Short description	Example	Size (bytes)	Hexadecimal value
PHUNIT	Conversion factor for phasor channels. PhasorMAG = PHUNIT × .00001 Voltage PHUNIT = (300 000/ 32 768) × 10E + 5 Current PHUNIT = (15 000/ 32 768) × 10E + 5	Factor = 915 527	4	00 0D F8 47
		Factor = 915 527	4	00 0D F8 47
		Factor = 915 527	4	00 0D F8 47
		Factor = 45 776	4	01 00 B2 D0
ANUNIT	Conversion factor for analog channels. Because the analogs are represented by floating point, conversion factor is unity (or simply not used).	This analog is an "instantaneous" sample of a point on the input waveform.	4	00 00 00 01
		This analog is an rms calculation.	4	01 00 00 01
		This analog is a peak calculation.	4	02 00 00 01
DIGUNIT	Mask words for digital status words.	First Mask: Normal state is 0 for all bits Second Mask: All 16 bits are valid.	4	00 00 FF FF
FNOM	Nominal line frequency code and flags.	Nominal 60 Hz	2	00 00
CFGCNT	Configuration change count.	22 changes	2	00 16
DATA_RATE	Rate of phasor data transmissions.	30 messages per second	2	00 1E
CHK	CRC-CCITT		2	D5 D1

D.4 Command message

Command messages affect the behavior of the PMU. They control the transmission of data, configuration, and header messages. The example shown in Table D.3 causes a PMU to begin transmission of data messages. The fields shown are described in 6.2 and 6.6.

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Table D.3—Command message example

Field	Short description	Example	Size (bytes)	Hexadecimal value
SYNC	Synchronization byte and version number	Command Message, Version 1	2	AA 41
FRAMESIZE	Number of bytes in frame	18	2	00 12
IDCODE	PMU/DC ID number, 16-bit integer, 1 to 65 534	7734	2	1E 36
SOC	Second-of-century time stamp	12:00 a.m. on 6/6/2006 = 1 149 591 600	4	44 85 60 30
FRACSEC	Fraction of Second with Time Quality	No leap second pending or past, clock never locked, fractional time 0.77 s.	4	0F 0B BF D0
CMD	Defined commands are: data on, data off, send header, send configuration, extended frame.	Turn on the data stream.	2	00 02
CHK	CRC-CCITT		2	CE 00

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Annex E

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Sources of synchronization

E.1 Synchronizing source requirements

A synchronizing source shall have sufficient availability, reliability, and accuracy to meet power system requirements. Power systems operate continuously without interruption. They typically span large geographic areas. A synchronization source should have continuous uninterrupted availability and be accessible to all sites among which the data is to be compared. This could range from two sites at either end of a single power line, to an entire interconnected system area.

The synchronizing signal shall have sufficient accuracy to ensure that the measurement meets TVE accuracy requirements. Its basic accuracy shall be greater than the TVE accuracy requirement detailed in 4.4. If the PMU uses an internal measurement clock, the synchronizing signal shall be have an accuracy and repetition rate sufficient to keep the measurement within the TVE accuracy requirement. The maximum timing error E_t in seconds is shown in Equation (E.1):

$$E_t = E_s + R_i A_c \quad \text{(E.1)}$$

where

E_s is the synchronizing signal maximum error in seconds

R_i is the repetition interval in seconds

A_c is the measurement clock accuracy figure (a ratio of seconds per seconds)

For example, a GPS based 1 PPS synchronizing signal with a maximum error of 1 μs coupled with a 10E-6 measurement clock yields a combined error of 2 μs.

E.2 Broadcasts from satellites

Satellite broadcast timing has significant advantages over other timing systems. Satellites have a wide area of coverage. The signal is little affected by atmospheric conditions or seasonal variations. The time signal is continuously referenced to a national standard. Cost is low because the primary reference and time dissemination system are provided by the satellite system sponsor.

The principal problem with satellite broadcasts has been availability. All satellite broadcast systems have been put up for purposes other than time dissemination. During crises the primary purposes take priority and timing function users have occasionally lost access. Satellite systems are expensive to put up and maintain, so in the longer term the time function user is also at the mercy of funding provided for the primary function.

For most users, the advantages still make satellite systems worth the risk. The main systems being used in 2004 are Geostationary Operational Environmental Satellite (GOES), Global Positioning System (GPS), and the Russian satellite-based radionavigation system, GLONASS. Several other potential sources are being proposed, including a GPS-like overlay on International Maritime Satellite System (INMARSAT) satellites and the proposed European radionavigation system, the GALILEO satellite system.

The GOES system's primary mission is weather monitoring, particularly for hurricane activity in the Western Hemisphere. The system consists of two geostationary satellites situated to provide coverage across

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the entire U.S. Small dish antennas are frequently used and must be readjusted if the satellites are moved. The radio link suffers some interference problems with land-based mobile communications and outages due to solar eclipses in the spring and fall. The system provides time synchronization referenced to UTC with a base accuracy of 25 μs, although a more realistic operating accuracy is 100 μs. Overall it provides a synchronizing signal that is marginally acceptable for phasor measurements.

GPS is a U.S. Department of Defense (DoD) satellite-based radio-navigation system. DoD designed it to provide navigation throughout the world without fail in the worst conceivable scenarios, including all weather, system degradation, and interference conditions. Completed in 1994, it consists of 24 satellites that circle the earth twice a day in six orbital planes. With a minimum of four-satellite coverage at all times, even sites with restricted sky view are unlikely to lose signal reception. Range and time is broadcast on three L-band frequencies. Time can be derived from the coarse acquisition (C/A) code transmitted at 1575 MHz. The signal can be received by a simple omnidirectional antenna. The spread spectrum technique that is used makes the signal resistant to interference.

GPS is steered by a ground-based cesium clock ensemble that itself is referenced to UTC, the world standard. Each satellite provides a correction to UTC time that the receiver automatically applies to the outputs. With this continuous adjustment, timing accuracy is limited only by short-term signal reception whose basic accuracy is 0.2 μs. That baseline accuracy can be improved by advanced decoding and processing techniques. For general applications, a 0.5 μs accuracy is a safer figure to depend on. The short-term frequency accuracy of the received signal is on the order of 10E-11.

Access issues were largely resolved in the 1990s, with agreements to add new civilian frequencies and culminating in termination of the selective availability (SA) signal degradation of the C/A code in 2000. The DoD and U.S. Department of Transportation (DoT) have committed to make GPS available to civilian users at all times except in a national emergency. It limits the inaccuracy introduced by SA so that 92% of the time it will not exceed 0.5 μs and 99.9% of the time it will not exceed 1.1 μs. The Departments also commit the U.S. to provide the signal worldwide without fee for a minimum of 10 years.

INMARSAT is a series of satellites in geostationary orbits put up for maritime communications and navigation. A transponder capable of transmitting a GPS-like signal was designed and planned for inclusion on these satellites, but not actually deployed because of political considerations. The signal is expected to be highly accurate, making a good source for timing. The drawback is it will not be very accessible at high latitudes since geostationary satellites orbit over the equator. Until issues of military control in times of conflict are resolved, these transponders will probably not be deployed.

GLONASS has been in service since the mid-1980s, as has GPS. It is similar to the GPS system but uses a different signal structure and frequency bands. Time synchronization is as good as undegraded GPS. GLONASS timing receivers are available commercially, and for critical applications, could be used as an alternate source for GPS. However, there have been difficulties keeping the system fully operational, and the long-term outlook is uncertain.

GALILEO is under development. It was fully authorized by the European Council (EC) in 2002 and is planned to be operational by 2008. It is planned to offer navigation services both free to the general public and by subscription for higher accuracy users. It will have some level of interoperability with GPS that is yet undefined. The system is still under final definition and development at the time of publication of this standard.

Overall, GPS is the only satellite system with sufficient availability and accuracy for phasor system synchronization. Alternatives will eventually become available, with GALILEO the most promising at this time.

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E.3 Broadcasts from terrestrial locations

Synchronizing signals may also be broadcast from a terrestrial location. This could be a radio broadcast through the atmosphere or a broadcast over a controlled medium such as fiber optics. Radio broadcasts are probably the least expensive, but are the most susceptible to interference and are usually the lowest accuracy. Microwave and fiber optics systems can achieve high accuracy but have high installation costs.

The accuracy of U.S. government provided AM broadcasts, WWV, WWVB, and WWVH, is typically around 1 ms, which is not accurate enough for this application. The LOng RANge navigation system (Loran C) can provide 1 μs accuracy, but requires careful monitoring and external raw time input. It is not available in many continental areas.

Fiber-optic and microwave systems can deliver synchronization reliably at 1 μs and better. This, however, requires a specialized interface that bypasses the usual digital telecommunication interface or a separate communication path. This solution is viable but expensive for implementation and maintenance.

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Annex F

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Time and synchronization communication

F.1 PMU time input

A PMU requires a source of UTC time synchronization. This may be supplied directly from a time broadcast such as GPS or from a local clock using a standard time code. IRIG-B is commonly used for local time dissemination. It may be provided in a level shift, a 1 kHz amplitude modulated signal, or in the bi-phase Manchester modulated format (modulation type 2, B2xx). If the amplitude modulation is used, it may need to be supplemented with a 1 PPS pulse train to achieve the required accuracy. The IRIG-B amplitude modulated format is commonly available and hence is the most readily implemented. The newer Manchester format is more compatible with fiber optic and digital systems and provides complete synchronization without additional signals. Other forms of precise time distribution, such as standard Ethernet using IEEE Std 1588, are emerging and will become increasingly available with new technology developments.

F.1.1 1 Pulse per second

A common feature of timing systems is a pulse train of positive pulses at a rate of 1 PPS. The rising edge of the pulses coincides with the seconds change in the clock and provides a very precise time reference. The pulse widths vary from 5 μs to 0.5 s, and the signal is usually a 5 V amplitude driving a 50 ohm load.

F.1.2 IEEE Std 1588

This is a new standard to allow timing accuracies better than 1 μs for devices connected via a network such as Ethernet. At the time of this writing (2004) several commercially available Ethernet switches have demonstrated this performance.[14]

F.1.3 IRIG-B

IRIG-B is fully described in IRIG Standard 200. Time is provided once per second in seconds through day of year in a binary coded decimal (BCD) format and an optional binary second-of-day count. The format standard allows a number of configurations that are designated as Bxyz, where x indicates the modulation technique, y indicates the counts included in the message, and z indicates the interval. The most commonly used form is B122, which has seconds through day-of-year coded in BCD and is amplitude modulated on a 1 kHz carrier. The amplitude should be a peak-to-peak amplitude of 1 V to 6 V for the mark (peak) with a mark-to-space amplitude ratio 10:3 as provided in the standard. A block of 27 control bits are available for user assignment and can be used to supplement the standard code for continuous timekeeping. The time code format is:

<sync> SS:MM:HH:DDD <control> <binary seconds>

[14] For more information, see http://ieee1588.nist.gov/.

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where

<sync> is the on-time sync marker
SS is the second of the minute [00 to 59 (60 during leap seconds)]
MM is the minute of the hour (00 to 59)
HH is the hour of day in 24 h format (00 to 23)
DDD is the day of year (001 to 366)
<control> is a block of 27 binary control characters
<binary seconds> is a 17-bit second of day in binary

F.1.4 Control bit assignment

By using IRIG-B with additional extensions, old and new time sources and time users can be easily integrated. PMUs should be programmed to check the control bit field and use this additional information where it is provided, but rely on user-entered data where it is not. Where possible, these new assignments are made with zero indicating a normal state, since unused control field bits are normally set to zero. This will minimize the possibility of creating a false alarm. For example, if a control field was all zeroes, the time quality code would indicate the clock was locked with full accuracy, which would not accidentally be interpreted as an error condition. See Table F.1.

Table F.1—Control bit assignments

IRIG-B Pos ID	CTRL bit#	Designation	Explanation
P 50	1	Year, BCD 1	Last 2 digits of year in BCD
P 51	2	Year, BCD 2	IBID
P 52	3	Year, BCD 4	IBID
P 53	4	Year, BCD 8	IBID
P 54	5	Not used	Unassigned
P 55	6	Year, BCD 10	Last 2 digits of year in BCD
P 56	7	Year, BCD 20	IBID
P 57	8	Year, BCD 40	IBID
P 58	9	Year, BCD 80	IBID
P 59	—	P6	Position identifier # 6
P 60	10	Leap Second Pending (LSP)	Becomes 1 s up to 59 s BEFORE leap second insert
P 61	11	Leap Second (LS)	0 = Add LS, 1 = Delete LS
P 62	12	Daylight Saving Pending (DSP)	Becomes 1 s up to 59 s before DST change
P 63	13	Daylight Savings Time (DST)	Becomes 1 during DST
P 64	14	Time Offset sign	Time offset sign—0 = +, 1 = –

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Table F.1—Control bit assignments *(continued)*

IRIG-B Pos ID	CTRL bit#	Designation	Explanation
P 65	15	Time Offset—binary 1	Offset from coded IRIG-B time to UTC time. IRIG coded time plus time offset (including sign) equals UTC time at all times (offset will change during DST).
P 66	16	Time Offset—binary 2	
P 67	17	Time Offset—binary 4	
P 68	18	Time Offset—binary 8	
P 69	—	P7	Position identifier # 7
P 70	19	Time Offset—0.5 h	0 = none, 1 = additional 0.5 h time offset
P 71	20	Time Quality	4-bit code representing approx. clock time error. 0000 = clock locked, maximum accuracy 1111 = clock failed, data unreliable
P 72	21	Time Quality	
P 73	22	Time Quality	
P 74	23	Time Quality	
P 75	24	PARITY	Parity on all preceding data bits
P 76	25	Not Used	Unassigned
P 77	26	Not Used	Unassigned
P 78	27	Not Used	Unassigned
P79	—	P8	Position identifier # 8

Virtually every timekeeping system is run by some kind of processor. Since IRIG time code numbers arrive *after* the on-time mark, the timekeeping system must generate the timetag based on the anticipated number rather than on what it just received. Consequently, time counts that are not in exact sequence require advance notice. Non-sequence clock counts include leap year, leap second, and DST changes. The LS and DST bits warn of impending special clock counts, and the last two digits of the year alert the timing system of leap year changes.

As an interpretation of IRIG Standard 200, BCD time and straight binary seconds (SBS) should be consistent. If BCD time changes by an hour for a daylight time change, SBS should change at the same time to reflect a consistent count. The year will roll over with BCD time regardless of whether it corresponds with UTC time.

F.1.4.1 Year

The last two digits of the year are in straight BCD in the same format as the rest of the IRIG-B code and follows first after day of year. It will roll over with the day-of-year in the BCD time count.

F.1.4.2 Leap second

The leap second pending (LSP) and polarity (LS) bits show that one is about to happen and whether it will be inserted or deleted. Leap seconds have only been positive for the last 20 years, so LS = 0 is almost certain. The LSP bit should be asserted between 1 s and 60 s before the hour it is to be inserted. The bit should go to 0 when the second count goes to 00. Leap seconds are always inserted at UTC midnight by altering the second time count only. Thus in UTC time, the time count goes from 23:59:59 to 23:59:60 to 00:00:00 to add the extra second. In another time zone, say Pacific Standard Time, which is 8 h behind UTC,

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the same count will be 15:59:59 to 15:59:60 to 16:00:00. SBS should give the count 57 600 (= 16:00:00) twice.

F.1.4.3 Daylight savings

The DSP and DST bits indicate that a change is about to happen and whether daylight savings is in effect. If DST = 0, then the impending change will be to ON, which will delete 1 h from the time scale (leap forward 1 h in the spring) and the DST bit will go to one. If DST = 1, the opposite will occur. Daylight time changes will be 1 h and are asserted at the minute rollover. The DSP bit should be asserted between 1 s and 60 s before time is to be changed. The DSP and DST bits should change at the same time between the 59 s and 00 s counts. In the U.S. where the time change is put into effect at 2 a.m., the time count in the spring is 01:59:59 to 03:00:00. In the fall, the count is 01:59:59 to 01:00:00.

F.1.4.4 Local time offset

The local time offset is a 4-bit binary count with a sign bit. An extra bit has been included for an additional 0.5 h offset used by a few countries. The offset gives the hours difference (up to ± 16.5 h) between UTC time and the IRIG-B time (both BCD and SBS codes). Subtracting the offset from the IRIG-B time using the included sign gives UTC time. [For example, if the IRIG-B time is 109:14:43:27 and the offset is –06 given by the code 0110 (.0), then UTC time is 109:20:43:27.] The local time offset should always give the true difference between IRIG code and UTC time, so the offset changes whenever a DST change is made. Keeping this offset consistent with UTC simplifies operation of remote equipment that uses UTC time.

F.1.4.5 Time Quality

A 4-bit Time Quality indicator code is used by several manufacturers and is in several existing standards. It is an indicator of time accuracy or synchronization relative to UTC and is based on the clock's internal parameters. The code recommended here is by order of magnitude relative to 1 ns. It is basically the same as used in the HaveQuick and STANAG 4430 (NATO) time codes but with a more practical scale. The 1 ns basic reference is fine enough to accommodate all present industry uses now and into the foreseeable future. With present GPS technology at the 100 ns accuracy level, a 0000 code indicating *locked* will go to a 0011 or a 0100 code at unlock. See Table F.2.

Table F.2—Four-bit Time Quality indicator code

Binary	Hex	Value (worst-case accuracy)
1111	F	Fault—clock failure, time not reliable
1011	B	10 s
1010	A	1 s
1001	9	100 ms (time within 0.1 s)
1000	8	10 ms (time within 0.01 s)
0111	7	1 ms (time within 0.001 s)
0110	6	100 μs (time within 10^{-4} s)
0101	5	10 μs (time within 10^{-5} s)
0100	4	1 μs (time within 10^{-6} s)

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Table F.2—Four-bit Time Quality indicator code *(continued)*

Binary	Hex	Value (worst-case accuracy)
0011	3	100 ns (time within 10^{-7} s)
0010	2	10 ns (time within 10^{-8} s)
0001	1	1 ns (time within 10^{-9} s)
0000	0	Normal operation, clock locked

F.1.4.6 Parity

A parity bit is easy to implement by simply adding modulo-2 to all the bits in the message from BCD seconds through the time quality control bits. This results in odd parity. (SBSs would not be included.) It provides some assurance that the data is correct and a secondary verification that the control bit field has been implemented. An unused bit could not be mistaken for parity since parity will change each second most of the time as the second count increments. The last three unused bits are left after the parity for user specific assignment without affecting this code. They could be used for higher order bits in a 4-bit parity or longitudinal redundancy check (LRC).

F.2 High precision time code format

IRIG-B format transmitted using modified Manchester modulation is recommended as an alternative to the AM modulated IRIG-B with separate 1 PPS sync. This modulation is better adapted for both fiber and metallic digital systems. With the previous control bit assignments, this time code format can serve all power industry requirements now and in the foreseeable future.

Manchester coding provides a zero mean code that is easy to decode, even at low signal levels. The 1 kHz clock provides a precise on-time mark that is always present. The coding method mimics 1 kHz modulated IRIG-B with binary 1's and 0's in place of high and low amplitude cycles. A Manchester binary 1 is equivalent to a high amplitude cycle in the AM modulation, and a binary 0 indicates a low amplitude cycle. Using this modulation, an IRIG-B code 0 will be two ones followed by eight zeroes. An IRIG-B code 1 will be five ones followed by five zeroes (see Figure F.1). This conversion keeps the codes compatible and makes translation or regeneration of the AM IRIG-B very simple.

F.2.1 Modified Manchester coding

Manchester modulation or encoding is a return-to-zero type where the pulse transition indicates binary 0 or 1. In this case, a 1 kHz square wave is the basic clock modulated by the data to produce a rising edge to indicate a binary one (1) and a falling edge to indicate a binary zero (0). The transition at every data bit provides good receiver synchronization. Each bit period is half high and half low, so the mean is always one-half, making it easy to decode, even at low levels. In standard Manchester coding, the data edge occurs in the middle of the clock window to indicate a binary one or zero. The "modification" moves the data window so the data is at the edge of the clock window that is on time with UTC (see Figure F.2). In another view, the modification simply defines the middle of the window as "on time." What is important is that the data edge is the on-time mark in the code. This simplifies the construction of readers and regeneration of the other IRIG code forms. Modified Manchester modulation is designated type 2 in the IRIG standard (B2xx).

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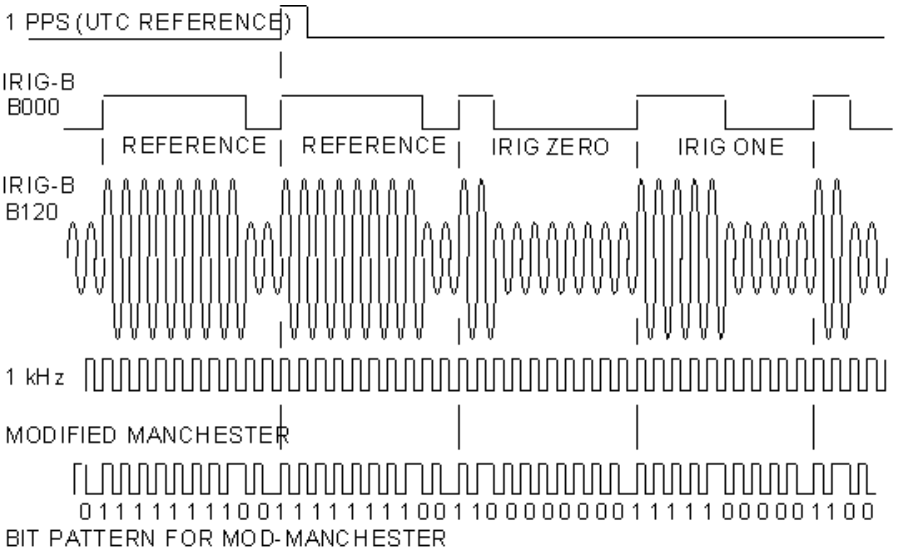

Figure F.1—IRIG-B coding comparisons: level shift, 1 kHz AM, and modified Manchester

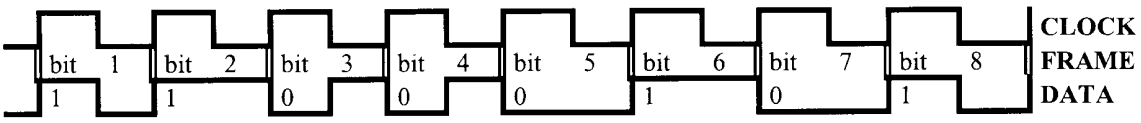

Figure F.2—Modified Manchester coding

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Annex G

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Benchmark tests

G.1 General

As indicated in 1.1, and further explained in Annex C, the exact algorithm used inside the PMU, and measured data behavior in a non steady-state condition, are beyond scope of this standard. A simple set of tests is included and is intended to aid manufacturers in their development process, and may be used to evaluate effects of device inter-operability during the system design and integration phase.

Three benchmark tests are described as follows:

a) 10% magnitude step test

b) 90° phase step test

c) 5 Hz frequency step test

While performing these tests, it is assumed that the sinusoidal test waveform is precisely synchronized (±1 μs) to a precision 1 PPS time source, which is also supplied to the device under test. All waveforms start from a steady-state condition defined at the nominal system frequency, with step change synchronized to a 1 PPS signal transition. A closed form waveform definition used to define the tests makes it possible to easily calculate TVE as described in 5.2.

Accuracy of the waveforms supplied to the PMU under test should be at least four times better that the accuracy of the device under test (i.e., a signal generator with TVE equal to or better than 0.25% will be required to test the 1% PMU requirement defined in 5.2). By using the same device to generate waveforms and the 1 PPS signal, it is possible to conveniently satisfy the 1 μs time synchronization requirement (i.e., arbitrary multi-channel waveform generator). Absolute time synchronization of the test generator to a high-precision UTC reference is not required (all test waveforms are generated with respects to a “local” 1 PPS signal reference).

G.2 Magnitude step test (10%)

The test waveform definition is show in Equation (G.1):

$$x(t<0) = X_{m1}\cos(\omega_0 t) \qquad \text{(G.1)}$$

$$x(0) = \frac{X_{m1}+X_{m2}}{2}\cos(\omega_0 t)$$

$$x(t>0) = X_{m2}\cos(\omega_0 t)$$

Current and voltage magnitude (X_{m1}) can be selected anywhere within the specified PMU input range with $X_{m2} = 0.9 \times X_{m1}$. Basic magnitude step size (10%) can be modified as desired to investigate a full range of operating conditions. See Figure G.1.

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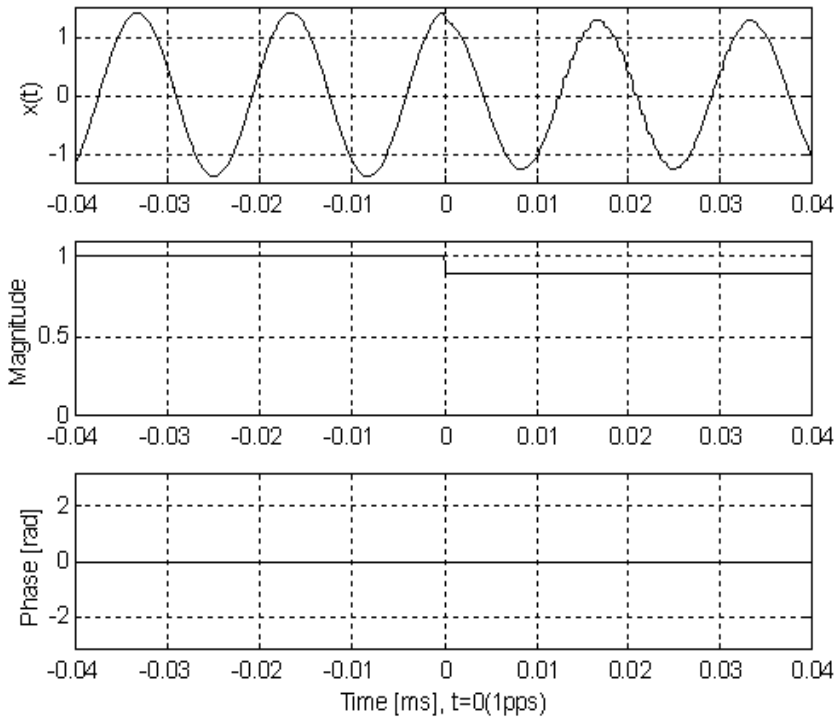

Figure G.1—Magnitude step test with X_{m1} = 1, X_{m2} = 0.9, f_0 = 60 Hz

G.3 Phase step test (90°)

The test waveform definition is shown in Equation (G.2):

$$x(t<0) = X_m \cos(\omega_0 t) \tag{G.2}$$

$$x(0) = X_m \cos\left(\omega_0 t + \frac{\pi}{4}\right)$$

$$x(t>0) = X_m \cos\left(\omega_0 t + \frac{\pi}{2}\right)$$

Current and voltage magnitude (X_m) can be selected anywhere within the specified PMU input range. Basic step size (90°) can be modified as desired to investigate a full range of operating conditions. See Figure G.2.

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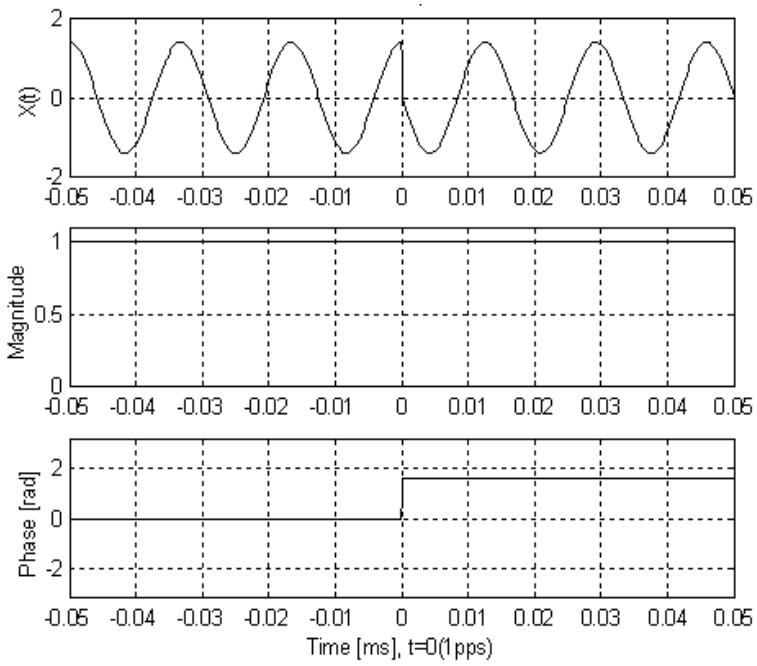

Figure G.2—Phase step test with X_m = 1, f_0 = 60 Hz, phase step = 90°

G.4 Frequency step test (+5 Hz)

The test waveform definition is shown in Equation (G.3):

$$x(t<0) = X_m\cos(\omega_0 t) \qquad \text{(G.3)}$$

$$x(0) = X_m$$

$$x(t>0) = X_m\cos[2\pi(f_0 + 5\ \text{Hz})t]$$

Current and voltage magnitude (X_m) can be selected anywhere within the specified PMU input range. Basic step size (+5 Hz) can be modified as desired to investigate a full range of operating conditions. See Figure G.3.

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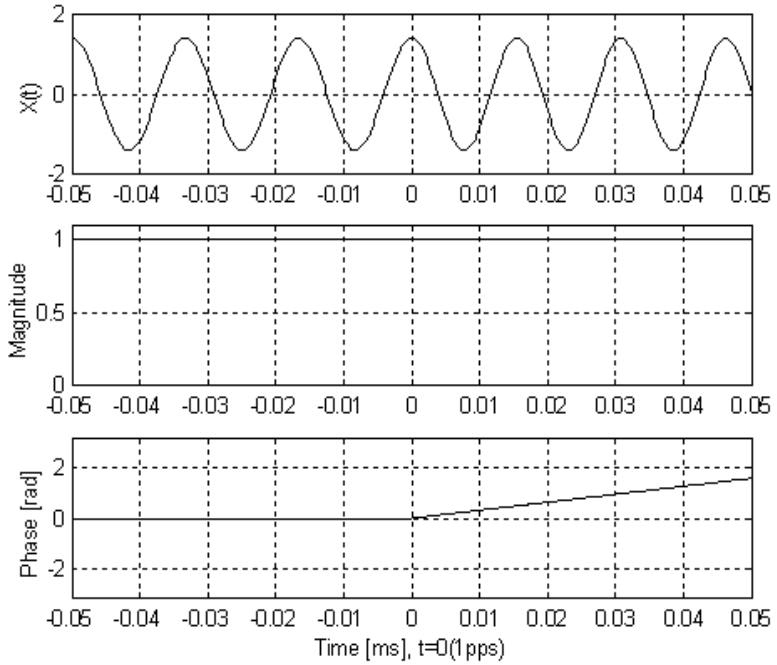

Figure G.3—Frequency step test with X_m = 1, f_0 = 60 Hz, frequency step = +5 Hz

G.5 Magnitude test example

Results of a simulated magnitude step test obtained with a single-cycle, fast Fourier transform (FFT) based algorithm are illustrated in Figure G.4. TVE limits defined in 5.2 are indicated by using dashed lines. It is assumed that the PMU output has been post corrected for PMU unit Group Delay, showing transient response centered within the measurement window. It is easy to see that under steady-state conditions, simulated PMU response stays within the prescribed TVE requirement. However, it is easy to see that a single transient occurring synchronously with a 1 PPS signal transition, gets spread over an entire power system cycle (±8.3 ms, caused by a single-cycle FFT algorithm).

With regard to transient behavior, the PMU manufacturer is encouraged to (at a minimum) specify the type of algorithm used for synchrophasor measurement and the amount of time the device output will stay outside the accuracy limits prescribed in 5.2, for each of the three benchmark tests described.

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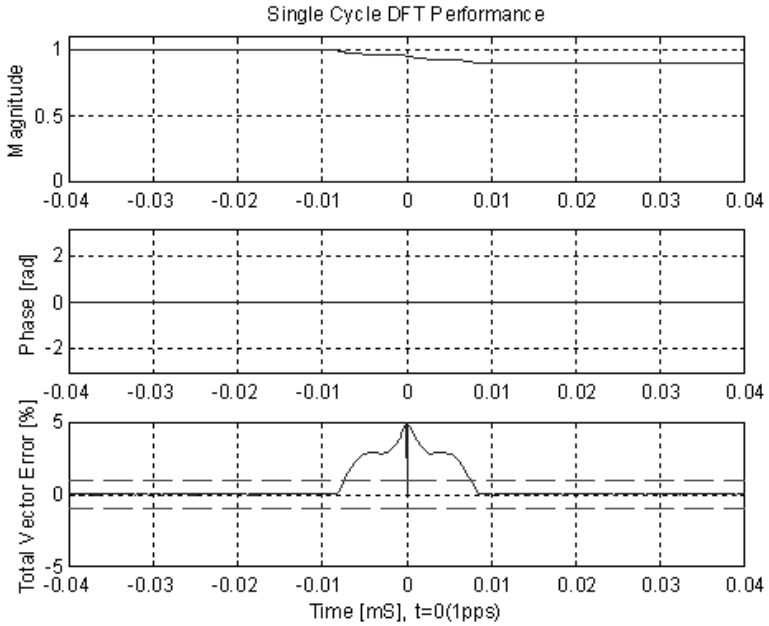

Figure G.4—Magnitude step test example (simulation, 1 cycle FFT based algorithm)

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Annex H

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TVE evaluation and PMU testing

H.1 TVE measurement technique

The TVE accuracy criterion detects errors in time synchronization, and phasor magnitude and angle estimation errors. Figure H.2, Figure H.3, and Figure H.4 are plots of the TVE vs. these three kinds of errors.

Figure H.1 illustrates the relationship between an input signal and PMU output. Here the input signal, $\boldsymbol{X}(t) = X_r(t) + jX_i(t)$, is defined precisely by its phasor representation, $\boldsymbol{X} = X_r + jX_i$, at an instant of time. The ac signal that this phasor model represents is input to the PMU device. The PMU then estimates phasor representation, $\boldsymbol{X}(n) = X_r(n) + jX_i(n)$, from the waveform itself. The TVE is the "vector" difference between the exact applied signal and the estimate.

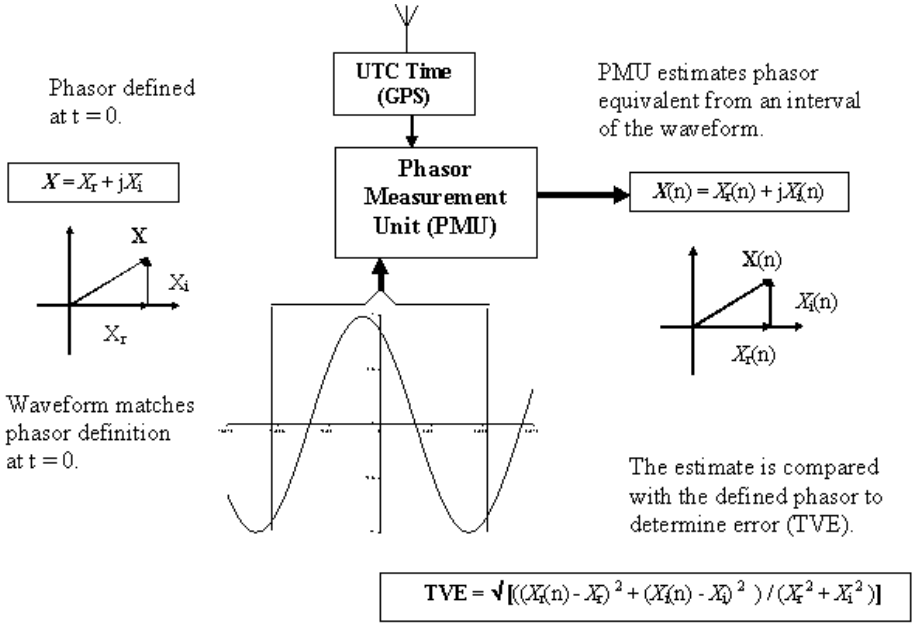

Figure H.1—Phasor measurement process with TVE error detection criteria

A phasor defines an ac signal at an instant of time, and consequently a signal that meets this definition can be generated for an arbitrarily short interval of time. However, measurement of the properties of an ac signal requires an interval of observation. If the signal changes over that interval of observation, the ac properties may be difficult to determine and represent. Phasor estimation is always made over an interval. The standard requires the signal properties to be constant throughout the measurement interval so the estimation can be easily and precisely compared with the input signal. This signal stability can be achieved with laboratory-grade signal generators. In power system operation, signals are not constant, and the measurement represents some kind of an "average" of the input signal over the observation interval. These variations are generally small, and the constant signal test is a good representation. PMU performance under transient conditions can be assessed by observing the transition and settling time after a step change between two

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constant input conditions. A reasonable approximation of transients is a series of steps between constant states, so this can be used to derive a model for measurement of transients.

H.2 TVE example results

Synchrophasor estimation is referenced to UTC as described in Clause 4. If the PMU is not accurately synchronized to UTC, the measured phase will not match the true signal phase. Figure H.2 is a graph of TVE vs. error in time synchronization.

NOTE—A 1% TVE limit is exceeded when the PMU synchronization error reaches ± 26 μs (at 60 Hz).

Errors in phase-angle estimation are similar to timing errors and are shown in Figure H.3. In this case, the error is shown in degrees of phase angle at 60 Hz. Here a 1% TVE is exceeded when phase-angle error reaches ± 0.57°. Errors in magnitude estimation directly correlate to TVE and are shown in Figure H.4. A 1% magnitude error shows up as a 1% TVE error.

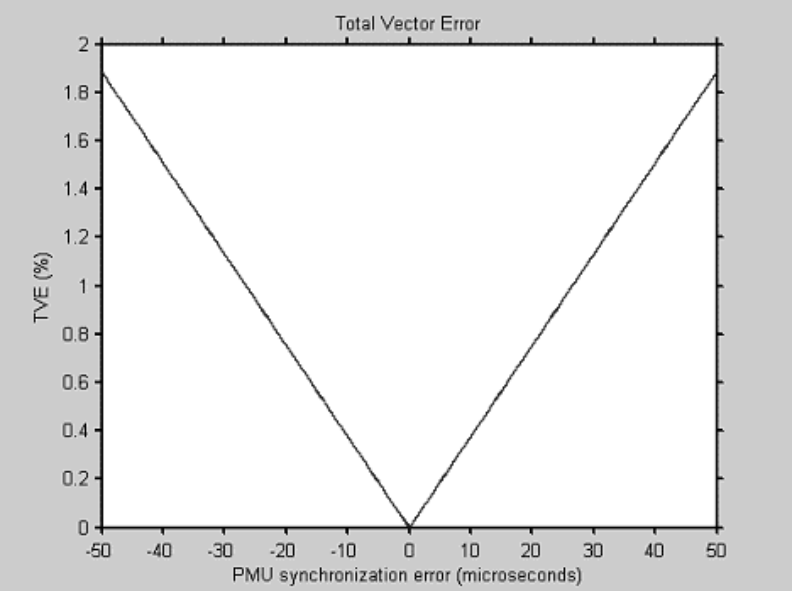

Figure H.2—Error in time synchronization as detected by TVE criteria (60 Hz system)

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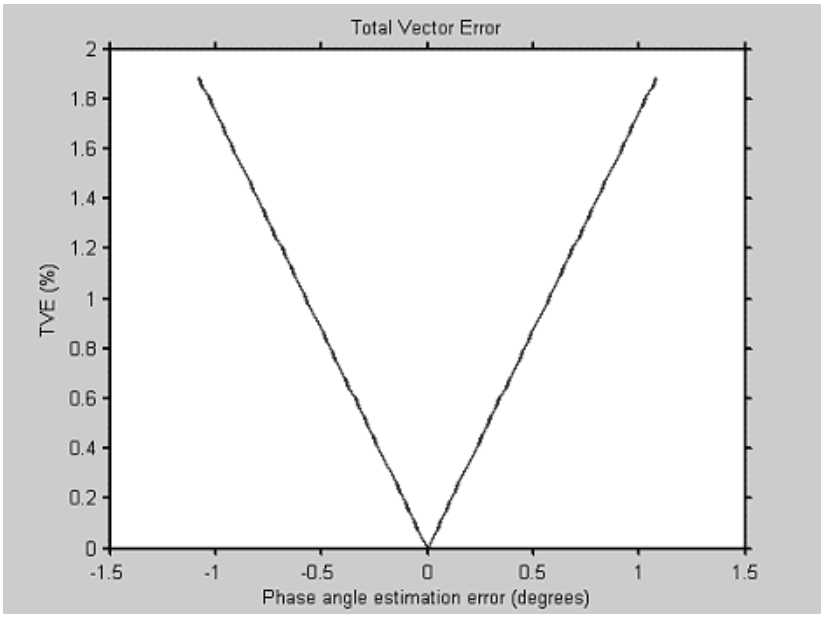

Figure H.3—Phase-angle measurement error as detected by TVE criteria

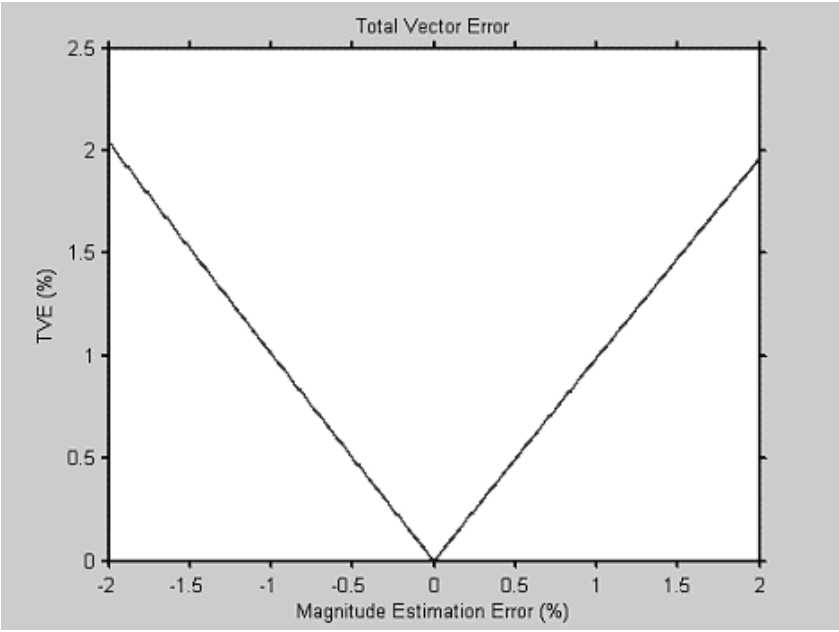

Figure H.4—Magnitude measurement error as detected by TVE criteria

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H.3 Testing

Testing requires providing an input signal synchronized to UTC that is generated with parameters matching a phasor definition. Generally that consists of a certain magnitude, phase angle, and frequency with the signal generator synchronized to a GPS reference. The phasor estimates that are output from the PMU are recorded and compared with the phasor representation of the input signal using the TVE criteria. Signal generators are available that provide precise phase angle, magnitude, and frequency settings that are GPS synchronized.

One of the difficult areas of testing is using a signal that is off the nominal power system frequency. The signal must be in sync with a 1 PPS UTC signal. With off-nominal frequencies, it may be difficult to determine the exact phase at a given instant. Testing can be done at whole or fractional integer frequency offsets to simplify testing. A test frequency of $f_0 + n$ where f_0 is the nominal frequency and n is an integer will be directly synchronizable every second (at 1 PPS). So, for example, frequencies of 61 Hz, 62 Hz, and 63 Hz can be synchronized at every 1 s rollover. Smaller fractional frequencies can be synchronized at longer integer intervals. For example, a test of 60.1 Hz will be synchronizable every 10 s. Testing of these parameters can be tedious, but can be done accurately with carefully planned and executed procedures.

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Annex I

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Synchrophasor message mapping into communications

I.1 Serial communications

The messages specified in Clause 6 shall be mapped in their entirety into the serial communication interface. RS-232 is commonly sent byte by byte with various functions that access the serial interface. The entire message as described in Clause 6 shall be written in the order described to the serial interface. Likewise, when received, it shall be read in its entirety from the serial interface. The serial communication system may apply ordering or encoding within the communication system, but as long as compatible devices are used at both ends, the data written into and read from the serial interface will be the same and in the same order. Figure I.1 illustrates this process.

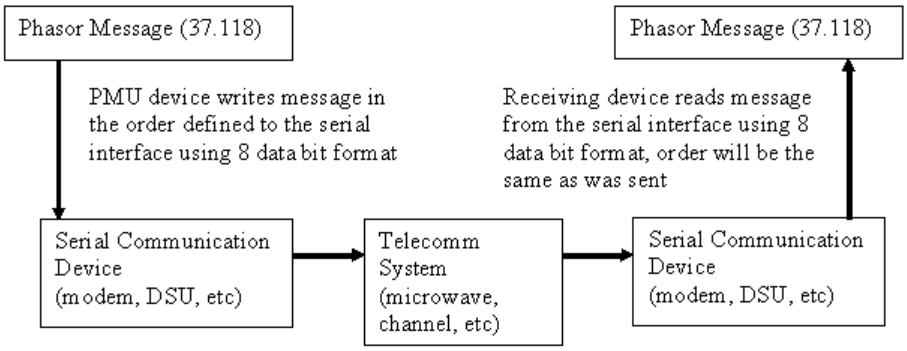

Figure I.1—Phasor message transmission over serial communications

I.2 Network communications using IP protocol

Phasor messages shall also be mapped in their entirety into transmission control protocol (TCP) (as defined in RFC 793-1981 [B8]) or user datagram protocol (UDP) (as defined in RFC 768-1980 [B9]). They shall be written to and read from using standard IP input-output functions. Default port numbers shall be 4712 for TCP and 4713 for UDP, but in all cases, the user shall be provided the means to set port numbers as desired. The IP protocol may be carried over Ethernet or another transport means. With a stacked protocol like IP, each message layer is encapsulated in the next one down to the transport layer where the message is sent. This process is illustrated in Figure I.2.

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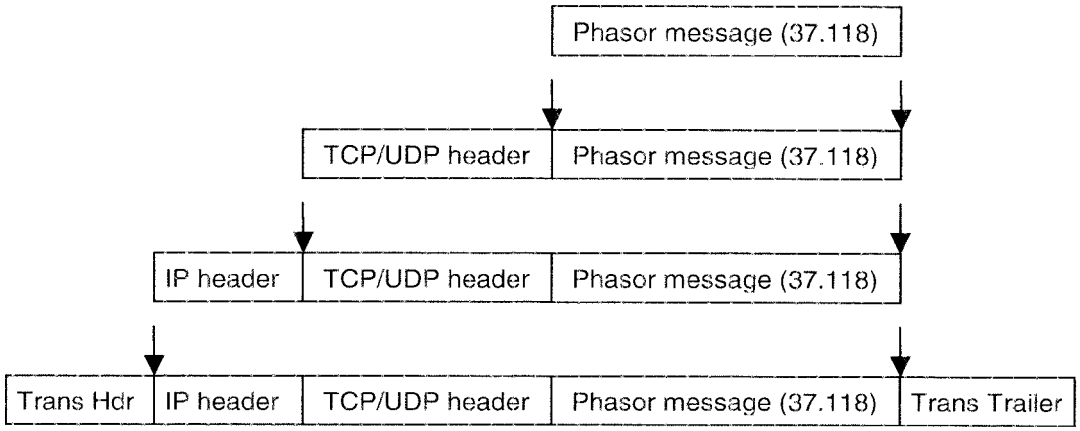

Figure I.2—Mapping of IEEE C37.118 data into a TCP or UDP packet. A transport layer header and trailer are shown, as it would be when using Ethernet.

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