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An American National Standard

IEEE Standard Test Specifications for Varistor Surge-Protective Devices

Sponsor
Surge Protective Devices Committee
of the
IEEE Power Engineering Society

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Foreword

(This Foreword is not a part of IEEE C62.33-1982, IEEE Standard Test Specifications for Varistor Surge-Protective Devices.)

This test specification has been developed for the purpose of testing and comparing varistor type surge protective devices.

The varistor device is a surge diverter used for limiting transient overvoltages in power and communications circuits. Two types of material have been used for many years, silicon carbide, primarily in high voltage arresters, and metal oxide varistors.

The interest in low voltage varistors has grown with the trend to highly sophisticated electrical and electronic devices which are exposed to surges from the environment. Initially, there were no standard terms or tests to define or compare these devices. The IEEE Surge Protection Devices Committee formed its Low Voltage Surge Protection Devices Working Group in 1970 to define these parameters.

Experts were drawn from many fields in communications and power utilities, electronic manufacturers and users, test equipment manufacturers and laboratories, and producers of varistors themselves. The requirements, experiences and vocabularies of these representatives were melded to produce this document as a guide to potential users of varistor surge protective devices.

At the time this standard was published it was under consideration for approval as an American National Standard. The American National Standards Committee C62 Surge Arresters had the following members at the time this document was sent to letter ballot.

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IEEE Standard Test Specifications for Varistor Surge-Protective Devices

1. Scope

1.1

This standard applies to varistors for surge protective applications on systems with dc to 420 Hz frequency and voltages equal to or less than 1000 V rms, or 1200 V dc. This standard contains definitions, service conditions and a series of test criteria for determining the electrical characteristics of these varistors. If the characteristics differ with the direction of conduction, then the tests determine characteristics for both polarities. Arresters covered by ANSI/IEEE C62.1-1984 [1][1] are excluded from this standard.

1.2

The tests in this standard are intended as design tests as defined in ANSI/IEEE Std 100-1984 [3] and provide a means of comparison among various surge-protective devices.

1.3

Varistor surge-protective devices are used to provide transient overvoltage protection in electrical circuits. Varistors, as defined in ANSI/IEEE Std 100-1984 [3], are devices exhibiting a nonlinear volt-ampere characteristic. More specifically, this standard applies to such devices having a monotonic increase in voltage with increasing current flow. Because the impedance of the device decreases with increasing voltage, it provides a relatively low impedance path for surge voltages and a relatively high impedance at normal system voltage, before and after the occurrence of the surge.

Test criteria and definitions in this standard provide a common engineering language beneficial to user and manufacturer of surge-protective varistor devices.

1.4

Due to the voltage and energy levels employed in the majority of tests described herein, all tests should be considered hazardous and appropriate caution should be taken in their performance.

[1]The numbers in brackets correspond to the standards listed in the Bibliography, Section 7. of this standard.

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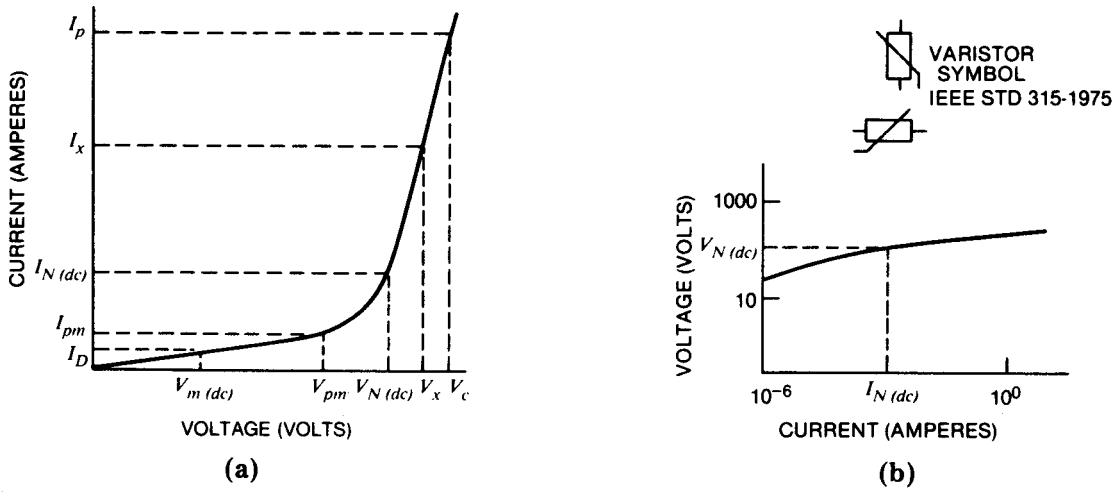
2. A Description of Terms and Letter Symbols Used in Defining Varistors

2.1 Rated Parameter Values

For the purpose of this standard, the values of rated parameters are established by the manufacturer, according to statistical acceptance criteria as indicated in 4.2.

2.2 Descriptions

The descriptions of this section apply to varistors having symmetrical volt-ampere characteristics or asymmetrical volt-ampere characteristics. If the volt-ampere characteristics are different with the direction of conduction they are asymmetrical and the characteristic values shall be specified for each direction. Figure 1 illustrates the relationship between terms on a graph. Some terms are based on impulse response behavior. For the method of defining impulse waveforms see ANSI/IEEE Std 4-1978 [2] and Fig 2 of this standard.



V_x = varistor voltage at current, I_x
$V_{N(dc)}$ = nominal varistor voltage at specified current, $I_{N(dc)}$
V_c = clamping voltage of varistor at peak current, I_p
V_{pm} = maximum rating of peak applied voltage for a specified waveform
$V_{m(dc)}$ = maximum rating of dc applied voltage

Figure 1— Graph Illustrating Symbols and Definitions
(a) Linear Coordinates (not to scale) (b) Logarithmic Coordinates (typical)

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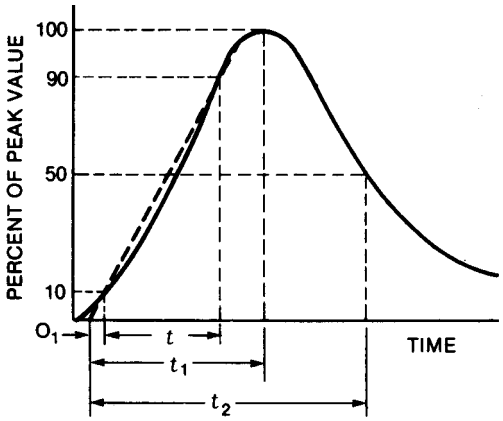

O_1 = virtual origin of wave
t = time from 10% to 90% of peak
t_1 = virtual front time = 1.25 • t
t_2 = virtual time to half value (impulse duration)

Example: For an 8/20 μs current waveform:

8 μs = t_1 = virtual front time
20 μs = t_2 = virtual time to half value

NOTES: (1) This waveform is for a current impulse. Voltage waveforms are defined differently in ANSI/IEEE Std 4-1978 [2].
(2) For details of waveform tolerances and anomalies see ANSI/IEEE Std 4-1978 [2].

Figure 2— Impulse Current Waveform

2.3 Basic Descriptions

Subsections 2.3.1 through 2.3.6 give descriptions of terms and letter symbols used in defining a varistor and are the minimum necessary to characterize the device.

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Term and Description	Symbol	Reference
2.3.1 Clamping Voltage. Peak voltage across the Varistor measured under conditions of a specified peak pulse current and specified waveform. *Note:* Peak voltage and peak current are not necessarily coincidental in time.	V_c	see 4.4 and Fig 3
2.3.2 Rated Peak Single Pulse Transient Current (Varistor). Maximum peak current which may be ap- plied for a single 8/20 μs impulse, with rated line voltage also applied, without causing device failure.	I_{tm}	see 4.5 and Fig 4
2.3.3 Lifetime Rated Pulse Currents (Varistor). Derated values of I_{tm} for impulse durations exceeding that of an 8/20 μs waveshape, and for multiple pulses which**may be applied over device's rated lifetime.**	—	see 4.6 and Fig 3
2.3.4 Rated RMS Voltage (Varistor). Maximum con- tinuous sinusoidal rms voltage which may be applied.	$V_{m(ac)}$	see 4.7 and Fig 5
2.3.5 Rated DC Voltage (Varistor). Maximum continuous dc voltage which may be applied.	$V_{m(dc)}$	see 4.7 and Fig 5
2.3.6 DC Standby Current (Varistor). Varistor current measured at rated voltage, $V_{m(dc)}$.	I_D	see 4.8 and Fig 6
2.4 Additional Descriptions. For certain applications some of the following terms may be useful.		
2.4.1 Nominal Varistor Voltage. Voltage across the varistor measured at a specified pulsed dc current, $I_{N(dc)}$, of specific duration. $I_{N(dc)}$ is specified by the varistor manufacturer.	$V_{N(dc)}$	see 4.9, 5.2 and Fig 6
2.4.2 Peak Nominal Varistor Voltage. Voltage across the varistor measured at a specified peak ac current, $I_{N(ac)}$, of specific duration. $I_{N(ac)}$ is specified by the varistor manufacturer.	$V_{N(ac)}$	see 4.9 and Fig 6
2.4.3 Rated Recurrent Peak Voltage (Varistor). Maximum recurrent peak voltage which may be applied for a specified duty cycle and waveform.	V_{pm}	see 4.10 and Fig 5
2.4.4 Rated Single Pulse Transient Energy (Varistor). Energy which may be dissipated for a single impulse of maximum rated current at a specified waveshape, with rated rms voltage or rated dc voltage also applied, without causing device failure.	W_{tm}	by evaluation, see 6.1
2.4.5 Rated Transient Average Power Dissipation (Varistor). Maximum average power which may be dissipated due to a group of pulses occurring within a specified isolated time period, without causing device failure.	$P_{t(AV)m}$	by evaluation, see 6.2
2.4.6 Varistor Voltage. Voltage across the varistor measured at a given current, I_x.	V_x	definition only, see Fig 1

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Term and Description	Symbol	Reference
2.4.7 Voltage Clamping Ratio (Varistor). A figure of merit measure of the varistor clamping effectiveness as defined by the symbols $V_c/V_{m(ac)}$, $V_c/V_{m\,(dc)}$.	$\frac{V_c}{V_{pm}}$	by computation shown
2.4.8 Nonlinear Exponent. A measure of varistor nonlinearity between two given operating currents, I_1 and I_2, as described by $I = kV^{\alpha}$ where k is a device constant, $I_1 \le I \le I_2$, and $\alpha_{12} = \frac{\log I_2/I_1}{\log V_2/V_1}$	α	by computation shown
2.4.9 Dynamic Impedance (Varistor). A measure of small signal impedance at a given operating point as defined by: $Z_x = \frac{dV_x}{dI_x}$	Z_x	by computation shown
2.4.10 Resistance (Varistor). Static resistance of the varistor at a given operating point as defined by: $R_x = \frac{dV_x}{dI_x}$	R_x	by computation shown
2.4.11 Capacitance (Varistor). Capacitance between the two terminals of the varistor measured at specified frequency and bias.	C	see 4.11
2.4.12 AC Standby Power (Varistor). Varistor ac power dissipation measured at rated rms voltage $V_{m(ac)}$.	P_d	see 4.12 and Fig 7
2.4.13 Voltage Overshoot (Varistor). The excess voltage above the clamping voltage of the device for a given current that occurs when current waves of less than 8 μs virtual front duration are applied. This value may be expressed as a % of the clamping voltage (V_c) for an 8/20 μs current wave.	V_{os}	definition only, see 6.3 and Fig 8
2.4.14 Response Time (Varistor). The time between the point at which the wave exceeds the clamping voltage level (V_c) and the peak of the voltage overshoot. For the purpose of this definition, clamping voltage is defined with a 8/20 μs current waveform of the same peak current amplitude as the waveform used for this response time.	—	definition only, see 6.4 and Fig 8
2.4.15 Overshoot Duration (Varistor). The time between the point at which the wave exceeds the clamping voltage level (V_c) and the point at which the voltage overshoot has decayed to 50% of its peak. For the purpose of this definition, clamping voltage is defined with an 8/20 μs current waveform of the same peak current amplitude as the waveform used for this over-shoot duration.	—	—

3. Service Conditions

3.1 Normal Service Conditions

In the absence of special requirements, the following items should be specified by the manufacturer as appropriate.

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3.1.1 Environmental Conditions

1) Operating and storage temperature ranges
2) Altitude or atmospheric pressure range
3) Humidity
4) Mechanical shock and vibration

3.1.2 Varistor Physical Properties

1) Solvent resistance
2) Solderability
3) Flammability
4) Package rupture during overload

3.1.3 System Conditions

1) Nominal system frequencies
2) Maximum continuous system voltage

3.1.4 Surge Rating of the Varistor under System Conditions

1) Peak single pulse transient current (I_{tm})
2) Lifetime rated pulse currents
3) Rated single pulse transient energy (W_{tm})
4) Rated transient average power dissipation ($P_{t(AV)m}$)

3.2 Unusual Service Conditions

The following service conditions may require special consideration in the design or application of varistors and should be called to the attention of the manufacturer.

3.2.1 Environmental Conditions

1) Ambient temperature exceeding the standard service conditions
2) Altitudes exceeding those specified by the manufacturer
3) Exposure to:
   a) Damaging fumes or vapors
   b) Excessive dirt or current conducting deposits; excessive humidity, moisture, dripping water, steam, or salt spray; explosive atmospheres; abnormal vibrations or shocks
   c) Radiation
4) Unusual transportation or storage conditions
5) Significance of flammability

3.2.2 Physical Conditions

Limitation on weight or space, including clearances to nearby conducting objects; particularly at altitudes exceeding those specified by the manufacturer.

3.2.3 System Conditions

1) System voltages, current or frequency operating conditions exceeding the ratings of the devices (see Section 5., Failure Modes).
2) System surge currents exceeding the rating of the device (see Section 5., Failure Modes).

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3) Any other unusual conditions known to the user

4. Standard Design Test Procedure

4.1 Standard Design Test Criteria

The design tests described in 4.4 through 4.12 provide standardized methods for making single observations of a specified property of a varistor device. These properties may vary from device to device, making it necessary to provide statistical descriptions of the property in order to compare products.

4.2 Statistical Procedures

The following procedure shall be used to describe any property which has been determined to have important statistical aspects. A product sample shall be chosen in a manner consistent with the definition of design tests as provided by ANSI/IEEE Std 100-1977 [3]. A sufficient number of devices shall be tested and the characteristic or rating in question measured as described in the applicable design test until the parameters of the underlying statistical distribution are determined within confidence limits specified by the manufacturer. Values relating to the product sample such as, but not limited to, mean, median, maximum, minimum, and standard deviation may then be stated.

4.3 Test Conditions

The tests of 4.4 through 4.12 should be performed on the device as required by the application. Unless otherwise specified, ambient test conditions should be as follows:

Temperature: 25 ± 5 °C

Relative Humidity: Less than 85%

Altitude: Less than 2000 m (6562 ft)

4.4 Clamping Voltage Test (V_c) (See Fig 3)

4.4.1

The purpose of this test is to determine the voltage protection provided by a varistor when passing a surge current. The clamping voltage shall be measured with a current impulse waveform of 8/20 μs, and specified crest value. A circuit functionally equivalent to Fig 3 shall be employed. The device shall be tested in both polarities unless otherwise specified.

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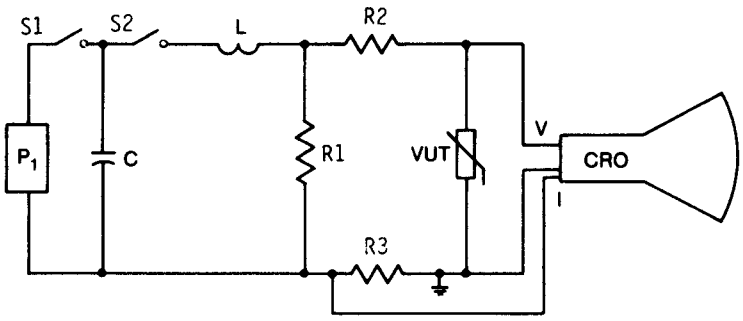

P_1 = charging network or supply
S1 = charging switch
S2 = impulse discharge switch
L = impulse shaping inductor
C = impulse generator capacitor
R1 = impulse shaping resistor
R2 = impulse shaping and current limiting resistor
R3 = current sensing resistor
CRO = oscilloscope for observing current and voltage
VUT = varistor under test

NOTE: Measurement techniques for high current, high frequency testing should be observed, such as a Kelvin contact (four-point probe) and short leads.

Figure 3— Test Circuit for Clamping Voltage Test (V_c)

4.4.2

To establish the shape of the volt-ampere characteristic curve clamping voltage shall be measured at two current levels. These levels shall be of a medium and a high value with respect to rated surge current capability. (The measurement of nominal varistor voltage per paragraph 4.9 provides a low current observation point.) In the absence of specific requirements a peak current test in the range of 5 A to 300 A is suggested for the medium level test. For the high level test a measurement of clamping voltage is suggested during lifetime rated pulse currents test (4.6), using the current from Table 1 corresponding to the two pulse condition, one pulse in both polarities, and an 8/20 μs test waveshape. For special applications, other test waveshapes may be specified.

4.5 Rated Peak Single Pulse Transient Current Test (I_{tm}) (See Fig 4)

4.5.1

The purpose of this test is to verify that a varistor design meets a statistically expressed level of reliability when subjected to a single surge at its rated capability. The failure criteria of Section 5. shall apply.

4.5.2

The varistor shall be subjected to one 8/20 μs current impulse of either polarity at the rated peak amplitude I_{tm}. Rated voltage, $V_{m(ac)}$ or $V_{m(dc)}$ as appropriate, shall be applied continuously for a minimum of 2 s before impulse and a minimum of 30 s after the impulse.

4.6 Lifetime Rated Pulse Currents Tests (See Fig 3)

4.6.1

The purpose of this test is to verify that a varistor design meets a statistically expressed level of reliability when subjected to multiple pulses or different waveshapes, or both, corresponding to any of the lifetime rated pulse currents specified by the manufacturer. In the absence of special requirements tests are recommended at each of the number of pulses and waveshape listed in Table 1. The failure criteria of Section 5. shall apply at the conclusion of each group of multiple impulse tests.

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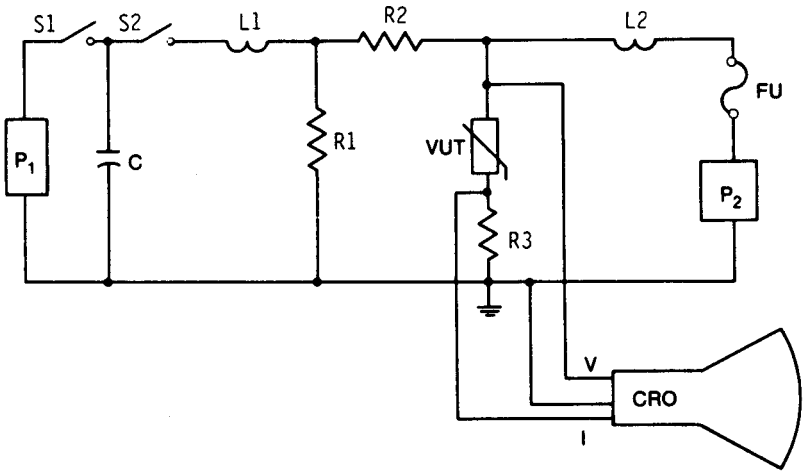
4.6.2

In performing the text matrix of Table 1 new samples shall be used for each current level and waveform tested. In the absence of special requirements surges shall be applied with alternating polarity. The period between pulses shall be selected so as not to exceed device rating of transient average power dissipation as defined under **2.4.5.** These tests except I_{tm} do not require application of line voltage.

Table 1—
Lifetime Rated Pulse Currents*

Number of Pulses	8/20 μs	10/1000 μs
1	I_{tm}	†
2	†	†
10	†	†
100	†	†
10 000	†	†
1 000 000	†	†

*Design Tests are defined in ANSI/IEEE Std 100-1984 [3].
†Value obtained from manufacturers' specifications.



P_1 = charging network or supply
S1 = charging switch
S2 = impulse discharge switch
L1 = impulse shaping inductor
C = impulse generator capacitor
R1 = impulse shaping resistor
R2 = impulse shaping and current limiting resistor
R3 = current sensing shunt
CRO = oscilloscope for observing current and voltage
VUT = varistor under test
P_2 = isolated source of $V_{m(ac)}$ or $V_{m(dc)}$
L2 = low pass filter inductor (see notes 2 and 3)
FU = fuse

NOTES: (1) Measurement techniques for high current, high frequency testing should be observed, such as Kelvin contact (four-point probe) and short leads.

(2) P2 with L2 in series shall be capable of delivering a minimum of 0.5 A to a short-circuit.

(3) Values of L2 are selected so as to present a very high impedance to the surge thereby isolating the power source P_2.

Figure 4— Test Circuit for Verifying Rated Peak Single Pulse Transient Current (I_{tm})

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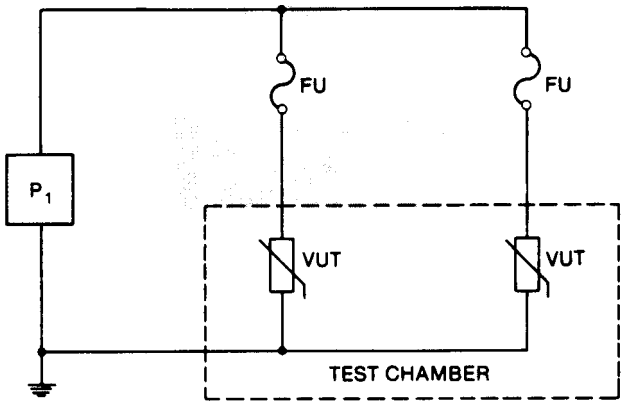

P_1 = regulated ac, dc, V_{pm} power source
FU = fuse
VUT = varistor under test

Figure 5— Test Circuit for Verifying Rated RMS, DC and Peak Voltage ($V_{m(ac)}$, $V_{m(dc)}$, V_{pm})

4.7 Rated RMS Voltage Test ($V_{m(ac)}$) (See Fig 5), Rated DC Voltage Tests ($V_{m(dc)}$) (See Fig 5)

The rated rms voltage or dc voltage of a varistor is based on the limitation of device life, as defined in Section 5., Failure Modes, for the maximum ambient temperature at which the devices are expected to operate. Practical considerations dictate that the test be accelerated by subjecting the device to full rated voltage at higher temperatures. There is no single test that can determine the voltage rating, but rather an evaluation process taking into consideration the desired device life, anticipated ambient temperature, incidence of high energy pulses, and selection of the end-of-life (failure) criteria. These considerations are within the realm of the manufacturer's and user's application engineering functions.

To illustrate this evaluation process, the following procedure is described as typical, with reference to Fig 5. The power supply source (ac or dc depending upon the intended application) must be closely regulated (± 2% maximum), as well as the test chamber temperature (± 3 °C). If the temperature is raised to accelerate the test to the point that catastrophic failures could occur during the test period, individual fusing of the varistors is advisable. Initial readout of the varistor characteristics, especially the varistor nominal voltage, is compared to readouts **at** set intervals, for instance, 168, 500 and 1000 h. Both the initial and intermediate readouts are made with the device at a controlled room temperature (25 ± 5 °C). In the absence of special requirements an ambient temperature of 85 °C and a duration of 1000 h are recommended for these tests.

4.8 DC Standby Current Test (I_D) (See Fig 6)

The varistor shall be tested using a circuit functionally equivalent to Fig 6. A well regulated dc supply is necessary. The current shall be measured after the voltage ($V_{m(dc)}$) has been applied for 10 ms maximum. This time delay allows stabilization of the conduction to approach the long term dc value. The device shall be tested in both polarities unless otherwise specified.

4.9 Nominal Varistor Voltage Test ($V_{N(dc)}$ and $V_{N(ac)}$) (See Fig 6)

4.9.1

The varistor shall be tested using a known or measured source of dc or peak ac current. The time of application shall be between 10 ms and 10 s, or of sufficient duration and with risetime such that the varistor voltage will settle to within

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± 2% of the 10 s value. A circuit functionally equivalent to Fig 6 shall be employed. For dc, the device shall be tested in both polarities unless otherwise specified.

4.9.2

If an ac test is required, peak nominal varistor voltage, $V_{N(ac)}$, shall be measured using a source of 50—60 Hz sinusoidal voltage. A circuit functionally equivalent to Fig 6 shall be employed.

4.10 Rated Recurrent Peak Voltage Test (V_{pm}) (See Fig 5)

The recurrent peak voltage rating of a varistor is related to nonsinusoidal voltage applications. The evaluation process described under **4.7** is applicable, with the exception that the sinusoidal ac power source shall be replaced by one of the specified waveshape.

P_1 = adjustable dc power supply (ac supply if ac test)
R1 = sufficient value to simulate current source (for example, 100 kΩ for $I_{N(dc)}$ = 1.0 mA)
R2 = sufficient value to simulate a voltage source (for example, 10 kΩ for I_D = 10 μA)
DVM = digital voltmeter
VUT = varistor under test

To Measure	Switch Position S1 V	S1 I	S2 V	S2 I_D
I_D		X		X
$V_{N(dc)}$	X		X	
$V_{m(dc)}$	X			X
$I_{N(dc)}$		X	X	

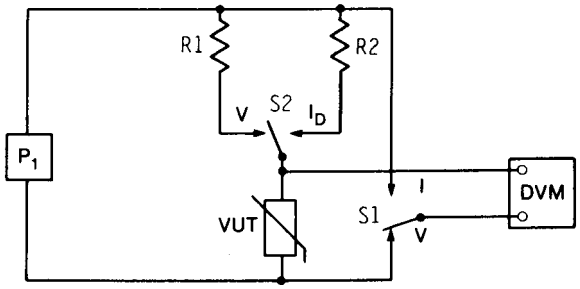

Figure 6— Test Circuit for DC Standby Current and Nominal Varistor Voltage Tests (I_D, $V_{N(dc)}$, $V_{N(ac)}$)

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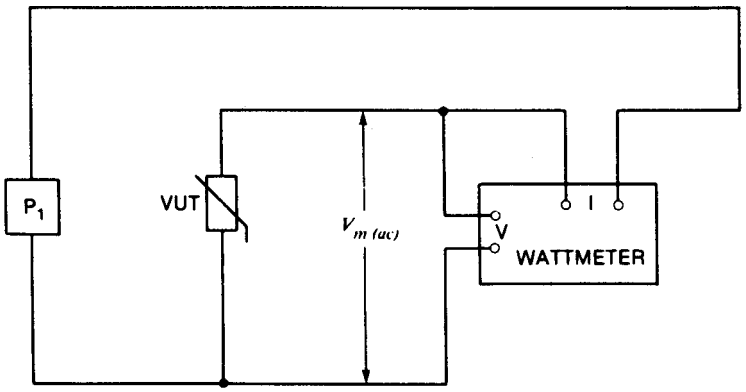

P_1 = 60 Hz power source variable voltage
VUT = varistor under test

NOTE: See 4.12 for information regarding wattmeter characteristics.

Figure 7— Test Circuit for AC Standby Power (P_d)

4.11 Capacitance Test

The capacitance shall be measured at a specified frequency and bias. Note that in the absence of requirements relating to a special application, a frequency of 1.0 MHz and a bias of zero volt dc, is suggested for this test. The signal level shall be such that doubling its amplitude does not change the measured value by more than 5%.

4.12 AC Standby Power (P_d) (See Fig 7)

The varistor shall be tested using a circuit functionally equivalent to Fig 7. The varistor shall be tested at its rated rms voltage $V_{m(ac)}$. The accuracy of $V_{m(ac)}$ shall be 2%. The wattmeter used shall operate accurately with nonsinusoidal current.[2]

The varistor must remain under test until it reaches steady state. The test results are dependent on the ambient temperature and air circulation around the varistor. Care must be taken to duplicate the conditions desired for this test.

5. Failure Modes

In the absence of special requirements, the following criteria are suggested. Tests for determining failure shall be performed after the device temperature has returned to 25 °C ± 5 °C.

5.1 Short-Circuit Failure Mode

In this mode, the device resistance is permanently reduced to less than 100 Ω at 1 V dc.

5.2 Degradation Failure Mode

In this mode, a device has a nominal varistor voltage of less than 90% of the pretest voltage value. Note that since the nominal varistor voltage is used as a basis of failure criteria, the selection of the current density at which the test is conducted can affect the outcome of a failure evaluation. In particular, as the current density selected for the test is

[2]One example of a wattmeter with the required characteristics is the Clarke-Hess Model 255.

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decreased, the sensitivity of the degradation failure mode criterion is increased. Typical values recommended for the current density are in the order of 1 mA/cm^2.

5.3 High Clamping Voltage Failure Mode

In this mode, a device has a clamping voltage of greater than 120% of the pretest clamping voltage measured at the medium current level.

5.4 “Fail-Safe” Operation

The use of “Fail-Safe” to describe a failure mode of a varistor is discouraged for the following reason: failure of a device can occur in any of the modes described above. Some users may consider that the most desirable failure mode for the *device* is to maintain the protective function; for example, fail in the short-circuit failure mode. However, system objectives of other users can require that a particular device should fail in a high clamping failure mode in order to achieve the described performance of the *system*. Thus, failure in the short mode, while considered“fail-safe” by many users, may in fact be opposite the desired (safe) mode of other users.

Therefore, the recommended practice is to describe the failure by one of the failure modes defined in 5.1 through 5.3.

6. Other Parameters

6.1 Rated Transient Energy

Determination of the energy dissipation in a varistor during an impulse requires simultaneous recording of the current and voltage, when real time processing of the product, or subsequent digitizing and multiplying of the waveforms. These operations are time consuming or require special instrumentation which may not be readily available. A very good approximation of the total energy dissipation by a simple waveform can be computed from the peak values. For instance, in the case of current impulse waves with decay times long compared to the front duration, energy is close to 1.4 $V_c I_p t$ where V_c is the clamping voltage, I_p the peak current, t the time to $I_p/2$ of the current wave, those three parameters being readily measured with conventional instrumentation. Furthermore, the data are already available from the results of the lifetime rated pulse current tests (4.6). For an 8/20 μs current wave the energy dissipated by the impulse is equal to 0.9 $V_c I_p t$. For other waveforms, these approximations may be less accurate, and users should revert to peak current evaluation only, unless critical requirements would then dictate a special test program.

Users should be aware that energy rating can be misleading as an indicator of the comparative merit of different varistor designs. The energy deposited in a varistor by a transient current source depends on the varistor clamping voltage. Therefore, a lower energy rating does not necessarily mean a lower capability of survival in the transient environment.

Instead, the single and lifetime pulse current ratings are appropriate tests of varistor surge withstand capability. In the absence of special requirements, energy ratings are recommended for use only as supplements to the predominant current ratings, and for application problems which are more conveniently treated in terms of energy.

A single pulse energy rating can be established, from the data collected in the rated peak current tests, using the same statistical methods for lot acceptance. For multiple pulses, where aging of the varistor is a parameter to be considered, a pulse lifetime factor can be derived. For practical purposes, the same factor used in current ratings, while not theoretically equivalent for the energy, can be applied to the single pulse energy rating for deriving the multiple pulse energy rating.

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6.2 Rated Transient Average Power Dissipation ($P_{t(A\ V)m}$).

The rated transient average power dissipation of a varistor is specified by the manufacturer, in order to limit device temperatures for reliable long life, taking into consideration three parameters:

1) Input average energy deposited in the material by repetitive transients
2) Input power dissipation associated with standby current at the operating temperature (normally a small factor of the total energy input)
3) Output energy transferred to the environment by leads, or heat sink mounting, or both, as recommended by the manufacturer

For stable operation of the varistor, the two inputs, 1 and 2, must be lower than the output capability of 3. The latter is greatly influenced by the specific mounting applied by the user.

6.3 Voltage Overshoot (V_{os}) (See Fig 8).

Under conditions of steep front current impulses at high amplitudes, measurement of the clamping voltage of a lead-mounted varistor indicates values exceeding the levels observed with the standard 8/20 μs waveform. This higher voltage is referred to as *overshoot*. Although some small intrinsic **difference** can be found in the varistor material response to steep current pulses (or ac versus dc), this overshoot is primarily attributable to the magnetic field established around the current-carrying leads of the device, which induces a voltage in the loop formed by the device leads and the protected circuit or the voltage probe used to simulate it.

In typical applications, some lead length is unavoidable, and the associated voltage will also be impressed on the protected circuitry downstream from the varistor. Thus, when measuring clamping voltages at steep fronts and high current it must be recognized that voltage overshoot is dependent on lead length and loop coupling and overshoot should not be treated as an intrinsic device characteristic.

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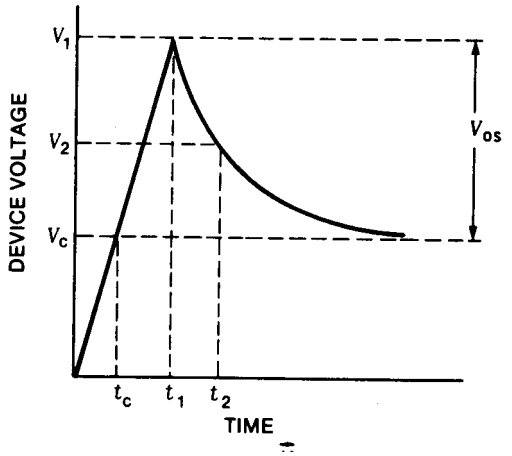

$$V_2 = \frac{V_1 + V_c}{2}$$

V_c = the device clamping voltage for an 8/20 μs current wave form

$V_{os} = V_1 - V_c$ = voltage overshoot

$t_2 - t_c$ = overshoot duration

t_c = the time for the device voltage to reach its clamping voltage

t_2 = the time for the device voltage to decay to 50% of its overshoot value

t_1 = the time for the device voltage to reach its peak value

$t_1 - t_c$ = response time

Figure 8— Graph Illustrating Voltage Overshoot, Response Time, and Overshoot Duration

6.4 Response Time, Overshoot Duration (See Fig 8)

Due to the high frequencies effects involved in steep wavefronts, response time and overshoot duration measurements require special fixtures and extremely fast-responding instrumentation. Response time and overshoot duration may be a function of the wave form used for the measurement. Except for special applications, a separate test for response time and overshoot duration are not a necessary design test.

7. Bibliography

[1] ANSI/IEEE C62.1-1984, IEEE Standard for Surge Arresters for AC Power Circuits

[2] ANSI/IEEE Std 4-1978, IEEE Standard Techniques for High Voltage Testing

[3] ANSI/IEEE Std 100-1984, IEEE Standard Dictionary of Electrical and Electronics Terms

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