IEEE Std 824™-2004
(Revision of
IEEE Std 824-1994)

IEEE Standards

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IEEE Standard for Series Capacitor Banks in Power Systems

IEEE Power Engineering Society

Sponsored by the
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IEEE

3 Park Avenue, New York, NY 10016-5997, USA

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IEEE Std 824™-2004
(Revision of
IEEE Std 824-1994)

IEEE Standard for Series Capacitor Banks in Power Systems

Sponsor

Transmission and Distribution Committee
of the
IEEE Power Engineering Society

Approved 7 February 2005

American National Standards Institute

Approved 15 November 2004

IEEE-SA Standards Board

Abstract: This standard represents a significant update to IEEE 824-1994. Series capacitor bank component and bank duty cycle ratings, equipment insulation levels, protective functions, component testing, instruction books, nameplates, and safety are covered in this standard.
Keywords: bypass gap, capacitor bank, capacitor segment, discharge reactor, metal-oxide varistor, protective level, reactive compensation, series capacitor, series compensation, SSR, trigger circuit, triggered gap, varistor

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Introduction

This introduction is not part of IEEE Std 824-2004, IEEE Standard for Series Capacitor Banks in Power Systems.

The purpose of this revision is to include additional approaches for capacitor fusing and references to new IEEE and IEC standards for related equipment. An additional purpose was to increase the precision and clarity of the wording to make it more consistent with actual industry practice.

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This standard is dedicated to the memory of our friend and colleague
Stan Miske

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IEEE Standard for Series Capacitor Banks in Power Systems

1. Scope

This standard applies to outdoor series capacitor banks and to the major components of a bank that are required to form a complete system for the insertion of capacitors in series with a transmission line. These major components include capacitors, varistors, bypass gaps, bypass switches, discharge current limiting reactors, insulated structures, and protection and control systems. This standard defines the major requirements for the bank and these components. Design and production tests for all of the components are outlined. Disconnect switches associated with the series capacitor bank are not discussed in detail.

This standard applies to fixed series capacitor banks where the inserted reactance is primarily established by the reactance of the capacitors. Not included in this standard are power electronic devices for the insertion or bypassing of the bank. In addition, series capacitor banks applied to distribution circuits are not within the scope of this standard.

2. References

This standard shall be used in conjunction with the following publications. In case of discrepancies between this standard and the referenced standards, this standard takes precedence. Where a specific clause is cited in the text of this document, the following standards should be used. When the following standards are superseded by an approved revision, the revision shall apply, and the reference clauses must be checked for accuracy.

Accredited Standards Committee C2-2002, National Electrical Safety Code® (NESC®).[1]

ANSI C29.8-1985 (Reaff 2002), American National Standard for Wet-Process Porcelain Insulators (Apparatus, Cap, and Pin Type).[2]

ANSI C29.9-1983 (Reaff 2002), American National Standard for Wet-Process Porcelain Insulators (Apparatus, Post-Type).

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ANSI C37.06–2000, American National Standard for AC High-Voltage Circuit Breakers Rated on Symmetrical Current Basis-Preferred Ratings and Related Required Capabilities.

ANSI Z55.1-1967 (Reaff 1973), American National Standard for Gray Finishes for Industrial Apparatus and Equipment.[3]

IEC 60071-1:1993, Insulation Coordination—Part 1: Definitions, Principles, and Rules.[4]

IEC 60071-2:1996, Insulation Coordination—Part 2: Application Guide.

IEC 60099-4:2004, Surge Arresters—Part 4: Metal-Oxide Surge Arresters without Gaps for AC Systems.

IEC 60694:1996 (Reaff 2002), Common Specifications for High-Voltage Switchgear and Controlgear Standards.

IEC/PAS 62271-100:2003, High-Voltage Switchgear and Controlgear—Part 100: High-Voltage Alternating-Current Circuit Breakers.

IEC 62271-109:2002, High-Voltage Switchgear and Controlgear—Part 109: Alternating-Current Series Capacitor Bypass Switches.

IEEE Std 4™-1995, IEEE Standard Techniques for High-Voltage Testing.[5,6]

IEEE Std 18™-1992, IEEE Standard for Shunt Power Capacitors.

IEEE Std 693™-1997, IEEE Recommended Practices for Seismic Design of Substations.

IEEE Std 980™-1994, IEEE Guide for Containment and Control of Oil Spills in Substations.

IEEE Std 1036™-1992, IEEE Guide for Application of Shunt Power Capacitors.

IEEE Std 1313.1™-1996, IEEE Standard for Insulation Coordination—Definitions, Principles, and Rules.

IEEE Std 1313.2™-1999, IEEE Guide for the Application of Insulation Coordination.

IEEE Std C37.09™-1999, IEEE Standard Test Procedure for AC High-Voltage Breakers Rated on a Symmetrical Current Basis.

IEEE Std C37.1™-1994, IEEE Standard Definition, Specification and Analysis of Systems Used for Supervisory Control, Data Acquisition, and Automatic Control.

IEEE Std C37.30™-1997, IEEE Standard Definitions and Requirements for High-Voltage Switches.

IEEE Std C37.90™-1989 (Reaff 1994), IEEE Standard for Relays and Relay Systems Associated with Electric Power Apparatus.

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[3]ANSI Z55.1-1967 has been withdrawn; however, copies can be obtained from Global Engineering Documents, 15 Inverness Way East, Englewood, CO 80112, USA (http://global.ihs.com/).

[4]IEC publications are available from the Sales Department of the International Electrotechnical Commission, Case Postale 131, 3, rue de Varembé, CH-1211, Genève 20, Switzerland/Suisse (http://www.iec.ch/). IEC publications are also available in the United States from the Sales Department, American National Standards Institute, 25 West 43rd Street, 4th Floor, New York, NY 10036, USA (http://www.ansi.org/).

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IEEE Std C37.90.2™-2004, IEEE Standard for Withstand Capability of Relay Systems to Radiated Electromagnetic Interference from Transceivers.

IEEE Std C57.12.00™-2000, IEEE Standard General Requirements for Liquid-Immersed Distribution, Power, and Regulating Transformers.

IEEE Std C57.13™-1993, IEEE Standard Requirements for Instrument Transformers.

IEEE Std C57.16™-1996, IEEE Standard Requirements, Terminology, and Test Code for Dry-Type Air-Core Series-Connected Reactors.

IEEE Std C57.19.00™-1991 (Reaff 1997), IEEE Standard General Requirements and Test Procedures for Outdoor Power Apparatus Bushings.

IEEE Std C62.11™-1999, IEEE Standard for Metal-Oxide Surge Arresters for Alternating Current Power Circuits (>1 kV).

3. Definitions

The meaning of other terms used in this standard shall be as defined in *The Authoritative Dictionary of IEEE Standards Terms,* Seventh Edition [B4].[7]

3.1 ambient temperature: The temperature of the air into which the heat of the equipment is dissipated.

3.2 bypass current: The current flowing through the bypass switch, protective device, or other devices in parallel with the series capacitor.

3.3 bypass gap: A system of specially designed electrodes arranged with a defined spacing between them, in which an arc is initiated to form a low-impedance path around one segment or a subsegment of the series capacitor bank. The conduction of the bypass gap is typically initiated to limit the voltage across the series capacitors and/or limit the duty to the varistor connected in parallel with the capacitors. The bypass gap includes the electrodes that conduct the bypass current, the triggering circuit (if any), and an enclosure.

NOTE—See Figure 1.[8]

3.4 bypass switch: A device such as a switch or circuit breaker used in parallel with a series capacitor and its protective device to bypass or insert the series capacitor bank for some specified time or continuously. This device shall also have the capability of bypassing the capacitor during specified power system fault conditions. The operation of the device is initiated by the capacitor control, remote control, or an operator. The device may be mounted on the platform or on the ground near the platform.

NOTE—See Figure 1.

3.5 capacitor element: The basic component of a capacitor unit consisting of two electrodes separated by a dielectric.

3.6 capacitor rack: A frame that supports one or more capacitor units.

[7]The numbers in brackets correspond to those of the bibliography in Annex C.

[8]Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

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3.7 capacitor unit: *See:* **power capacitor.**

3.8 discharge current limiting reactor: A reactor to limit the current magnitude and provide damping of the oscillatory discharge of the capacitors during a closing operation of the bypass switch or the start of conduction of the bypass gap.

NOTE—See Figure 1.

3.9 discharge device: An internal or external device permanently connected in parallel with the terminals of a capacitor for the purpose of reducing the trapped charge after the capacitor bank is disconnected from the energized power system.

3.10 external fuse (of a capacitor unit): A fuse located outside of the capacitor unit that is connected in series with the unit.

3.11 external line fault: A fault that occurs on adjacent lines or equipment other than on the transmission line that includes the series capacitor installation.

3.12 forced-triggered bypass gap: A bypass gap that is designed to operate on external command on quantities such as varistor energy, current magnitude, or rate of change of such quantities. The sparkover of the gap is initiated by a trigger circuit. After initiation, an arc is established in the power gap. Forced-triggered gaps typically spark over only during internal faults.

3.13 fuseless capacitor bank: A capacitor bank without any fuses, internal or external, that is constructed of (parallel) strings of capacitor units. Each string consists of capacitor units connected in series.

3.14 insertion: The opening of the capacitor bypass switch to insert the series capacitor bank in series with the line.

3.15 insertion current: The root-mean-square (rms) current that flows through the series capacitor bank after the bypass switch has opened. This current may be at the specified continuous, overload, or swing current magnitudes.

3.16 insertion voltage: The peak voltage appearing across the series capacitor bank upon the interruption of the bypass current with the opening of the bypass switch.

3.17 insulation level: The combination of power frequency and impulse test voltage values that characterize the insulation of the capacitor bank with regard to its capability of withstanding the electric stresses between platform and earth, or between platform-mounted equipment and the platform.

3.18 internal fuse (of a capacitor): A fuse connected inside a capacitor unit, in series with an element or a group of elements.

3.19 internal line fault: A fault that occurs on the transmission line section that includes the series capacitor installation.

3.20 internally fused capacitor (unit): A capacitor unit that includes internal fuses.

3.21 main gap: The part of the bypass gap that carries the fault current after sparkover of the bypass gap.

3.22 platform: A structure that supports one or more segments of the bank and is supported on insulators compatible with line-to-ground insulation requirements.

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3.23 platform-to-ground communication insulator: An insulator that encloses communication signal paths between platform and ground level.

3.24 power capacitor (capacitor, capacitor unit): An assembly of dielectric and electrodes in a container (case), with terminals brought out, that is intended to introduce capacitance into an electric power circuit.

3.25 protective device: A bypass gap, varistor, or other device that limits the voltage on the capacitor segment or subsegment to a predetermined level when overcurrent flows through the series capacitor.

3.26 protective level: The magnitude of the maximum peak of the power-frequency voltage allowed by the protective device during a power system fault. The protective level may be expressed in terms of the actual peak voltage across a segment or subsegment or in terms of the per unit of the peak of the rated voltage across the segment or subsegment.

NOTE—See 5.5.

3.27 reinsertion: The restoration of load current to the series capacitor from the bypass path.

3.28 reinsertion current: The transient current, power-frequency current, or both, flowing through the series capacitor bank after the opening of the bypass path.

3.29 reinsertion voltage: The transient voltage, steady-state voltage, or both, appearing across the series capacitor after the opening of the bypass path.

3.30 series capacitor bank: A three-phase assembly of capacitor units with the associated protective devices, discharge current limiting reactors, protection and control system, bypass switch, and insulated support structure that has the primary purpose of introducing capacitive reactance in series with an electric circuit.

3.31 series capacitor installation: An installed series capacitor bank complete with disconnect switches.

3.32 segment: A single-phase assembly of capacitor units and an associated protective device, discharge current limiting reactor, protection and control functions, and one phase of a bypass switch. Segments are not normally separated by isolating disconnect switches. More than one segment can be on the same insulated platform.

NOTE—See Figure 1.

3.33 subsegment: A portion of a segment that includes a single-phase assembly of capacitor units and an associated protective device, discharge current limiting reactor, and selected protection and control functions, but does not have a dedicated bypass switch.

NOTE—See Figure 1.

3.34 switching step: A three-phase assembly that consists of one segment per phase, with a three-phase operating bypass switch for bypassing or inserting the capacitor segments. This is sometimes referred to as a capacitor module.

NOTE—See Figure 1.

3.35 thyristor protected series capacitor bank (TPSC): A fixed series capacitor bank equipped with thyristor valve configured to fast bypass and/or to provide capacitor overvoltage protection. The thyristor valve circuit consists of a series of anti-parallel thyristor levels and a current-limiting reactor. In a TPSC application, the thyristor is switched to a conductive condition at the specified protection level by the control and

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protection system. When the line current returns to nominal value or the bypass switch closes, the thyristor valve is blocked.

NOTE—See A.3.

3.36 trigger circuit: The part of the bypass gap that initiates the sparkover of the bypass gap at a specified voltage level or by external command.

3.37 valve element (of a varistor unit): A single nonlinear resistor disc used in a surge arrester or varistor unit.

3.38 varistor: An assembly of varistor units that limit overvoltages to a given value. In the context of series capacitor banks, the varistor is typically defined by its ability to divert fault current around the series capacitor units, limiting the voltage to a specified protective level while absorbing energy. The varistor is designed to withstand the temporary overvoltages and continuous operating voltage across the series capacitor units.

3.39 varistor coordinating current: The varistor current magnitude associated with the protective level. The varistor coordinating current waveform is considered to have a virtual front time of 30 μs to 50 μs. The tail of the waveform is not significant in establishing the protective level voltage.

3.40 varistor energy rating: The maximum energy the varistor can absorb within a short period of time without being damaged due to thermal shock or thermal runaway during the subsequent applied voltage. This rating is based on the duty cycle defined by the purchaser. This is the usable rating after taking into account factors such as current sharing among parallel columns. The additional energy absorption capability of the spare units is not normally included in this rating.

3.41 varistor maximum continuous operating voltage (MCOV): The rated rms voltage of the capacitor segment that the varistor is connected across.

3.42 varistor unit: A single insulated enclosure containing one or more valve elements in series and possibly in parallel.

3.43 voltage-triggered bypass gap: A bypass gap that is designed to spark over on the voltage that appears across the gap terminals. The sparkover of the gap is normally initiated by a trigger circuit set at a specified voltage level. A voltage-triggered bypass gap may be used for the primary protection of the capacitor and may spark over during external as well as internal faults.

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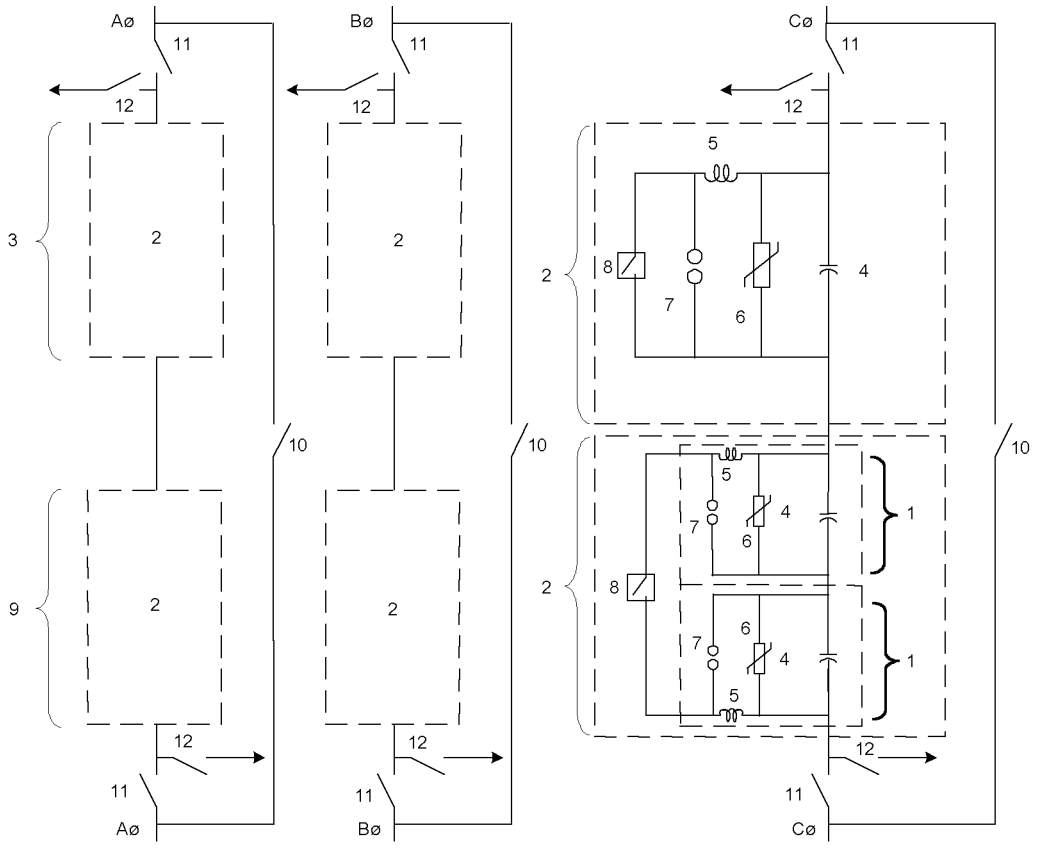

1—Subsegment (1ø)
2—Segment (1ø)
3—Switching step (3ø) or module (3ø)
4—Capacitor units
5—Discharge current limiting reactor
6—Varistor
7—Bypass gap
8—Bypass switch
9—Additional switching steps when required
10—External bypass disconnect switch
11—External isolating disconnect switch
12—External grounding disconnect switch
3, 9—Included in a series capacitor bank
3, 9, 10, 11, 12—Included in a series capacitor installation

Figure 1—Typical series capacitor installation nomenclature

4. Service conditions

4.1 Normal service conditions

Series capacitor banks shall be suitable for operation at the specified bank and equipment ratings and duty cycle sequence under the following conditions:

a) The elevation does not exceed 1000 m above sea level.

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b) The indoor and outdoor ambient temperatures are within the limits specified by the purchaser (see 5.2).

c) The ice load does not exceed 19 mm (if applicable).

d) Wind velocities are no greater than 128 km/h.

e) The horizontal seismic acceleration (if applicable) of the equipment does not exceed 0.2 g, and the vertical acceleration does not exceed 0.16 g, when applied simultaneously at the base of the support insulators. For the purposes of this standard, the values of acceleration are static. This is the *low seismic level* defined in IEEE Std 693-1997.[9] The seismic acceleration and the maximum wind do not have to be considered to occur simultaneously.

f) The snow depth (if applicable) does not exceed the height of the foundations for the platform support insulators. (A typical maximum height is 1 m.)

g) Maximum solar radiation in watts per square meter as specified by the purchaser.

4.2 Abnormal service conditions

The application of series capacitor banks at other than the normal service conditions shall be considered as special and should be identified in the purchaser's specification. Examples of such conditions are as follows:

a) Service conditions other than those listed in 4.1

b) Exposure to excessively abrasive and conducting dust

c) Exposure to salt, damaging fumes, or vapors

d) Swarming insects

e) Flocking birds

f) Conditions requiring over-insulation or extra leakage distance on insulators

g) Unusual transportation or storage conditions

h) Seismic accelerations at the *moderate or high seismic qualification levels* as defined in IEEE Std 693-1997

4.3 Abnormal power system conditions

Examples of abnormal power system conditions are as follows:

a) Significant continuous harmonic currents in the transmission line

b) The transmission line on which the series capacitor bank is located does not have phase transpositions, so the reactances of each phase of the line are not approximately equal.

5. Ratings

5.1 Fundamental bank ratings

The following items are the fundamental ratings for a series capacitor bank for a specific application:

a) *Rated system voltage*—The maximum continuous power system phase-to-phase rms voltage for which the phase-to-ground insulation system is designed.

b) *Rated frequency*—The frequency (measured in Hz) of the power system for which the capacitor bank is designed.

[9]Information on references can be found in Clause 2.

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c) *Rated reactance (X_C)*—The capacitive reactance for each phase of the series capacitor bank at its rated frequency with internal dielectric temperature of 25 °C. The maximum tolerance for this reactance is shown in Table 1.

Table 1—Maximum tolerances

Bank three-phase Mvar	Maximum difference of any phase from rated reactance	Maximum reactance difference among phases
Less than 30 Mvar	±5%	3%
30 Mvar or more	±3%	1%

The reactance change with ambient temperature at rated frequency shall be less than 0.1% per °C.

The total reactance per phase shall be divided among the number of segments as defined by the purchaser.

d) *Rated continuous current (I_R)*—The rms current that the capacitor or capacitor bank shall be capable of carrying continuously at rated frequency and rated ambient temperature range.

e) *Rated segment voltage (V_R)*—The rated rms voltage across a segment when the segment is carrying rated current.

f) *Reactive power rating (Q_R)*—The reactive power rating for the bank, as determined from rated reactance and rated current per phase, may be calculated using Equation (1):

$$Q_R = 3\, I_R^2 X_C \tag{1}$$

where

Q_R is the reactive power rating in Mvar,
I_R is the rated current (kA),
X_C is the rated reactance of each phase (ohms).

5.2 Ambient temperature

The series capacitor equipment shall be designed for energization, continuous operation, and short-time overloads in an outdoor environment with an ambient temperature range as specified by the purchaser. This shall apply to all equipment that is associated with the series capacitor bank located outdoors. The heating caused by the close proximity of some of the series capacitor bank equipment and by exposure to sunlight shall be accounted for in the design.

In the case of series capacitor bank equipment such as the ground-level protection and control that is to be located in a control building, the design of that indoor equipment shall be consistent with the temperature range within the building. IEEE Std C37.1-1994 provides guidance for buildings with different types of heating and cooling.

5.3 Component current ratings

The series capacitor bank shall be capable of withstanding continuous rated current, system swing currents, emergency loading, power system faults, and in some applications, harmonic currents. Some of these

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conditions are illustrated in Figure 2. These quantities are generally specified by the purchaser and can include different values for inserted and bypassed operating modes. Figure 2 identifies considerations used in establishing the specified current levels for the major components under both operating modes.

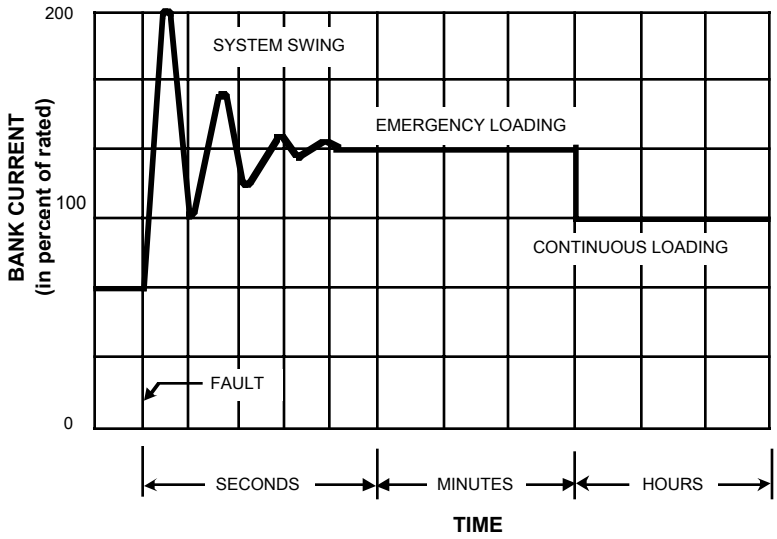

Figure 2—Typical current-time profile of an inserted capacitor bank following the fault and clearing of parallel lines. The fault current is not shown.

5.3.1 Bank inserted operating mode

5.3.1.1 Capacitor units

The capacitance of the segment is realized by connecting capacitor units in series and parallel to provide the required capacitive reactance with the continuous current rating. The capacitors shall also be designed to withstand higher currents, such as those experienced during emergency loadings (typically the 30 min rating), system swings, and faults (see 5.5) as specified by the purchaser. These requirements can impact the design. Figure 2 shows a typical current-time profile.

The capacitor units shall be designed to withstand the specified continuous rated current, emergency loading, swing current, and power system faults with the maximum capacitor unbalance condition for which the control and protection system will allow the bank to remain in service.

The capacitor fuses, either internal or external, shall be designed to operate correctly for bank currents of 50% of rated current up to and including power system fault conditions.

5.3.1.2 Discharge current limiting reactor

Typically, the discharge current limiting reactor is connected as shown is Figure 1, and hence does not carry current when the bank is inserted. However, in some applications the discharge current limiting reactor is connected in series with the capacitors. This arrangement is infrequently used to reduce losses where the segment is frequently bypassed and may be used to eliminate the potential for harmonic current magnification where the reactor is paralleled with the capacitor during bypassed operation. It is also used to reduce the duty on the disconnect switch typically used in parallel with the bank (see 5.3.2 and 5.5.2).

If the discharge current limiting reactor is in series with the capacitors, the reactor shall be rated to withstand the same current magnitudes and durations as required for the capacitor segment (see 5.5.2).

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5.3.1.3 Varistor

Current through the capacitor segment produces a voltage stress across the varistor. The varistor shall be designed to withstand these stresses. The varistor protective level shall be sufficiently above the voltage produced during a system swing to avoid excessive energy absorption during the swing.

5.3.1.4 Bypass switch and bypass gap

As in the case of the varistor, the interrupter of the bypass switch and the bypass gap are also exposed to voltages resulting from currents through the capacitors. In addition, this equipment is exposed to protective level voltage during power system faults. This equipment shall be designed to withstand these voltages.

5.3.2 Bank bypassed operating mode

The continuous, emergency, swing, and fault currents specified for this mode of operation may be different from those selected for the bank inserted mode based on power system operational considerations. Thus the purchaser should also specify the current ratings for this operating mode.

5.3.2.1 Discharge current limiting reactor

When the discharge current limiting reactor is in the typical position in the bypass path (as shown in Figure 1), the circuit is exposed to the continuous, emergency, swing, and fault currents specified for this mode of operation. The circuit shall be designed for these conditions. The maximum duration of the fault current will be the extended fault clearing condition (backup power system relaying) defined as part of the fault duty cycle for the bank (see 5.4), unless the purchaser specifies a 1, 2, or 3 s requirement.

If there are significant harmonic currents anticipated in the transmission line, these currents should be specified by the purchaser as an abnormal service condition. Harmonic current can be important because, if the bypass switch is in the closed position, the reactor is in parallel with the capacitors. This parallel inductor/capacitor circuit can circulate harmonic currents that are greater in magnitude than those present in the transmission line. This amplification can be significant for harmonic frequencies that are near the natural frequency of the parallel inductor/capacitor circuit. Under such circumstances, it is necessary that the inductive reactance be selected to minimize harmonic current amplification and that the reactor be designed to withstand harmonics in addition to the power-frequency requirements. In addition, a protection function can be implemented to close the bypass disconnect switch in case of excess harmonic current in the reactor. If the bank is often in the bypassed condition and the harmonic current in the transmission line is significant, it may be desirable to eliminate the amplification of the harmonic current by the parallel inductor/capacitor by locating the discharge current limiting reactor in series with the capacitors. However, this arrangement can affect the magnitude of the voltage across the capacitors during power system faults (see 5.5.2).

5.3.2.2 Capacitors

When the bank is in the bypassed mode, the power-frequency current in the capacitors is very small. However, if the harmonic current conditions discussed in 5.3.2.1 prevail, the capacitors can also carry significant harmonic current. The capacitor design shall take this into account.

5.3.2.3 Bypass switch

The bypass switch is exposed to the continuous, emergency, swing, and fault currents specified for this mode of operation. The switch shall be designed for these conditions as well as having the capability to successfully open and insert the capacitor bank at the varistor protective level and withstand transient current occurring during closing to bypass the bank.

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5.3.3 Bypassing of the bank

The start of conduction of the bypass gap or the closure of the bypass switch will result in a capacitor discharge current. The parameters of the discharge current limiting reactor shall be selected to limit the magnitude of the discharge current and provide sufficient damping of the oscillations so that the discharge is within the capabilities of all the equipment of the bank.

All of the equipment included in the discharge path shall be designed for the magnitude and duration of the capacitor discharge current resulting from bypass with protective level voltage on the capacitors. This includes the bypass gap, the discharge current limiting reactor, the capacitors and fuses, and the interconnecting bus. If there is no bypass gap and the bypass switch operates during the fault, the design of the discharge current limiting reactor shall be consistent with the capabilities of the switch. The capacitor discharge current can combine with the power-frequency fault current. The bypass gap, discharge current limiting equipment, and the bypass switch shall be designed to withstand this combined current.

5.3.4 Bank ultimate ratings

If specified by the purchaser, the bank shall be designed such that it may be modified in the future to meet operating conditions. These requirements can include a higher current rating and/or a change in capacitive reactance as discussed in the following items a) and b). In addition, the possibility of higher power system fault currents in the ultimate stage must be considered, as this may impact the rating of the varistor, the bypass gap, and the discharge current limiting reactor.

The degree to which these various future changes are incorporated into the initial design of the bank shall be consistent with that specified by the purchaser. Impacts on the ratings of all the equipment, including the layout and mechanical design of the platform (including seismic and clearances), must be considered.

a) Increasing the current rating of a bank is accomplished by adding capacitors in parallel with those initially delivered. Therefore: (1) capacitor rack space must be available in the initial design, and (2) the other current-carrying components and protective elements must be designed to accommodate this change. However, this change will reduce the capacitive reactance of the bank and, as a result, the percent compensation provided for the associated transmission line. In some applications, this may be considered acceptable.

b) Increasing the current rating and maintaining or increasing the banks capacitive reactance requires that capacitors be added not only in parallel but also in series with those initially delivered. This significantly impacts the initial design of the bank. Bank and component design changes include the following:

   1) Platform and rack space to accommodate the additional capacitors in series and parallel.
   2) Varistor ratings to accommodate the future series section or space to install additional varistor units.
   3) Initially specified design of the bypass switch, bypass gap, and discharge current limiting reactor must account for the increased voltage stress and increased duty during a bypass operation. Alternately, provisions must be made for adding an additional gap and/or bypass switch and discharge current limiting reactors in the future.
   4) Increased insulation level for selected insulators and increased clearances.

5.4 Duty cycle

The equipment shall be designed to withstand the required sequences of faults, system swing currents, emergency loading, and continuous currents for the series capacitor bank as specified by the purchaser. These sequences form the duty cycles that all of the components of the bank shall be designed to withstand. The duty cycle should be consistent with the manner in which the surrounding power system will be operated for both internal and external line faults. The purchaser shall define duty cycles for faults of normal

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and extended durations and for faults of different types (three-phase and single-phase). Phase-to-phase faults shall be considered if specifically defined by the purchaser, as these can be decisive for the energy rating of the varistor.

Although the focus of this discussion is duty cycles involving faults on the power system, it is understood that the bank shall be designed to operate for other events, such as insertion under the conditions defined by the purchaser.

The purchaser specification shall include information about the magnitude of the fault currents that impact the series capacitor bank. Examples of approaches used to define this are as follows:

a) The parameters of the transmission lines on which the series capacitors are to be located and the equivalent short-circuit impedances for the surrounding power system at the terminals of those lines are defined by the purchaser. The supplier then uses this information to define the requirements of the protective device.
b) For banks with varistors, the duty to the varistor during faults is defined by the purchaser.

5.4.1 Normal external faults

Examples of duty cycles for normal external faults are as follows:

a) A varistor provides the primary overvoltage protection

1) The bank is initially in the inserted condition with rated continuous current.
2) An external fault occurs that is cleared within normal clearing time. The varistor will typically be required to withstand the duty associated with the fault. Bypassing the bank with a bypass gap or switch is not normally permitted. The restoration of all the current back in the series capacitor units following the clearing of the external line fault is immediate.
3) The bank is exposed to the swing current followed by the post-fault power current as specified by the purchaser. The post-fault power current may be at rated current or at the 30 min overload current followed by rated current.
4) The bank returns to operation at rated current.

b) A bypass gap provides the primary overvoltage protection

1) The bank is initially in the inserted condition with rated continuous current.
2) An external fault occurs that is cleared within normal clearing time. The bypass gap will be required to withstand either the voltage associated with the fault or be allowed to spark over. If the gap has been permitted to spark over, the bypass switch must reinsert the capacitors within the time specified by the purchaser, and the gap must not spark over on the resulting transient reinsertion voltage.
3) The bank is exposed to the swing current followed by the post-fault power current as specified by the purchaser. The post-fault power current may be at rated current or the 30 min overload current.
4) The bank returns to operation at rated current.

5.4.2 Normal internal faults

Examples of duty cycles for normal internal faults are as follows:

a) A varistor provides the primary overvoltage protection.

1) The bank is initially in the inserted condition with rated continuous current.
2) An internal fault occurs. Bypassing the bank with a bypass gap or the bypass switch is permitted. The varistor must withstand the duty that occurs prior to the completion of the bypass. The bypass gap and/or switch shall withstand the resulting capacitor discharge and power-frequency fault current. The line circuit breakers interrupt the fault.

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3) The line remains open until it is reclosed within the time specified by the purchaser. The bank must reinsert within the time specified by the purchaser. The speed of recovery of the dielectric voltage withstand of a bypass gap shall be consistent with the required reinsertion time.

4) If the line reclosing is successful and the fault is not present, the bank returns to operation at rated current. If the line reclosing is not successful and the bank was inserted prior to reclosure, the varistor must be capable of withstanding this additional duty until bypassing occurs.

b) A bypass gap provides the primary overvoltage protection

1) The bank is initially in the inserted condition with rated continuous current.

2) An internal fault occurs. Bypass with the bypass gap followed by optional switch closure is permitted. The bypass gap and/or switch shall withstand the resulting capacitor discharge and power-frequency fault current. The transmission line circuit breakers interrupt the fault.

3) The line remains open until it is reclosed within the time specified by the purchaser. The bank shall reinsert within the time specified by the purchaser. The speed of recovery of the dielectric voltage withstand of the gap must be consistent with the required reinsertion time.

4) If the line reclosing is successful and the fault is not present, the bank returns to operation at rated current. If the line reclosing is not successful and the bank was inserted prior to reclosure, the bypass gap shall spark over again as required to limit the voltage to the protective level.

The operation duty cycle of the bypass switch shall be consistent with the fault duty cycle required for the bank and other operational requirements specified by the purchaser.

5.5 Voltage limitation during power system faults

The series capacitor bank shall have a means of limiting the voltage across each segment or subsegment during power system faults. The protective device must limit the peak of the power-frequency voltage to the protective level for all power system fault or other conditions specified by the purchaser. Each segment or subsegment shall be capable of withstanding the voltages as limited by the protective device as established by the supplier or specified by the purchaser.

The voltage magnitude of the protective level of the protective device of a segment has the relationship shown in Equation (2) to the rated segment voltage:

$$V_{PL} = (pu)V_R\sqrt{2} \tag{2}$$

where

V_{PL} is the peak voltage magnitude of the protective level,
V_R is the rated rms segment voltage,
pu is the per unit magnitude of the protective level.

5.5.1 Voltage limitation when the inductance between the primary protective device and the capacitors is not significant

The following subclauses are applicable when the inductance between the primary protective device and the capacitors is not significant.

5.5.1.1 Voltage fired gap

In the case where the protective device is a voltage fired gap, the protective level is the maximum power-frequency sparkover voltage of the gap. For a protective system based on more than one gap, the protective level is the maximum power-frequency sparkover voltage of the gap with the highest sparkover voltage. As

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is typically the case, the inductance of the discharge current limiting reactor must be sufficiently low so that, during any specified power system fault, the voltage across the segment is less than the protective level.

5.5.1.2 Varistor without a forced bypass gap

For a protective system based on a varistor and no bypass gap, the protective level is based on the highest current that will flow through the varistor for the specified power system fault conditions. This highest current is either specified by the purchaser or is determined by computer simulations performed by the supplier based on power system information provided by the purchaser. The inductance of the bus-work between the varistor and the capacitors is not a significant factor.

5.5.1.3 Varistor with a forced bypass gap

In the case of a protective device consisting of a varistor and a forced-triggered bypass gap, the varistor coordinating current selected to define the protective level shall be based on either of the following:

a) The maximum varistor current for any fault condition, taking into account the control logic of the gap firing system and the associated time delays.

b) The varistor current threshold for which the gap will be triggered. For internal faults near the bank, the current through the varistor will briefly exceed this current threshold, and the associated varistor voltage will be correspondingly higher. The increased voltage is permitted, provided the duration of the increased voltage is less than 1 ms and the magnitude of the voltage does not exceed 90% of the capacitor terminal-to-terminal dc production test value or 90% of the peak of the power-frequency withstand of the segment insulation system.

The value selected for the varistor coordinating current may be dependent on the application requirements of the purchaser and is subject to agreement between the supplier and the purchaser. These current magnitudes are determined from computer simulations.

5.5.2 Voltage limitation when the inductance between the primary protective device and the capacitors is significant

In some applications, there is significant inductance between the primary protective device and the capacitors being protected. This creates the possibility that, during a power system fault, the voltage across the capacitors will be significantly higher than the maximum voltage across the protective device.

One circuit arrangement that creates this possibility is where the discharge current limiting reactor is connected in series with the capacitors. If a varistor is the primary protective device and it is connected across the series combination of the reactor and capacitors, the voltage across the capacitors can be higher than the voltage limited by the varistor. The magnitude of the difference in voltage is dependent on the inductance of the reactor and the available fault current from the power system. If this circuit arrangement is used, computer simulations shall be performed by the supplier to establish the magnitude of the voltage across the capacitors during the power system faults specified by the purchaser. The magnitude of the capacitor voltage shall be used as the effective protective level in determining the terminal-to-terminal dielectric test on the capacitor units and the insulation coordination for the capacitor assembly.

5.6 Phase-to-ground insulation levels

The phase-to-ground insulation for the series capacitor bank shall meet the withstand levels specified by the purchaser. These levels should be the consistent with the standard practice for nearby substations taking into account that the voltage on the platform support insulators may be higher than the voltage at the substation. Listed in Table 2 and Table 3 are various possible insulation levels that are consistent with ANSI and IEC standards. For installations at elevations significantly above 1000 m, an increased BIL may be required.

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The leakage distance (creepage distance) for the phase-to-ground insulators shall meet that specified by the purchaser.

The values specified shall apply to the platform-to-ground insulators, the line-to-ground insulators of the bypass switch, and the platform-to-ground communication equipment insulators.

Table 2—Standard withstand voltages for Class 1 and 2 (15 kV < V_m ≤ 800 kV)

	Withstand		
Maximum system voltage (phase-to-phase) V_m (kV rms)	**Low-frequency, short-duration withstand voltage (phase-to-ground) (kV rms)**	**Basic lightning impulse insulation level (phase-to-ground) BIL (kV crest)**	**Basic switching impulse insulation level (phase-to-ground) BSL (kV crest)**
15	34	95 110	
26.2	50	150	
36.2	70	200	
48.3	95	250	
72.5	95 140	250 350	
121	140 185 230	350 450 550	
145	230 275 325	450 550 650	
169	230 275 325	550 650 750	
242	275 325 360 395 480	630 750 825 900 975 1050	
362		900 975 1050 1175 1300	650 750 825 900 975 1050

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Table 2—Standard withstand voltages for Class 1 and 2 (15 kV < V_m ≤ 800 kV) *(continued)*

	Withstand		
Maximum system voltage (phase-to-phase) V_m (kV rms)	**Low-frequency, short-duration withstand voltage (phase-to-ground) (kV rms)**	**Basic lightning impulse insulation level (phase-to-ground) BIL (kV crest)**	**Basic switching impulse insulation level (phase-to-ground) BSL (kV crest)**
550		1300 1425 1550 1675 1800	1175 1300 1425 1550
800		1800 1925 2050	1300 1425 1550 1675 1800
NOTE—This table shows several withstand voltages for a given maximum rated voltage. The selected voltages are based on proper insulation coordination.			

Table 3—Selected typical insulation levels based on IEC 60071-1:1993 and IEC 60071-2:1996

	Withstand		
Maximum system voltage (kV rms)	**BIL (kV pk)**	**Switching impulse wet (kV pk)**	**Power frequency 1 min wet (kV rms)**
12	75		28
17.5	95		38
24	125		50
36	170		70
52	250	—	95
72.5	325	—	140
123	450 550	—	185 230
145	550 650	—	230 275
170	650 750	—	275 325
245	850 950 1050	—	360 395 460

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Table 3—Selected typical insulation levels based on IEC 60071-1:1993 and IEC 60071-2:1996 *(continued)*

	Withstand		
Maximum system voltage (kV rms)	**BIL (kV pk)**	**Switching impulse wet (kV pk)**	**Power frequency 1 min wet (kV rms)**
300	950 950 1050	750 850 850	
362	1050 1050 1175	850 950 950	
420	1175 1300 1425	950 1050 1050	
525	1425 1425 1550	1050 1175 1175	
765	1800 1950 2100	1300 1425 1550	

NOTES

1—Switching surge withstand is not defined for system voltages 245 kV and below.
2—Power-frequency withstand is not defined for system voltages 300 kV and above.
3—The introduction of Um = 550 kV (instead of 525 kV), 800 kV (instead of 765 kV), of a value between 765 kV and 1200 kV and of the associated standard withstands voltages, is under consideration.

5.7 Insulation levels for equipment and insulators on the platform

The insulation levels for insulators and series capacitor equipment mounted on the supporting platform are in reference to the platform. For installations at elevations above 1000 m, higher insulation levels may be required.

The wet withstand of the insulators and equipment on the platform shall be selected based on the protective level established by the protective device, using Equation (3). The relationship applies to the insulation across the entire segment using the protective level for the segment. It also applies to the insulation within the segment using the prorated protective level across that part of the segment.

$$K_{PFW} \geq 1.2 \times V_{PL} / \sqrt{2} \tag{3}$$

where

V_{PFW} is the power-frequency wet rms voltage-withstand level,
V_{PL} is the peak voltage magnitude of the protective level.

5.7.1 Insulators

The wet withstand of the insulators shall be selected based on the relationship shown in Equation (3). The insulator voltage class, BIL, and wet withstand values are determined by selecting an insulator with an

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equivalent or greater power-frequency wet withstand rating in accordance from Table 2 and Table 3. In this process, the left columns of the tables are not used.

5.7.2 Equipment insulators

In general, the power-frequency insulation level of the equipment on the platform shall be established by the relationship shown in Equation (3) with some exceptions.

5.7.2.1 Capacitor units

The minimum insulation level for the capacitor bushings is selected based on the power-frequency wet withstand test voltage. Standard insulation levels of the capacitor bushings as defined in IEEE Std 18-1992 are as shown in Table 4.

Table 4—Electrical characteristics of bushings

		Withstand test voltage		
BIL	**Minimum insulation creepage distance (mm)**	**60 Hz dry 1 min (kV rms)**	**60 Hz wet 10 s (kV rms)**	**1.2/50 μs impulse (kV pk)**
30	51	10	6	30
75	140	27	24	75
95	250	35	30	95
125	410	42	36	125
150	430	60	50	150
200	660	80	75	200

5.7.2.2 Bypass switch

The power-frequency wet withstand level across the interrupter of the bypass switch shall be based on the relationships defined in Equation (3).

5.7.2.3 Varistor

The power-frequency wet withstand level of the varistor insulated enclosure shall be based on the relationships defined in Equation (3), taking into account the portion of segment voltage to which the enclosure is exposed. It is not required that the insulation level be selected from the standard values contained in Table 2 and Table 3.

5.7.2.4 Bypass gap

The insulators used in the bypass gap shall be based on the relationships defined in Equation (3), taking into account the portion of the segment voltage to which the bypass gap is exposed. Intermediate assemblies can see high transients during the normal breakdown process and must be designed for these conditions. In addition, the withstand level of the power gap and any trigger circuit shall be coordinated to withstand all system disturbances without sparking over under power system conditions for which this is inappropriate.

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5.7.2.5 Discharge current limiting reactor

The insulators used to support the discharge current limiting reactor from the platform shall be based on the relationships defined in Equation (3), taking into account the portion of the segment voltage to which these insulators are exposed. The level shall be selected from the standard values included in Table 2 or Table 3.

The insulation level across the discharge current limiting reactor shall be selected based on instantaneous voltage appearing across the circuit when the bypass gap starts conducting or the bypass switch closes. The power-frequency withstand of the required insulation class must be at least times this instantaneous voltage. The BIL of the circuit is then selected from Table 2 or Table 3. However, it must be recognized that the voltage that appears across the circuit when the bypass gap conducts or the bypass switch closes is of a much higher frequency than 50 Hz or 60 Hz and that the duration is very brief. At 50 Hz or 60 Hz, the magnitude of impedance of the circuit is usually very small, making it virtually impossible to perform a power-frequency voltage-withstand test at the selected level. On the other hand, the reactor can be easily tested with an impulse. As a result, the primary focus of the insulation across the reactor is its BIL.

5.7.3 Leakage distance

If the purchaser specifies that the platform-to-ground insulators have extra leakage distance, the insulation on the platform shall have commensurate leakage distance. The insulators on the platform must then be selected to have at least the same ratio of leakage distance to rated operating voltage, as is the case for the specified phase-to-ground insulators with respect to the phase-to-ground maximum system voltage. When the 30 min overload rating exceeds 1.35 pu, the equipment leakage distances shall increase linearly above this level.

5.7.4 Air clearances

The air clearances on the platform shall be selected to have a power-frequency withstand of at least $1.2/\sqrt{2}$ times the prorated protective level voltage at all points in the equipment arrangement. The formulas in IEC 60071-2:1996, Appendix G, shall be used for this purpose.

6. Protection, control, and indication

The series capacitor bank is continuously monitored and protected by a protection and control system. The system provides indications (or alarms) for various system conditions and equipment failures or malfunctions. This clause only covers the protective aspects relating to the protection and control of the series capacitor equipment. It is generally the responsibility of the transmission line protection system to detect faults from the series capacitor platform to ground.

General information about series capacitor protection is contained in the IEEE Special Publication TP-126-0 [B5].

6.1 Protection and control functions

The series capacitor bank shall be provided with the following protection and control functions, as applicable. These functions are divided into four basic categories, as follows:

a) Protection functions against overstress from system conditions

1) Capacitor overload protection—This is a function of the specified overload current requirements for the bank and utility practices.

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2) Varistor fault energy protection—This function is achieved by measuring varistor current and deducing varistor energy. This function may also include monitoring the magnitude of the varistor current.

3) Varistor over-temperature protection—This function is achieved by measuring varistor current and deducing varistor temperature.

4) Bypass gap protections—Bypass gap protections typically include detection of prolonged gap conduction.

5) Discharge current limiting reactor harmonic overcurrent protection (optional)—This function detects excessive harmonic current in the reactor.

b) Protection functions associated with equipment failure or malfunction

1) Capacitor unbalance

2) Platform fault

3) Bypass gap failure

4) Varistor failure

5) Bypass switch failure

6) Pole disagreement

7) Protection and control system failure

c) Control functions

1) Bypassing

2) Insertion (automatic or manual) and reinsertion

3) Lockout

4) Temporary block insertion

5) Operation of disconnect switches

d) *Power system protection (optional)*—These functions are intended to limit the exposure of the power system to possible interactions between the power system and the series capacitor. This group includes subharmonic and subsynchronous protections. These protections are frequently used on series capacitors in distribution circuits but have limited applicability in transmission systems.

A summary of the preceding protections, including the typical resultant protective actions, is presented in Table 5. The table is for a series capacitor bank with one switching step that has a protective device consisting of a varistor and a forced bypass gap. Some protective actions may be different if there is a redundant protection system. In Table 5, the column labeled *local indications* relates to labeled visual indications at the series capacitor protection system. A *3* in the column means that the indication is typically provided on an individual phase basis. A *1* in the column means that the indication is typically provided on bank basis. The column labeled *remote indications* relates to outputs provided to the purchaser's SCADA system.

The purchaser should specify the protective functions and the indications that are required.

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Table 5—Summary of typical protection indications and actions

	Indications		Protection actions		
Condition	**Local**	**Remote**	**Switch/ closes**	**Lockout**	**Gap fires**
Capacitor unbalance—level 1	3	1			
Capacitor unbalance—level 2	1	1	X	X	
Capacitor overcurrent	3	1	X		
Flashover to platform	3	1	X	X	
Varistor energy/current					X (See Note 1)
Varistor over-temperature—level 1	3	1			
Varistor over-temperature—level 2	1	1	X		X (See Note 2)
Varistor failure	3	1	X	X	(See Note 3)
Gap conduction	3	1	X (See Note 4)		
Prolonged gap conduction		1	X	X	
Gap failure to bypass	3	1	X	X	
Bypass switch pole discordance	1	1	X	X	
Communication failure	3	1	X	X	
Lockout	1	1	X	X	
Abnormal platform power supply	3	1	X	X	
Ground control undervoltage	1	1	X	X	
Controller failure	1	1	X	X	
Bypass switch/low SF6—level 1	1	1			
Bypass switch/low SF6—level 2	1	1	X	X	
Bypass switch/low stored energy—level 1	1	1			
Bypass switch/low stored energy—level 2	1	1	X	X	

NOTES

1—If the protective device is a varistor with no forced bypass gap, the bypass switch will be closed for this condition.
2—In some systems, the bypass gap is also fired for varistor over-temperature if there is sufficient voltage across the gap.
3—Varistor failure may result in the triggering of the bypass gap. However, the gap may not fire reliably since the voltage across it will likely be low due to the faulted varistor. This is, however, not a protection action since the varistor has already failed.
4—In some applications, the bypass switch is closed whenever the bypass gap conducts.

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6.2 Protection redundancy

The protection system shall be designed with at least the level of redundancy specified by the purchaser. Items that may be specified to have redundancy are shown in the following list. It may also be specified by the purchaser that the two protection systems be physically separate, each in its own cabinet. The purchaser may specify if the protection system is to be operated from one or two station batteries and the degree of separation between the supplies that is required within the series capacitor bank protection and control system.

a) Digital controllers and relays
b) Power supplies
c) Platform-to-ground communication insulators
d) Current transformers and current sensors
e) Circuits to trigger the forced-triggered gap
f) Closing coils for the bypass switch

6.3 Capacitor unit fusing and unbalance protection

The bank shall be provided with a system to detect capacitor unit/element failures and alarm and bypass the bank if it becomes necessary. Three approaches may be used to achieve this objective, as described in 6.3.1, 6.3.2, and 6.3.3. The test levels for the capacitors and fuses defined in Clause 7 are consistent with the indicated alarm and bypass thresholds. These shall be the basis of the design unless otherwise specified by the purchaser. It is important to note that the magnitude of unbalance currents can vary significantly depending on the design of the capacitor units and how they are interconnected to form the bank. The design of the protection system must carefully consider these factors to avoid nuisance alarms and false bypass events.

It should be recognized that a capacitor unbalance condition could contribute significant additional voltage stress on some units or elements within a bank. A common maximum degree for this *unbalance factor* for which the unbalance protection will allow the bank to remain in service is 1.1 pu on unfaulted units in series or parallel with the faulty unit. The unbalance factor is the additional voltage on the units or elements remaining in service, resulting from elements or units shorted and fuses opened, in per unit of the voltage that would exist if the capacitors and fuses were all in a normal state. This unbalance factor causes a proportionate increase in the capacitor unit/element stresses during overloads and power system faults that a series capacitor bank typically experiences. For example, if the protective level of the bank is 2.3 pu and the unbalance factor is 1.1 pu, then a group of capacitor units or elements will experience a voltage of 2.3 × 1.1 = 2.53 pu. If the terminal-to-terminal test on the capacitor units is performed with the minimum test voltage of 4.3 times the rms rated voltage of the units as defined in 7.1.2.1, the test voltage level is $4.3/\sqrt{2} = 3.04$ pu. The latter value is the ratio of the dc test level to peak value of the rated voltage of the capacitor units. For this example, the protective margin between the protective level including the unbalance factor (2.53 pu) and the test voltage (3.04 pu) is 20%.

6.3.1 Capacitor units with external fuses

The typical arrangement used with externally fused capacitors involves the connection of groups of fused capacitors in parallel as necessary to meet the current rating of the bank. These groups are connected in series to realize the voltage and impedance ratings of the bank. The capacitor units of each segment or subsegment are split into two or more parallel strings to allow capacitor current unbalance detection.

The failure of a capacitor unit results in increased current in the external fuse and blowing of the fuse. This in turn results in increased voltage on the parallel capacitor units. For the purposes of establishing the thresholds for the capacitor unbalance protection, it is typically assumed as a worst case that additional capacitor units will fail and fuses blow in the same parallel group. The thresholds for alarm and bypass for

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the capacitor current unbalance protection function are typically based on calculations of the increasing voltage across this worst capacitor group with an increasing number of blown fuses. Typically, an alarm occurs when the unbalance current is indicative of greater than a 1.05 pu unbalance factor, and bypass occurs when the unbalance current is indicative of factor of greater than a 1.1 pu. The objective of these thresholds is to restrict the operation of the capacitors and fuses to within their tested capabilities.

6.3.2 Fuseless capacitor arrangement

The typical arrangement used with fuseless capacitors involves strings of series-connected capacitor units. The number of units connected in series is as required to achieve the necessary voltage capability. These strings of capacitors are connected in parallel as necessary to realize the current and impedance ratings of the bank. The capacitor units of each segment or subsegment are split into two or more parallel groups of strings to allow capacitor current unbalance detection. The internal arrangement within the capacitor units consists of a number of series elements.

The failure of a capacitor element results in a short circuit of the associated element and of the elements that may be connected in parallel within that capacitor unit. This results in an increase in current through the remaining elements within that capacitor unit and the other units in the associated string. For the purposes of establishing the thresholds for the capacitor unbalance protection, it is typically assumed as a worst case that additional capacitor elements will fail in the same string of capacitor units. The thresholds for alarm and bypass for the capacitor current unbalance protection function are typically based on calculations of the increasing voltage across the remaining capacitor elements in the worst capacitor string with an increasing number of shorted elements. Typically, an alarm occurs when the unbalance current is indicative of an unbalance factor of 1.05 pu to 1.1 pu or when the equivalent of more than 50% of the elements of a unit are shorted. Bypass typically occurs when the unbalance current is indicative of an unbalance factor greater than 1.15 pu to 1.2 pu or when the equivalent of all the elements of a unit have shorted. The objective of these thresholds is to restrict the operation of the capacitors to within their tested capabilities.

6.3.3 Capacitors with internal fuses

The typical arrangement used within an internally fused capacitor unit involves groups of fused elements connected in parallel. These groups are then connected in series to realize the rating for the unit. The units are connected in series and parallel as necessary to meet the overall ratings of the bank. A number of different arrangements are possible. The capacitor units of each segment or subsegment are split into two or more parallel strings to allow capacitor current unbalance detection. These strings are sometimes interconnected via a current transformer in a bridge arrangement.

The failure of a capacitor element results in increased current in the associated internal fuse and blowing of the fuse. This results in an important increase in the voltage across the parallel elements and a much smaller increase in the voltage across the group of capacitor units that are in parallel with the affected unit. The typical protection strategy has two parts: one for situations involving groups of capacitors, and one for situations within a unit.

6.3.3.1 Group of capacitor units

For a group of capacitor units, typically an alarm will be initiated when the unbalance current is indicative of an unbalance factor of 1.05 pu, and bypass occurs when the unbalance current is indicative of a factor of greater than 1.1 pu. The objective of these thresholds is to restrict the operation of the capacitors and fuses to within their tested capabilities.

6.3.3.2 Within one unit

For a situation within a capacitor unit, the worst condition involves increasing numbers of shorted elements and blowing fuses in the same group of parallel elements. In this case, bypass typically occurs when the

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unbalance current is indicative of a unbalance factor of greater than 1.5 pu to 2.0 pu with an alarm initiated when the unbalance current is indicative of an unbalance factor greater than 1.25 pu to 1.5 pu. The objective of these thresholds is to restrict the operation of the fuses to within their tested capabilities (see 7.2.1.2). It is not expected that the affected capacitor elements will withstand these high overstresses continuously at rated current in the bank or during a 30 min overload condition or a power system fault that results in protective level voltage.

6.4 Bypass switch protection functions

The control circuits of the bypass switch shall be designed to give priority to closing over opening. In addition, the opening of the bypass switch shall be blocked if it is detected that the operational capabilities of the switch are impaired.

Additional protection functions related to the bypass switch are as follows. The exact implementation will be dependent on the type of mechanism and the type of insulation used in the switch and the requirements of the purchaser.

a) Detection of reduction of the properties of the internal dielectric
b) Detection of abnormal mechanism operation
c) Pole disagreement
d) Failure to close

If specified by the purchaser, a signal shall be provided that may be used to initiate the trip of the associated line, if the bypass switch fails to close when initiated by a bank protective function.

6.5 Bypass thyristor valve protection

In recent years to reduce the size and cost of the varistor, an alternate form of capacitor protection involving the use of thyristor valves has been developed. The thyristor valve operates much in the same manner as a varistor by commutating the line current away from the capacitor until either the current is at or below its rated value or the bypass switch closes. (See Figure A.1 and A.3 for more details.)

7. Testing

Tests on the equipment that constitute the series capacitor banks are designated as either design tests or production tests. Additional tests are typically performed after the bank is installed, as discussed in A.4.

a) *Design tests*— Design tests on the series capacitor bank equipment may be performed as outlined in the following subclauses. For a specific project, these tests shall demonstrate that the equipment to be provided complies with the requirements of the purchaser's specification. When a design test has previously been successfully performed on equipment of similar design at stress or duty levels that are equal to or greater than that required for the specific project, then the manufacturer does not have to repeat the test if a written report describing the previous test is provided. The manufacturer must also provide an explanation of how the previous test satisfies the requirements for the specific project. New design tests must be performed for a specific project only if the equipment design is new or if a critical manufacturing process is new, or if it is to be applied at a higher stress or duty level than previously tested designs, or if specifically contracted by the purchaser. The need for new design tests is assessed on an individual equipment basis.

   Data obtained during staged fault tests involving a complete series capacitor bank may be used to demonstrate the sufficiency of certain aspects of the design.

b) *Production tests*—Production tests shall be performed by the manufacturer on each component.

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7.1 Capacitors

The tests described in this subclause apply to externally fused, internally fused, and fuseless capacitor units. Differences in the tests for the different fuse types are only as noted.

The minimum rated voltage of the capacitor units is equal to the rated segment voltage (V_R) divided by the number of units in series.

7.1.1 Design tests

7.1.1.1 Capacitance change vs. temperature test

Test data shall be provided to verify that the capacitance change is within 0.1% /°C over a temperature range of –40 °C to +60 °C or as specified by the purchaser. The capacitance vs. temperature characteristic is dependent only on the dielectric materials and is not a function of capacitor unit rating. Therefore, it is not necessary to repeat the test if the unit rating being supplied is different from the tested unit as long as the dielectric materials are the same.

7.1.1.2 Thermal stability test

Testing shall be performed in accordance with IEEE Std 18-1992, except that all references to voltage should be changed to current, and references to capacitance should be changed to reactance. This test may be waived if a similar unit has passed this test. The thermal density of the tested unit shall be at least as high as that of the design to be qualified.

7.1.1.3 Radio influence voltage test

Radio influence voltage (RIV) tests on capacitor units shall be performed in accordance with the requirements given in IEEE Std 18-1992.

7.1.1.4 Short-circuit discharge test

The capacitor shall be tested at approximately 25 °C by charging to a dc voltage of 110% of the protective level and discharging through a circuit that limits the first peak of discharge current to not less than 120% of the current that flows when the capacitor is bypassed by the protective device or bypass switch. The damping of the capacitor discharge shall be such that the capacitor voltage and current at the end of the third half cycle of the oscillation shall be equal to or greater than that which will occur in the actual application. Three samples shall each be tested 25 times at intervals of less than 2 min.

After this test, the capacitor units shall be tested at approximately 25 °C by charging to a dc voltage equal to 110% of the maximum protective level and then discharging once through a circuit having an impedance as low as possible. The discharge circuit may be implemented with a small fuse wire or a shorting switch. The capacitance of each unit should be rechecked after the test, to determine if there is any adverse change. Any change in the capacitance of the unit shall be less than that associated with the shorting of one element or the operation of an internal fuse.

7.1.1.5 Voltage decay test

The capacitor unit should be charged to a dc voltage equal to the peak of the rated voltage and then isolated for 5 min. The residual voltage remaining on the capacitor unit after 5 min shall not exceed 50 V unless otherwise specified by the purchaser.

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7.1.1.6 Terminal-to-terminal dielectric test

Tests shall be performed in accordance with 7.1.2.1.

7.1.1.7 Terminal-to-case test

Tests shall be performed in accordance with the requirements given in IEEE Std 18-1992 and 7.1.2.2.

7.1.1.8 Impulse withstand test

Tests shall be performed in accordance with the requirements given in IEEE Std 18-1992.

7.1.1.9 Capacitor bushing test

Tests shall be performed in accordance with the requirements given in IEEE Std 18-1992. The test voltages must be consistent with 5.7.

7.1.2 Production tests

7.1.2.1 Terminal-to-terminal dielectric test

The capacitor units shall withstand a dc test voltage equal to a minimum of 120% of the peak value of the protective level. The dc test voltage shall be not less than 4.3 times the rated voltage of the unit. (This equates to $4.3/(1.2*\sqrt{2}) = 2.53$ pu.) If the protective device protects more than one group of units in series, the test voltage shall be prorated accordingly to determine the test voltage to be applied to each capacitor. This test shall be applied at a capacitor case temperature of 25 °C ± 5 °C for a period of 10 s. The capacitance shall be measured on each unit both before and after the application of the test voltage. A higher test voltage, based on specific application and capacitor protection considerations, may be specified by the purchaser.

The initial capacitance measurement shall be at low voltage. The change in capacitance as a result of the test voltage shall be less than either a value of 2% or that caused by failure of a single capacitor element of the particular design.

7.1.2.2 Terminal-to-case dielectric test

Testing will be performed in accordance with the requirements given in IEEE Std 18-1992.

7.1.2.3 Capacitance tests

Capacitance measurements shall be performed on each capacitor to demonstrate that its operating kilovar will be within ±5% of the rating capacitance of the capacitor when operated at the rated current and frequency, and with a case and internal temperature of 25 °C. Measurements made at other than 25 °C shall be adjusted, using a curve applicable to the type of capacitor being tested.

7.1.2.4 Leak test

A suitable test shall be made on each capacitor unit to ensure that it is free from leaks.

7.1.2.5 Discharge resistor test

Testing shall be performed in accordance with the requirements given in IEEE Std 18-1992.

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7.1.2.6 Loss determination test

Testing shall be performed in accordance with IEEE Std 18-1992 to confirm that the losses of each unit at the time of manufacture are within the manufacturer's limits.

7.1.2.7 Capacitance test on multi-unit rack assemblies

Capacitance measurements shall be made to ensure that its value is within ±2.5% of rating, and its measured value shall be stamped on the nameplate. This requirement is applicable to racks of parallel-connected externally fused or internally fused capacitor units.

7.2 Capacitor fuse

7.2.1 Design tests

7.2.1.1 Discharge test

Requirements for internal and external fuses—The capacitor fuse shall be tested to confirm that it will withstand the capacitor discharges associated with gap sparkover or bypass switch closure. The discharge shall have a peak current, I^2t, and frequency of greater than 110% of that required by the application. Five samples shall each be tested with 25 discharges. Tests shall be made before and after the discharges to verify that the fuses have not changed significantly.

7.2.1.2 Interruption test

a) *External fuse*—The external fuses shall be tested to demonstrate that they will interrupt the power-frequency current and the discharge current into a faulted capacitor from the parallel unfaulted capacitors and withstand the associated recovery voltage. The test shall reflect the magnitude and frequency of the current and the fuse recovery voltage of the actual installation. The test should be performed at higher than the prorated protective level to take into account the effect of previously blown fuses up to the maximum capacitor unbalance protection thresholds for which the bypass is initiated.

b) *Internal fuse*—The internal fuses shall be tested to demonstrate that they will interrupt the power-frequency current and the discharge current into a faulted element from the parallel unfaulted elements and withstand the associated recovery voltage. The test shall reflect the magnitude and frequency of the current and the fuse recovery voltage of the actual installation. The test shall be performed at higher than the prorated protective level to take into account the effect of previously blown fuses up to the maximum capacitor unbalance protection thresholds for which the bypass is initiated.

7.2.2 Production tests

a) *External fuses*—As a minimum, the external fuse shall be inspected and the fuse resistance shall be measured, and be within manufacturer's specified tolerance.

b) *Internal fuses*—The internal connections of the fuses are checked by discharging the capacitor from a voltage not less than 120% of the peak of the rated voltage. The capacitance shall be measured before and after the discharge test. The difference between these two measurements shall be less than the corresponding loss of one internal fuse operation.

7.3 Varistor

Some of the following tests are the same as or similar to those described in IEEE Std C62.11-1999.

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The testing procedures described in the following subclauses do not cover special applications such as under oil varistor units. In cases of abnormal service conditions, the test procedures and levels are subject to agreement between the manufacturer and the purchaser.

For the purpose of the following tests, the maximum continuous operating voltage (MCOV) of the varistor is the rated voltage of the segment (V_R).

7.3.1 Design tests

7.3.1.1 Accelerated aging procedure

Tests shall be performed in accordance with IEEE Std C62.11-1999 to determine the voltage ratios K_C and K_R used in the thermal recovery test of 7.3.1.3.2. These ratios are used to simulate the effects of in-service aging on the performance of the valve elements. K_C and K_R correspond to the MCOV and the 30 min emergency overload voltage, respectively.

7.3.1.2 Discharge voltage test

This test shall be performed to confirm that when the complete varistor is operating under specified line fault conditions, it will limit the voltage to the required protective level. The discharge voltage to define the protective level shall be measured for a discharge current having a virtual front time of 30 μs to 50 μs or less. The purpose of this test is to establish the relationship between the discharge voltage for the protective level current waveform and the discharge voltage that results for the current waveform used in the production test. If the current magnitudes are the same and the virtual front time of the production test waveform is less than 30 μs to 50 μs, the production test is sufficient, and this design test is not required.

7.3.1.3 Energy absorption and thermal recovery tests

Tests shall be performed to demonstrate that the varistor can withstand the energy associated with specified fault and operating conditions, and still show thermal recovery.

7.3.1.3.1 Energy absorption test

The energy absorption test shall be performed on a minimum of three test samples, each with an MCOV of at least 3 kV but not greater than 12 kV in open air at 20 °C ± 5 °C

The test energy shall correspond to the most severe of the line fault conditions specified (decisive case). This energy is then scaled down (prorated) with respect to rating and number of parallel columns and series valve elements of the actual test samples compared to the complete varistor.

Since the energy capability of a varistor depends somewhat on the current density (amplitude or equivalent pulse duration), the test has to demonstrate the worst-case conditions. The test shall be made 20 times with the application of power-frequency voltage with the same duration as or shorter than the decisive case. For shorter durations, the power-frequency voltage can be replaced by a single impulse (rectangular or sinusoidal wave) of the maximum current amplitude. The test energy shall be increased to account for the given current-sharing tolerances. This is done by multiplying test energy by the maximum specified current-sharing ratio divided by the actual current-sharing ratio of each test sample. If the tests are performed on single-column test samples, the actual current-sharing ratio is always one. Full cooling to ambient temperature between each energy application is permitted.

Discharge voltage and reference voltage measurements prior to and after the test shall be made. The discharge voltage shall be made at a current magnitude corresponding to the maximum fault current for the varistor. The discharge voltage and reference voltage shall not change by more than 3%. The valve elements shall not exhibit any significant physical damage, such as cracks or punctures.

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7.3.1.3.2 Thermal recovery test

A test shall be performed on three thermally prorated sections to demonstrate that the varistor can absorb the total energy from the duty cycle specified by the purchaser, as discussed in 5.4, and withstand the associated subsequent operating conditions. The operating condition following fault energy absorption is assumed to be rated current unless otherwise specified by the purchaser. Prior to testing, the prorated sections shall be preheated to a temperature in excess of the specified maximum ambient, heating due to solar radiation, and prior operation, based on a duty cycle defined in 5.4, at rated segment voltage unless a different temperature is defined by the purchaser. The thermal suitability of the prorated section shall be demonstrated using a technique equivalent to that described in IEC 60099-4:2004.

Within 5 min after removing the heat source, the prorated energy discharge should be applied. Within 1 min after the discharge, the equivalent of rated segment voltage shall be applied. The first 30 min may be at the 30 min overload voltage if that duty cycle is specified by the purchaser. This part of the test will be performed in still air with the air at room temperature or the maximum ambient temperature, if the latter is specified by the purchaser. The magnitude of the test voltages for the 30 min overload voltage and the continuous operating voltage should be increased by the voltage ratios K_R and K_C, which were determined in 7.3.1.1. More specifically, the 30 min overload test voltage should be equal to K_R times the voltage due to the 30 min emergency overload current. The continuous voltage should be K_C times the voltage associated with rated continuous current.

The rated segment voltage shall be applied for 30 min to verify thermal stability. During this time, the valve element temperature, the resistive component of current, and/or power dissipation shall be monitored until the measured value is appreciably reduced (success) or a thermal runaway condition is evident (failure).

Discharge voltage and reference voltage measurements prior to and after the test shall be made. The discharge voltage shall be made at a current magnitude corresponding to the maximum fault current for the varistor. The discharge voltage and reference voltage shall not change by more than 3%. The valve elements shall not exhibit any significant physical damage, such as cracks or punctures.

7.3.1.4 Pressure relief tests

The test procedure shall be generally consistent with that described in IEEE Std C62.11-1999 for station class arresters. For varistor units designed with a pressure relief device, the test sample shall incorporate prefailed elements or a short-circuiting internal fuse wire bypassing the elements. If prefailed elements are used, the failure must be within the body of the element. For a varistor unit designed without a pressure relief device, the test sample shall incorporate prefailed elements or elements with a fuse wire through a drilled hole. A successful test requires the confinement of all of the components of the test unit within the boundary defined in IEEE Std C62.11-1999. Only small non-injurious fragments may be expelled beyond the boundary. The high-current and low-current tests shall be performed on at least two completely assembled varistor units for each test. The varistor unit enclosures tested must be equal in length or longer than that required for the specific application.

The high-current test must include a capacitor discharge current, as is typically the case for a varistor failure. This test will be performed with a power-frequency current that is equal to or greater than that for the specific application. At the start of this current, a capacitor bank shall be discharged into the unit. The stored energy and peak discharge current of the test capacitor shall not be less than that of the specific application. Because of the presence of the capacitor discharge, the power-frequency current injection does not have to be timed to create significant asymmetry. The laboratory facilities required to perform this test are very extensive.

The low-current test (600 A rms) shall also be performed. The capacitor discharge current is not required for this test.

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7.3.2 Production (routine) tests

7.3.2.1 Energy absorption

All varistor elements shall be subjected to an energy withstand test at a prorated energy level equal to or greater than that required by the specified duty cycle. The test level must take into account factors such as current sharing between columns.

7.3.2.2 Current sharing

Current-sharing measurements shall be performed on all parallel-connected valve element columns of the varistor for each segment, to verify that the maximum current-sharing tolerances between columns are within the limit established for the design. Measurements shall be made such that the average test current per column is of a magnitude equal to the average current per column, which would occur in the entire varistor during system fault conditions, imparting maximum energy into the varistor. The testing can be made in either of two ways:

a) All parallel columns are tested with measurements taken of the current through each column.

b) The discharge voltage at the average test current per column shall be measured for all columns. After this discharge voltage measurement, the columns showing the highest and lowest discharge voltage shall be tested simultaneously with measurements of the current recorded. If the voltage measurement method is adopted, the relative measuring accuracy must be within ±0.3%.

7.3.2.3 Protective level

Measurements shall be made in order to confirm that the varistor meets its guaranteed protective level at a discharge current magnitude corresponding to the coordinating current of the complete varistor. The measurements can be made either on single valve elements and added up, or on complete varistor units.

7.3.2.4 Verification of low-current characteristics

Measurement of watts loss or reference voltage of each varistor unit shall be made to verify the continuous and emergency overload capability of the varistor. The reference voltage is the lowest peak value independent of polarity of power-frequency voltage, divided by the square root of two, and measured at the reference current. The reference current is the peak value of the resistive component of a power-frequency current used to determine the reference voltage of the varistor unit. The reference current shall be high enough to make the effects of stray capacitance negligible and shall be specified by the manufacturer. Typically, this is in the range of 0.05 mA to 1.0 mA per square centimeter of disk area.

7.3.2.5 Ionization voltage test

Measurement of RIV or internal corona (picocoulomb) of each varistor unit shall be made at a voltage corresponding to the 30 min emergency overload condition.

7.3.2.6 Seal integrity test

A test shall be made of the atmospheric sealing system of each varistor unit in accordance with IEEE Std C62.11-1999.

7.4 Discharge current limiting reactor

7.4.1 Design tests

The tests shall be in accordance with the applicable subclauses of IEEE Std C57.16-1996, Annex C.

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In some cases, laboratory limitations may prevent the tests described in 7.4.1.1, 7.4.1.2, and 7.4.1.3 from being performed at full current.

In lieu of performing a design test, reactors for a specific application can be validated via calculations that show the stresses do not exceed those that were successfully withstood in similar tests performed in the laboratory or in the field on other reactors using the same design techniques.

7.4.1.1 Discharge test

A discharge current test shall be performed to demonstrate that the discharge current limiting reactor will withstand the capacitor discharge currents and the fundamental fault currents the reactor will be exposed to during bypass of the capacitor.

The reactor shall be subjected to a test current not less than 1.1 times the total transient bypass current (capacitor discharge current plus system fault current).

The discharge current test may be carried out with a test current comprising a half-cycle current wave of power frequency and with the same amplitude.

If the reactor is used with overvoltage protective system based on a self-triggered gap, the test should be performed 25 times without evidence of mechanical or electrical damage. If the overvoltage protective system is based on a varistor, then the test should be performed 10 times.

NOTE—The 1.1 factor is applied to the total transient current to provide and demonstrate margin for service duty.

7.4.1.2 Fault current test

A fault current test shall be performed to demonstrate that the discharge current limiting reactor will withstand the rated power-frequency fault current (including peak asymmetrical) for its rated duration without evidence of excessive temperature or mechanical or electrical damage. The duration of the test should be according to the duty cycle defined by the purchaser, as outlined in 5.4.

Testing shall be performed in accordance with IEEE Std C57.16-1996, C.5.5.3.

7.4.1.3 Modified short-circuit test

As an alternate to the preceding tests, a modified short-circuit test may be performed. This test will include both the requirements in the discharge current test and the fault current test. The modified short-circuit test shall be performed in accordance with IEEE Std C57.16-1996, C.5.5.4. One multiple-cycle test is performed.

Some laboratory limitations also exist for this test.

7.4.1.4 Temperature rise

A temperature rise test shall be performed to demonstrate that the reactor will withstand the rated power-frequency current without excessive temperature rise above the specified ambient temperature. The temperature rise should not exceed the manufacturer’s established limit for the materials used.

Testing shall be performed in accordance with IEEE Std C57.16-1996, C.5.5.5.

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7.4.1.5 Mechanical resonance (optional)

A mechanical resonance test shall be performed if specifically requested by the purchaser. The test verifies that mechanical resonant frequencies of the reactor are at least 10% more or less than a value equal to twice the discharge current frequency.

One method that may be used to determine the mechanical resonance frequencies of the reactor involves the application of an acoustical impulse to the reactor. The impulse can be produced by the detonation of a small explosive device (firecracker) at the center of the core of the reactor. Accelerometers are placed at selected locations on the outside circumference of the reactor to sense the resulting vibrations of the reactor. These vibrations are analyzed to determine the mechanical frequencies of the reactor.

7.4.2 Production tests

The tests shall be in accordance with the applicable subclauses of IEEE Std C57.16-1996, Annex C.

7.4.2.1 Measurement of winding dc resistance

Testing shall be performed in accordance with IEEE Std C57.16-1996, C.5.4.1.

7.4.2.2 Measurement of inductance

Testing shall be performed in accordance with IEEE Std C57.16-1996, C.5.4.2.

7.4.2.3 Measurement of losses and Q-factor

Testing shall be performed in accordance with IEEE Std C57.16-1996, C.5.4.3.

The resistance shall be measured at the discharge frequency to confirm that the damping provided by the reactor is consistent with the overall design of the series capacitor bank.

7.4.2.4 Lightning impulse test or turn-to-turn overvoltage test depending on reactor voltage class

Testing shall be performed in accordance with IEEE Std C57.16-1996, C.5.4.4

7.5 Bypass gap

7.5.1 Voltage-triggered gap

7.5.1.1 Design tests

The following design tests shall be carried out. If the discharge and power-frequency fault currents do not affect the trigger circuit, it can be omitted in the tests.

The requirements of a specific application as related to the tests described in 7.5.1.1.1 and 7.5.1.1.2 can be evaluated by comparing the ampere-seconds for the application to the ampere-seconds of a previous design test.

7.5.1.1.1 Discharge current test

The power gap shall be subjected to a test current not less than 1.1 times the maximum total transient bypass branch discharge current. The transient bypass branch current shall be the combined system fault and

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capacitor discharge current that is calculated at maximum gap setting and specified power-frequency fault current including offset.

The discharge test may be carried out with a test current comprising a one half-cycle current wave of power frequency and with the same amplitude.

The test shall be repeated 25 times without mechanical damage, excessive erosion, or greater than 10% change in sparkover voltage of the power gap corrected to standard atmosphere conditions.

7.5.1.1.2 Fault current test

The power gap shall be tested 25 times to demonstrate that it will carry its specified power-frequency fault current for specified primary clearing time duration without evidence of excessive erosion or greater than 10% change in sparkover voltage of the power gap corrected to standard atmospheric conditions.

7.5.1.1.3 Recovery voltage test

A test shall be performed to demonstrate that the bypass gap recovers its voltage-withstand capability within the specified time after conducting the specified fault current for the specified duration. The sequence is to be consistent with the overall duty cycle specified by the purchaser, as outlined in 5.4.

For practical reasons, the test may be carried out on the power gap and the trigger circuit separately.

7.5.1.1.4 Sparkover test

The trigger circuit shall be subjected to a sparkover test to demonstrate that the trigger circuit sparks over correctly at the correct voltage level and recovers to the specified recovery voltage level within the specified time interval.

7.5.1.1.5 Overall bypass gap test

A design test shall be carried out to verify that the bypass gap comprising the power gap and the trigger circuit operates correctly during normal, emergency, and fault conditions. Considerations shall be taken for possible variation in sparkover voltage of the power gaps due to environmental factors and possible electrode erosion, as determined in 7.5.1.1.1 and 7.5.1.1.2. Oscillographic recordings shall be made.

7.5.1.1.6 Ambient environmental test

The trigger circuit shall be subjected to an ambient environmental test to demonstrate that it operates correctly within the specified tolerances, for specified variations in the environmental factors, such as temperature and air pressure. If the triggering function is independent of environmental factors, this test does not apply.

7.5.1.2 Production tests

The following production tests shall be made:

a) Verification that the components used are of the proper ratings

b) Adjustment and checking of power and trigger gaps for proper sparkover setting

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7.5.2 Forced-triggered gap

7.5.2.1 Design tests

The following design tests shall be carried out. If the discharge and power-frequency fault currents do not affect the trigger circuit, it can be omitted in tests described in 7.5.2.1.1, 7.5.2.1.2, and 7.5.2.1.3.

The requirements of a specific application as related to the tests described in 7.5.2.1.1 and 7.5.2.1.2 can be evaluated by comparing the ampere-seconds for the application to the ampere-seconds of a previous design test.

7.5.2.1.1 Discharge current test

The power gap shall be subjected to a test current not less than 1.1 the maximum total transient bypass branch discharge current. The transient bypass branch current shall be calculated at maximum protective varistor level and at specified power-frequency fault current. The power-frequency fault current will typically not include offset because of the effect of the varistor. The discharge test may be carried out with a test current comprising of one half-cycle current wave of power frequency and with the same amplitude.

The test shall be repeated 10 times without mechanical damage, excessive erosion, or greater than 10% change in sparkover voltage of the power gap corrected to standard atmospheric conditions.

7.5.2.1.2 Fault current test

The power gap shall be tested 10 times to demonstrate that it will carry its specified power-frequency fault current for its specified primary clearing time duration without evidence of excessive erosion and greater than 10% change in sparkover of the power gap corrected to standard atmospheric conditions.

7.5.2.1.3 Recovery voltage test

A test shall be performed to demonstrate that the bypass gap recovers sufficient voltage-withstand capability within the specified time after conducting the specified fault current for the specified duration. The recovery period is typically the dead time of line reclosing.

The sequence is to be consistent with the overall duty cycle specified by the purchaser, as outlined in 5.4. For practical reasons, by agreement the test may be carried out on the power gap and the trigger circuit separately. The test shall be carried out once.

7.5.2.1.4 Overall bypass gap controlled triggering test

The bypass gap comprising the power gap and the trigger circuit shall be subjected to a design test to verify that the bypass gap operates correctly during normal, emergency, and fault conditions. The gap shall only spark over when ordered to do so. Consideration shall be taken to possible variation in sparkover voltage of the power gaps due to environmental factors and possible erosion, as determined in 7.5.2.1.1 and 7.5.2.1.2.

The time delay associated with triggering of the bypass gap shall be established. This delay is from the time the varistor energy protection reaches its threshold to the time the power gap starts conduction. This time delay must be consistent with the design of the varistor for internal line faults. Oscillographic recordings shall be made.

7.5.2.2 Production tests

The following production tests shall be made:

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a) Verification that the components are of the proper ratings

b) Adjustment and testing of the trigger circuit

7.6 Platform-to-ground dielectric tests

Dielectric design tests shall be performed or reports shall be available to demonstrate that the platform support insulators and the platform-to-ground communication insulator meet the phase-to-ground insulation levels specified by the purchaser. These tests shall be performed in general accordance with IEEE Std C57.19.00-1991 and IEEE Std 4-1995.

When specified by the purchaser, dielectric tests shall be performed on a complete platform and insulator system or a dielectrically representative portion of a platform. These tests can include impulse, switching surge, and power-frequency withstand tests. Tests can also be performed for RIV and visible corona when reviewed in complete darkness with 120% rated power-frequency line-to-ground voltage applied. Previous design tests may satisfy this requirement.

7.7 Bypass switch

7.7.1 Design tests

If the design and construction of the bypass switch is essentially the same as that of a transmission line power circuit breaker, then the design tests described in 7.7.1.1, 7.7.1.2, 7.7.1.3, 7.7.1.4, and 7.7.1.5 can be supplanted with similar tests from IEEE Std C37.09-1999 or IEC/PAS 62271-109:2002.

7.7.1.1 Discharge test

A test shall be made to demonstrate that with the bypass switch open and the segment carrying maximum rated emergency current, the bypass switch will close and will satisfactorily withstand the combination of the maximum capacitor discharge and the power-frequency current. If used with a protective scheme where the bypass switch closes for system faults, then maximum-related fault current should be applied to demonstrate its close and latch capability.

An alternate discharge test may be substituted for bank designs where it is not reasonable, due to laboratory limitations, to complete the preceding test. The concern is to verify that the switch can successfully close and latch on the combination of the power-frequency fault current and the capacitor discharge current. The switch can be tested using a capacitor discharge, where the switch is exposed to a discharge current with a magnitude equal to the combination of the peak discharge current and the peak power-frequency current. This test recognizes that bypass switches are sensitive to the frequency of the discharge current. Therefore, a power-frequency bypass test is not as meaningful.

The peak current value and discharge frequency are to be established based on the requirements of the application. This frequency is typically in the range of 600 Hz to 1000 Hz.

7.7.1.2 Fault current test

A test shall be performed to demonstrate that with the bypass switch in the closed position, the switch is capable of withstanding its maximum momentary power-frequency current rating without requiring maintenance.

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7.7.1.3 Temperature rise test

With the bypass switch closed, apply rated continuous power-frequency current, measure temperature conditions for the length of time required to reach stable thermal conditions, and establish temperature rise above the specified ambient. This temperature rise shall not exceed the manufacturer's established limit.

7.7.1.4 Insertion test

A test shall be performed to demonstrate that with the bypass switch closed and maximum emergency current flowing through the bypass switch, the bypass switch will successfully interrupt the bypass current and divert the current through the capacitor and withstand the resulting recovery voltage.

This test requirement can also be satisfied using synthetic test procedures that produce the required current to be interrupted and a recovery voltage across the switch that is similar to that of the specific application.

7.7.1.5 Dielectric tests

Tests shall be performed to demonstrate that the voltage withstand across the interrupter and from phase-to-ground satisfy the requirements established in 5.7.

7.7.1.6 Closing time

For an overvoltage protective system utilizing a varistor but no bypass gap, the closing time of the bypass switch shall be determined by test. The timing test shall include operations at three or more ambient temperatures covering the specified temperature range. The maximum closing time established from these tests shall be consistent with the overall design for the varistor for internal line faults.

The magnitude of the control voltage used in the test shall be consistent with the application.

7.7.2 Production tests

The bypass switch shall be operated with its controls to determine that all mechanical, electrical, and pneumatic or hydraulic devices, if included, are functioning correctly. This test may be performed in the field. A dielectric test of 1500 V power frequency shall be applied to control circuit insulation.

If a circuit breaker is used as a bypass switch, it shall pass the requirements of applicable production tests found in IEEE Std C37.09-1999 or IEC 62271-100:2003.

7.8 Apparatus insulators (on the platform)

Tests shall be made in accordance with insulator standards referenced in 5.6.

7.9 Current transformers

Tests shall be made in accordance with the requirements of IEEE Std C57.13-1993.

7.10 Control transformers

Tests shall be made in accordance with IEEE Std C57.12.00-2000. When applied in parallel with capacitors, the transformer shall be tested to demonstrate the ability to withstand the discharge of the capacitors charged to the protective level.

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7.11 Protection and control

7.11.1 Design tests

The following tests shall be performed on the control and protection system in order to verify the design:

a) *Functional tests*—The objective is to verify the design of the protection and the proper functionality of the logic as implemented in hardware and software. Tests by current injection using appropriate waveforms to simulate the system conditions or tests are recommended. Correct output operation of each protection function is verified. The proper performance of the software logic also is verified. All settings, operating times, and proper performance are confirmed with these tests. The correct functioning of the platform-to-ground communication protocol shall be confirmed.

b) *Environmental tests*—The objective is to verify the functionality of the control and protection system over the specified temperature range. The accuracy and speed of response of critical functions should be established and confirmed to be consistent with overall design of the series capacitor bank. This testing is normally performed in an environmental chamber and with power applied.

c) *Electrical, surge, and electromagnetic interference tests*—The control and protection panels should be tested in accordance with the IEEE Std C37.90-1989, IEEE Std C37.90.1-2002, and IEEE Std C37.90.2-2004). These tests include electromagnetic interference, surge withstand capability, and electrostatic discharge tests.

7.11.2 Production tests

Tests shall be performed to verify the manufacturing quality of all components and of the complete assembly. Separate testing for platform and ground control equipment is acceptable. The procedure consists of injecting power-frequency steady-state signals that simulate conditions requiring protective action into each control input. Each output is monitored during these tests. All hardware and software settings are verified. Software settings may be verified by software techniques.

If optical platform-to-ground communication is used, the output power of the transmitters shall be checked.

An optical loss test shall be performed on each fiber of the platform-to-ground communication insulators.

8. Nameplates and instruction books

8.1 Nameplates

8.1.1 Nameplates for capacitors

The following minimum information shall be given on nameplates for each individual capacitor:

a) Name of manufacturer
b) Manufacturer’s type, model, style, or catalog number
c) Rated kilovar
d) Rated current or rated voltage
e) Rated frequency
f) Statement indicating whether or not the capacitor has a discharge device inside the case
g) Code number or serial number indicating approximate date of manufacture
h) Statement that indicates whether the insulating liquid is inflammable (if flammable, the volume of the liquid shall be shown)
i) Impregnate identification (Additional marking, decal, or stick-on label shall be visible from the ground. The color blue shall be used to designate non-PCB liquid.)

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8.1.2 Nameplates for capacitor racks

The following minimum information shall be given on nameplates for racks:

a) Name of manufacturer
b) Identification style or other number
c) Measured capacitance, μF
d) Serial number or the equivalent

8.1.3 Nameplates for bypass switch

Nameplates shall contain the following minimum information:

a) Name of manufacturer
b) Identification number
c) Rated continuous current
d) Rated frequency
e) Rated impulse withstand across the interrupter and from the bottom of the interrupter-to-ground
f) Rated closing time
g) Rated interrupting time
h) Rated close and latch current
i) Duty cycle

8.1.4 Nameplates for the varistor and varistor units

8.1.4.1 Nameplate for varistor units

The nameplate of each varistor unit(s) shall contain the following information:

a) Name of manufacturer
b) Manufacturer's type, model, style, and catalog number
c) MCOV
d) Rated leakage current at MCOV
e) Rated frequency
f) Year of manufacture
g) Weight
h) Energy

8.1.4.2 Nameplate for the varistor

The nameplate for each varistor shall contain the following:

a) Name of manufacturer
b) Manufacture's type, model, style, and catalog number
c) Varistor energy rating
d) Protective level and coordinating current
e) Number of housings required for the varistor energy rating

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8.1.5 Nameplates for discharge current limiting reactors

The nameplates for the reactors shall include the recommended nameplate information defined in IEEE Std C57.16-1996.

8.1.6 Nameplates for protection and control cabinets

The following minimum information shall be given on nameplates for protection and control cabinets:

a) Name of manufacturer

b) Identification number

c) Instruction book number

8.2 Instruction books

8.2.1 Instructions for series capacitor bank

The following minimum information shall be provided in the instruction book for the series capacitor bank:

a) Name of supplier

b) Overall bank

   1) Summary of ratings

   2) Layout drawings

c) Power equipment

   1) Description

   2) Ratings

   3) Outline drawings

   4) Maintenance procedures

   5) Spare parts

d) Protection and control

   1) Description of operation

   2) Schematics

   3) Maintenance procedures

   4) Testing procedures

   5) Spare parts

9. Color

The color for all of the insulators including the insulators and bushings of the equipment, the capacitor units, and the discharge current limiting reactor shall be as defined in ANSI Z55.1-1967, Designation No. 70 (light gray finishes for industrial apparatus and equipment), unless otherwise specified by the purchaser.

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10. Safety

10.1 General Requirements

The specification, design, installation, operation, and maintenance of the series capacitor installation shall meet, wherever applicable, the safety and environmental codes in effect in the geographical region in which the bank is installed. Where specific guidelines are not available, reference should be made to the applicable sections of the NESC. Adherence to this code by the electric utilities within its scope is mandatory, and its use is encouraged wherever the installation is governed by IEEE standards. Where installations are required to meet other than IEEE standards, this standard, IEEE Std 824-2004, may provide guidance with regard to safeguarding people from hazards arising from the installation, operation, or maintenance of electric supply and communication lines and equipment. Particular attention is drawn to subclauses dealing with safety grounding, clearances, and insulation coordination issues as it affects the series capacitor platform relative to earth, the fence enclosing the platform, and the BIL issues dealing with insulators supporting the series capacitor platform and the bypass switch. However, the NESC is not applicable in establishing electrical clearances on the platform, as there are no personnel on the platform when the equipment is energized.

10.2 Discharge devices

Each capacitor unit shall be provided with a means for discharging to 50 V or less in 5 min from a dc voltage of $\sqrt{2}$ times the rms rated unit voltage. (The discharge criteria may instead be consistent with IEC 60143-1:1992 [B1], if so specified by the purchaser.)

Where a control transformer is permanently connected across a capacitor segment, it may discharge the capacitor in a short time and shall meet the thermal and mechanical requirements involved. All equipment on the platform shall be interconnected via low impedance paths.

The bypass switch (see Figure 1, number 8) shall also provide a means to bypass the capacitors and maintain them in a discharged condition prior to removing the related capacitors from service.

Provisions shall also be made for disconnect switches (see Figure 1, numbers 10 and 11) to isolate and bypass the series capacitor bank. The grounding switches (see Figure 1, number 12) are also used with some installations to ground the capacitors.

All grounding attachment points or terminals shall be capable of carrying the fault current specified by the purchaser for the bypassed mode discussed in 5.3.2.

10.3 Personnel protection

The series capacitor bank shall be designed so that its operation can include precautionary measures to minimize the possibility of personnel coming into contact with energized parts. The series capacitor bank is normally enclosed by a safety fence. Access to the capacitor platforms for maintenance is obtained through a secured entrance gate that may optionally have an interlock system. The series capacitor bank is considered energized unless it is isolated, grounded, tested to be de-energized, and suitable tags have been applied. The following safety precautions should be taken:

a) Bypass and isolating disconnect switches for a series capacitor bank should be located externally to the series capacitor platform and outside the capacitor bank safety fence.

b) Grounding disconnect switches are often used for grounding the series capacitor bank terminals at one or both ends of the bank.

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c) Interlocking should be used to establish the proper sequence of closing or opening the switches associated with a series capacitor bank and, optionally, the opening and closing of the gate to the protective fence.

d) Before opening the capacitor bypass switch for maintenance and inspection, the terminals of the bank should be connected to ground using personal safety grounds. These shorting grounds should not be removed unless the capacitor bypass switches are closed.

e) For a capacitor unit not connected within a grounded bank, the capacitor terminals shall be shorted before touching. The terminals shall remain shorted until no further handling is necessary. This is to guard against the possibility of an accident should an open circuit to the internal discharge resistor have developed and a trapped charge built up on the capacitor unit.

10.4 Handling and disposal of capacitor units and fluid

Handling and disposal of capacitor units and insulating fluid should follow methods such as those prescribed by the U.S. Environmental Protection Agency or other governing agencies as applicable. Guidance may also be obtained from IEEE Std 980-1994.

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Annex A

(informative)

Additional related information

A.1 Capacitor short-time and transient overvoltage capability

The life of a capacitor may be shortened by overstressing, overheating, or physical damage. Therefore, the length of life depends upon the control of operating conditions involving voltage, temperature limits, and physical care.

Capacitors may be operated above rated voltage under emergency and infrequent conditions. The magnitude of the overvoltages that may be tolerated without loss of life is dependent upon the duration of each overvoltage, the number of applications, and the temperature of the capacitor. The capacitor short-time power-frequency capabilities given in IEEE Std 1036-1992 and previously given in IEEE Std 18-1992 are shown in Figure A.1 and Figure A.2. Table A.1 provides similar capabilities from IEC 60143-1:1992 [B1], Table 10.

These capabilities may be different from those of a specific application, depending on the requirements specified by the purchaser. A capacitor may be reasonably expected to withstand, during normal service life, a combined total of 300 applications of such power-frequency terminal-to-terminal overvoltages without superimposed transients of harmonic content.

Very high-current transients due to bypassing are limited by the application of overvoltage protective devices and discharge current limiting reactors.

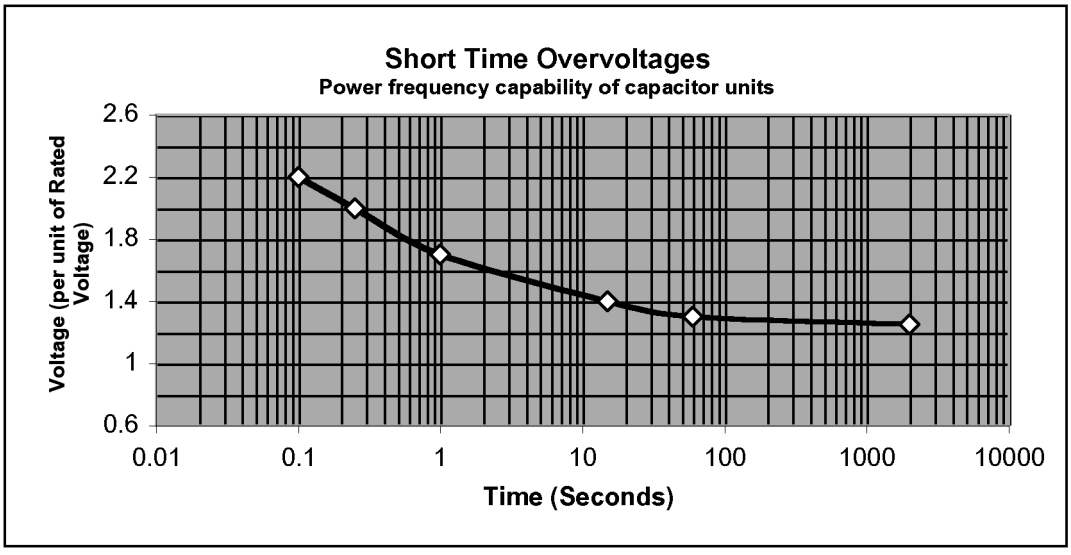

Figure A.1—IEEE Std 1036-1992 short-time power-frequency capability

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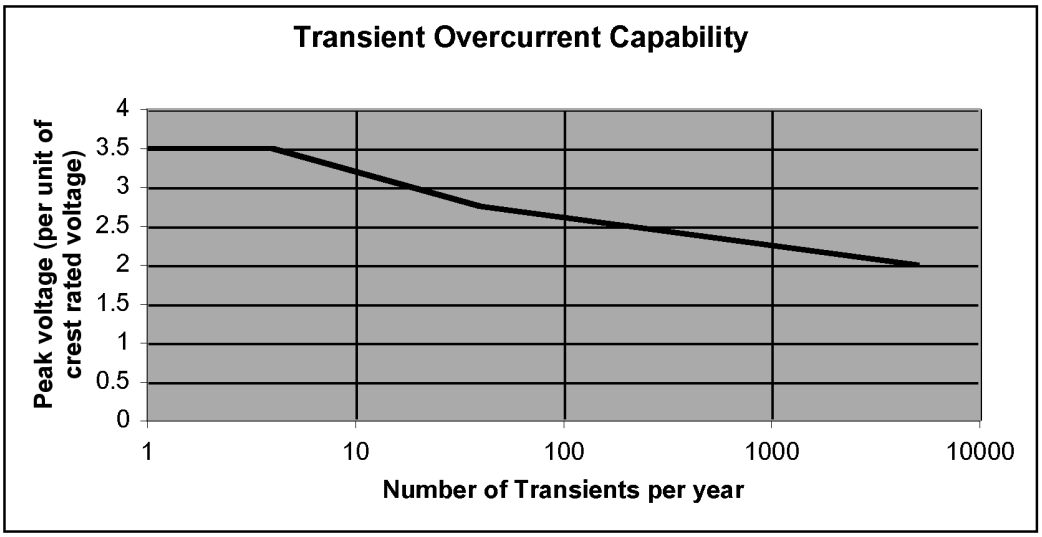

Figure A.2—IEEE Std 1036-1992 transient overcurrent capability

Table A.1—IEC 60143-1:1992 [B1], Table 10, typical bank overload and swing current capability

Current	Duration	Typical range per unit	Most common values per unit
Rated	Continuous	1.0	1.0
1.1 × rated	8 hr in 12 hr period	1.1	1.1
Emergency overload	30 min	1.2 to 1.6	1.35 to 1.5
Swing	1 s to 10 s	1.7 to 2.5	1.7 to 2.0

A.2 Economic evaluation of series capacitor bank losses

The purpose of this annex is to clarify certain aspects of the losses of a series capacitor bank. Although purchasers have not typically evaluated series capacitor bank losses since the dielectric losses of a modern all film design are quite low, such an evaluation may foster the development of more efficient designs. It must be noted that a significant percentage of the losses are associated with the discharge resistor that is provided to increase safety by discharging the unit following removal of the power-frequency voltage.

The losses of the bank vary with the square of the current. Therefore, it is important that the application of the bank be reviewed to select the current magnitude or magnitudes for the loss evaluation that best represent normal continuous operation of the bank. For example, for a transmission system with two parallel lines, the purchaser may chose to rate the series capacitor banks so that a bank can carry the current associated with full power with only one line in service. In this case, the normal bank current will be 50% of its rated value and the bank losses only 25% of those at rated bank current.

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The losses on the bank stem primarily from the losses of the capacitor and capacitor fuse losses. The capacitor losses consist of those of the internal discharge resistors, internal connections, and dielectric. The first two types of losses are fairly constant over the operating life of the capacitor. However, the dielectric losses decrease with time with ac voltage applied. Thus, the losses of the capacitor unit and the bank will decrease from the initial value measured in the factory during the routine test described in 7.1.2.6. The initial losses may vary among identical units manufactured at the same time. However, the variation among the units of the final *stabilized losses* are usually much less. Manufacturers have developed tests that predict long term operating losses for loss evaluation purposes. These techniques are not defined in this standard.

Most series capacitor banks do not have any additional significant components of losses other than capacitor units and fuses. Usually the discharge current limiting reactor is in series with the bypass switch, which is normally open. In this operating mode, the discharge current limiting reactor contributes no additional losses to the bank. However, in some installations this circuit is in series with the capacitors. For this case, or if the bank is normally bypassed, the losses of the discharge current limiting reactor must be considered.

The power losses associated with cabinet heaters and control power are small and are not normally considered in a loss evaluation.

It is not practical to measure the losses of a series capacitor bank after it is installed.

A.3 Discussion of capacitor overvoltage protection

A.3.1 General considerations

During normal service operation, series capacitors are subject to power system swing currents and fault currents that result in transient voltage stresses across the capacitors and to platform equipment. The magnitude and duration of voltage stresses are essential parameters in series capacitor bank design. If the voltage stress and duration are not controlled, an uneconomical bank design, based on these short-time stresses, could result.

Bypass gaps and varistors used alone or in combination are normally used in parallel with the series capacitor to control the magnitude and duration of capacitor overvoltages. The method of overvoltage protection selected should take into consideration a number of factors that include swing current and overload current ratings, operating practices, maintenance, reinsertion capability, fault magnitude, fault duty cycle, and economics.

The bypass gap protects the capacitor by collapsing the voltage across the capacitor and providing a path for current around the capacitor. Power gaps can be designed to operate on voltage magnitude across the gap or be induced to fire by a triggering circuit. Generally, the trigger circuit uses quantities, such as varistor energy, current magnitude, and rate of change of quantities, to determine gap operation. Power gaps need to be deionized after operation to restore dielectric strength to allow reinsertion of the capacitor bank.

The varistor is a voltage-dependent nonlinear resistor that protects by limiting (clamping) voltage across its terminals to a specified protective level by diverting excess fault current. The varistor does not require any deionization time after a protection or voltage limiting action; therefore, reinsertion of capacitors into the circuit is immediate.

The bypass gap and varistor both need to be protected from excess duty. For gaps, this is generally excessive conduction time measured in cycles. For varistors, the measure is typically energy.

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Generally, capacitor overvoltages and varistor energies resulting from fault currents through the bank are critical to the design of the protection equipment. The following is a list of parameters that should be considered when reviewing these stresses:

a) *Bank location*

b) *Fault location*—Internal vs. external

c) *Fault type*—Single-phase and multiphase

d) *Fault duration*—Fault scenarios, including automatic and manual reclosing times, and breaker normal and extended clearing times

e) *Fault currents*—Fault current magnitudes through the bank

f) *Post-fault conditions*—Swing current and half-hour overload

g) *Back-up fault clearing scenarios*

h) *Reinsertion voltages*—(Gap systems) under post-fault conditions

A.3.2 Bypass gaps

A bypass gap can be designed to operate with sustained or unsustained arcs. The sustained arc gap (non-self-extinguishing gap) requires bypassing or current interruption by other devices to extinguish the arc. The unsustained arc gap (self-extinguishing gap) has the ability to extinguish the arc itself, by magnetic or pneumatic action. The unsustained arc gap may cause greater stress on capacitors and other equipment.

Sparkover of a bypass gap is often initiated by a trigger circuit.

An untriggered bypass gap, that is, a bypass gap without a trigger circuit, is very seldom used for series capacitor protection application, due to its sensitivity to variations in ambient conditions as well as gap wear. This causes large variations in sparkover voltage, which can result in unreliable operation.

A triggered bypass gap can be designed to operate on voltage (self-triggered gap) or on command, based on other quantities, such as varistor energy, current magnitude, or rate of change of quantities (forced-triggered gap).

A forced-triggered gap may be used in combination with a varistor for varistor-protected series capacitors.

A.3.3 Voltage-triggered bypass gaps

The bypass gap is normally set to such a level that sparkover will occur for internal faults. The gap may or may not spark over for external faults, depending on power system requirements.

For an internal fault cleared by the primary line protection, the gap should, after arc extinction, recover dielectrically within the interval before line circuit-breaker auto-reclosing or shortly after line auto-reclosing when the bypass switch re-opens.

For an external fault, after sparkover followed by arc extinction resulting from closure of a bypass switch, the gap should recover dielectrically so that the capacitor can be reinserted by the opening of the bypass switch shortly after the external fault has been cleared. If fast capacitor reinsertion is required, two self-triggered gaps with different settings and an additional switch can be used to obtain this function (dual gap system). The same function may be achieved by forced arc extinguishing of the power gap.

Selection of the gap setting should consider the need for capacitor reinsertion during specified power system post-fault conditions.

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The gap must be able to withstand the specified fault current for the specified duration. In case of high-speed reclosing of line circuit breakers, the gap must be designed to withstand consecutive sparkover that may result as a consequence of unsuccessful high-speed reclosing, while maintaining the protective level to within the specified tolerance.

If the series capacitor comprises multiple segments, due regard shall be taken to the dc component in the reinsertion voltage, when the gap setting is determined.

When the bypass gap sparks over, the capacitor will discharge from the sparkover voltage level through a loop circuit that normally consists of the bypass gap, capacitor fuses, and current-limiting reactor. In the case where the bank bypass switch closes, the capacitor voltage prior to closing will be the product of the load current and capacitive reactance.

The reactor inductance is chosen to limit the current, considering each of the components in the loop circuit for both switch and bypass gap operations. The current-limiting damping equipment normally comprises a reactor with inherent damping and a parallel-connected resistor, if required.

A.3.4 Forced-triggered bypass gap

A forced-triggered gap may be used in combination with a varistor to limit the varistor energy under certain fault conditions. It should operate only on command.

For an internal fault, the gap may be permitted to spark over on command and bypass the varistor and the capacitor. The gap should recover dielectrically within the dead interval before the line circuit-breaker recloses.

For an external fault, the gap should normally not operate. The capacitor voltage is limited to a specified protection level by the varistor. Capacitor reinsertion is obtained automatically and without delay upon clearing of the fault by the line circuit breakers.

The design of the varistor/gap combination should be designed to work correctly during specified power system swing and emergency loading conditions.

As in the case of a voltage-triggered gap, the forced-triggered gap should withstand specified fault current for specified durations, repeated sparkovers during unsuccessful reclosings, and capacitor discharge current superimposed on the power-frequency fault current.

A.3.5 Protection with a varistor

A varistor limits the temporary overvoltage across the capacitors by conducting the excess transmission line current, usually due to faults, that would otherwise cause excessive capacitor voltage. This condition occurs on each half cycle during the overcurrent condition or until the parallel bypass switch closes or the bypass gap fires. The maximum voltage that results across the series capacitor is dependent upon the nonlinear voltage-current characteristics of the varistor and the magnitude of the overcurrent. Because the varistor voltage increases with current, the protective level is usually defined at a coordinating current representative of expected varistor current during a power system fault. Energy is absorbed by the varistor during conduction. The selection of the varistor energy capability and protection of the varistor against overstress are important aspects of the series capacitor protection system.

The selection of the protective level of the varistor should take into account the voltage associated with the various nonfault currents through the series capacitor for normal, emergency, and system swing conditions. The varistor shall be designed to be capable of withstanding these voltages following the absorption of fault energy and with the most unfavorable ambient temperature, if so specified by the purchaser.

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The voltage associated with the power system swing is often the highest nonfault voltage that the series capacitor and the varistor must withstand. As such, it can be the determining factor in establishing the protective level. A low varistor protective level may mean the varistor will exhibit significant conduction and energy absorption during the swing, necessitating a varistor with a greater energy rating. Increasing the protective level of the varistor can reduce varistor energy absorption. However, the capacitor design is subject to change because of the higher overvoltages.

The choice of protective level can also be influenced by its relationship to the varistor energy requirements for external faults. Typically, a lower protective level increases varistor energy absorption. Conversely, a higher protective level requires less energy absorption. These factors, plus the preference of the purchaser and other power system considerations, are included in the choice of protective level. One power system consideration is subsynchronous resonance. The voltage magnitude of large subsynchronous oscillations is limited by the varistor. In applications where subsynchronous oscillations are a concern, there is a preference for a lower protective level. A second power system consideration is the effect that series capacitors have on the capability of the transmission line breaker to dielectrically recover against the transient recovery voltage (TRV) present during opening. Series capacitors can increase this recovery voltage. The voltage is reduced by lower protective levels. Both of these phenomena are affected by the varistor voltage at currents lower than those associated with an external fault.

The varistor is designed with power current and energy absorption capabilities that shall be consistent with anticipated power system fault conditions. In addition to the protective level, critical factors determining varistor requirements are the equivalent impedance of the power system, the duration of the fault, and transmission line circuit-breaker reclosure sequence. With this information, the varistor current and energy absorption can be determined.

Computer simulations are needed to adequately determine varistor duty. Typically, the varistor will be designed to withstand the current and energy associated with specified external line section faults so that the series capacitor in the unfaulted line remains in service during the fault and the critical post-fault period to enhance power system stability.

Internal line section faults near the series capacitor bank can cause much higher varistor current and energy. This is especially true if the installation is located at the end of the line near a substation with a high short-circuit current. In this case, the series capacitor protection system typically incorporates a parallel gap to bypass the series capacitor at high speed for a close-in fault. The bypass gap greatly reduces the energy requirements for the varistor. However, the varistor shall withstand the high fault current until bypass occurs.

In such applications, the speed of the bypass is an important factor in the varistor design. If the installation is located out on the transmission line, the varistor duty for a fault near a bank is substantially less than the end of the line application (but far more than for the external fault). This makes the speed of the bypass less important. It becomes more practical to omit a parallel bypass gap and to limit the duration of varistor conduction for a fault by closing the bypass switch.

A.3.6 Protection using a thyristor valve

Instead of a conventional bypass gap or varistor protection scheme, the overvoltage protective function can be provided by a thyristor valve assembly, as shown in Figure A.3. The thyristor valve commutates fault current around the capacitors during internal line faults. At normal operating voltages across the capacitors, the thyristor valve is blocked and line current flows through the capacitor. The fault protection strategy is to monitor ac-line current through a current transformer located on the platform. When the ac-line current exceeds a threshold value, a fault condition is assumed and protective valve firing sequence initiated. In addition to the ground-based firing signal, the thyristors may be equipped with an independent overvoltage protection that is designed to operate at or slightly above the bank protective level. The thyristor valve

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continues to conduct line fault current on each half cycle until the parallel bypass switch closes or the current returns to a nominal value; a typical internal fault would involve 2 to 3 cycles of fault current conduction. During valve conduction, the ac-line current is monitored to detect when the fault has cleared. If the fault current is lower than a specified threshold value for a longer time period, the event is interpreted to be an external fault and the valve may be fired to accommodate the specified swing current with the bypass breaker remaining open during the event.

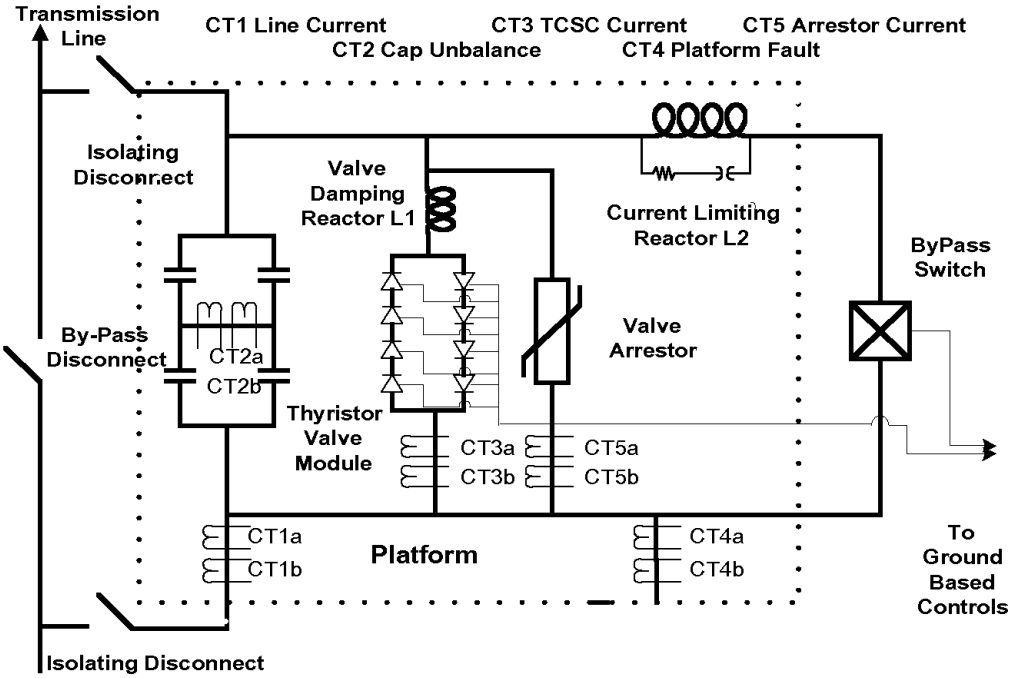

Figure A.3—Typical thyristor protected series capacitor bank

During the initial energization of the capacitor bank, the thyristor valve is blocked and a minimal MOV is provided to limit overvoltage during inrush. The line current is checked prior to opening the bypass breaker to prevent initial energization of the bank into a line fault. The recommended procedure involves first closing the line breakers before inserting the series capacitors. The TPSC control and protection system can prohibit opening the bypass breaker when the line breaker is open.

A current-limiting reactor is placed in series with the thyristor valve to dampen discharge current when the bypass breaker opens.

A.4 Field tests

After installation of the series capacitor bank is complete, tests may be performed on the completed bank to verify proper operation of all equipment. These fall into three categories of tests: pre-energization, commissioning, and staged fault. The pre-energization tests may be carried out by the purchaser or the supplier in accordance with the procedures defined by the supplier. Commissioning tests and staged fault tests are performed by the purchaser using procedures that have the concurrence of the supplier.

a) *Pre-energization tests*—These tests are performed before the bank is energized for the first time. The procedures include, but are not be limited to, visual inspection of all equipment and checking power circuit connections. This includes tests such as current transformer ratios, breaker timing, control circuit wiring, protection calibration and settings, and bypass gap functioning. Tests designed to verify the functioning of the overall system are also performed.

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b) *Commissioning tests*—It is recommended that operational tests be performed after successful completion of the pre-energization tests. These tests are performed under actual operating conditions, exposing the bank to actual line-to-ground voltage and line current with increasing test durations. It is recommended that the bank first be energized from one terminal for a short period of time to test the line-to-ground insulation. During initial energization of the bank, protection alarms and equipment performance should be closely monitored. Subsequent tests also may be performed at overload current levels. Operational tests typically include opening and closing operations of the bypass switch, and going through the isolation and energizing procedures of the bank. Operation of other breakers and disconnect switches not associated with the bank in the substation may be done to verify that the bank operation is not affected by stray electromagnetic influence.

c) *Staged fault tests*—After the series capacitor banks are operational, staged fault tests are sometimes performed. These tests should be carefully discussed with the supplier. Incorrectly performed, these tests could result in damage to the equipment. All important quantities should be monitored and the results analyzed.

   Staged fault tests of series capacitor installations can have a number of possible objectives, as follows:

   1) To verify that, under fault conditions, all the major platform components within the current-carrying path can withstand a duty approaching their specified capability, such as the varistor, capacitors, bypass gap, damping reactor, and bypass breaker
   2) To establish that the insulation levels of the platform components have been properly coordinated
   3) To verify the proper operation of the protection and control system, including the bypass gap and associated circuitry where required
   4) To confirm the proper operation of the relays, both for the compensated line and for the adjacent lines, under various system conditions
   5) To evaluate secondary arc extinction times where single pole tripping is utilized
   6) To use the resulting measurements to improve computer modeling of the series capacitor bank and the power system

A.5 Inspection and maintenance

On established schedules, regular inspection of the capacitor installation should include a check for blown capacitor fuses, capacitor case leaks, bulged cases, spacing of protective gaps, operation and settings of protective and control devices, and other maintenance operations as suggested in the manufacturer's instructions. Insulators and capacitor bushings should be cleaned periodically, the interval depending upon the severity of the conditions to which they are exposed. Equipment components exposed to weathering should be repainted periodically to limit corrosion.

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Annex B

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Summary of specification items

The following is a summary of the items that should be specified by the purchaser. All of these items are discussed in the main body of this standard. If the bank is to have provisions for increased ratings in the future, the purchaser's specification must also include definition of items f), g), h), j1), j3), j4), and k1) for the future conditions, as well as the degree to which these requirements are to be met in the initial design and equipment of the bank.

a) Service conditions
b) Ambient temperature requirements for outdoor and indoor equipment
c) Power system frequency
d) Maximum power system operating voltage
e) Phase-to-ground insulation requirements per IEEE or IEC standards
    1) BIL
    2) Power frequency or switching surge withstand
    3) Leakage distance
f) Rated reactance of each segment or subsegment
g) Current ratings for the bank inserted mode
    1) Continuous current
    2) Emergency overload currents and durations
    3) Swing current and duration
h) Current ratings for the bank bypassed mode
    1) Continuous current
    2) Emergency overload currents and durations
    3) Swing current and duration
    4) Fault currents and duration
i) Capacitor units
    1) Type of fusing
    2) Terminal-to-terminal dielectric production test if performed at a higher voltage than identified 7.1.2
j) Overvoltage protection
    1) One-line diagram of the surrounding power system with reactances of the lines and equivalent sources
    2) Type of overvoltage protective device
    3) Fault sequences for internal and external faults
    4) Results of purchaser's computer simulations showing varistor duty
    5) Protective level of the overvoltage protective device

    It is recommended that the purchaser not specify the magnitude of the protective level unless the purchaser has related power system application objectives, such as limitation of sub-synchronous resonance (SSR) or line circuit-breaker TRV. In this case, the purchaser should add the required protective margin. This allows the supplier to select the protective level to better optimize the equipment.

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k) Protection and control
   1) Extent of local and remote indications
   2) Degree of redundancy
   3) Available supply voltages
l) Safety—The purchaser should specify any unique requirements for grounding or interlocking.
m) Tests—Additional testing not included in Clause 7 or A.4.

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Annex C

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[10]IEC publications are available from the Sales Department of the International Electrotechnical Commission, Case Postale 131, 3, rue de Varembé, CH-1211, Genève 20, Switzerland/Suisse (http://www.iec.ch/). IEC publications are also available in the United States from the Sales Department, American National Standards Institute, 25 West 43rd Street, 4th Floor, New York, NY 10036, USA (http://www.ansi.org/).

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