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IEEE Standards

1547.1™

IEEE Standard Conformance Test Procedures for Equipment Interconnecting Distributed Resources with Electric Power Systems

IEEE Standards Coordinating Committee 21

Sponsored by the
IEEE Standards Coordinating Committee 21 on
Fuel Cells, Photovoltaics, Dispersed Generation, and Energy Storage

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IEEE Standard Conformance Test Procedures for Equipment Interconnecting Distributed Resources with Electric Power Systems

Sponsor

IEEE Standards Coordinating Committee 21 on Fuel Cells, Photovoltaics, Dispersed Generation, and Energy Storage

Approved 9 June 2005

IEEE-SA Standards Board

Abstract: This standard specifies the type, production, and commissioning tests that shall be performed to demonstrate that the interconnection functions and equipment of the distributed resources (DR) conform to IEEE Std 1547™.
Keywords: distributed resources, interconnection, test procedures

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Introduction

This introduction is not part of IEEE Std 1547.1-2005, IEEE Standard Conformance Test Procedures for Equipment Interconnecting Distributed Resources with Electric Power Systems.

IEEE Std 1547.1 is one of a series of standards developed by Standards Coordinating Committee 21 (SCC21) concerning distributed resources (DR) interconnection. The titles of the additional documents in that series follow:

— IEEE Std 1547, IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems[a]

— IEEE P1547.2™, Draft Application Guide for IEEE Std 1547, Interconnecting Distributed Resources with Electric Power Systems [B6][b]

— IEEE P1547.3™, Draft Guide for Monitoring, Information Exchange, and Control of Distributed Resources Interconnected with Electric Power Systems [B7]

— IEEE P1547.4™, Draft Guide for Design, Operation, and Integration of Distributed Resource Island Systems with Electric Power Systems [B8]

— IEEE P1547.5™, Draft Technical Guidelines for Interconnection of Electric Power Sources Greater Than 10 MVA to the Power Transmission Grid [B9]

— IEEE P1547.6™, Draft Recommended Practice for Interconnecting Distributed Resources with Electric Power Systems Distribution Secondary Networks [B10]

The root standard, IEEE Std 1547, defines a set of uniform requirements for the interconnection of DR to the distribution segment of the electric power system (EPS). IEEE Std 1547 is an outgrowth of the changes in the environment for production and delivery of electricity and builds on prior IEEE recommended practices and guidelines developed by SCC21.

IEEE Std 1547 includes requirements relevant to the operation of the interconnection. It generally defines limitations and set points for various parameters that must be satisfied prior to the connection of a DR unit to the EPS, at the instant of connection, and for the separation of such resources from the EPS for abnormal conditions.

IEEE Std 1547.1 provides conformance test procedures to establish and verify compliance with the requirements of IEEE Std 1547. When applied, the IEEE 1547.1 test procedures can provide a means for manufacturers, utilities, or independent testing agencies to confirm the suitability of any given interconnection system (ICS) or component intended for use in the interconnection of DR with the EPS. Such certification can lead to the ready acceptance of confirmed equipment as suitable for use in the intended service by the parties concerned. While this standard defines test procedures, it does not specify measurement techniques. Suitable measurement techniques can be found in various technical publications including, but not limited to, IEEE Std 120™ [B13].

It is beyond the scope of IEEE 1547.1 to specify the design and performance criteria for ICSs or components. It is left to the parties concerned to determine that the equipment manufacturer's specifications and confirmed performance satisfy the technical needs of the EPS distribution circuit to which the DR unit is to be connected. Similarly, this standard does not address the local electrical power system technical needs nor load requirements for the facility or premises where the point of DR connection is made.

[a]Information on references can be found in Clause 2.

[b]The numbers in brackets correspond to the numbers of the bibliography in Annex B.

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IEEE Standard Conformance Test Procedures for Equipment Interconnecting Distributed Resources with Electric Power Systems

1. Overview

This standard provides tests and procedures for verifying conformance of interconnection systems (ICSs) to IEEE Std 1547™.[1] It is recognized that an ICS can be a single device providing all required functions or an assembly of components, each having limited functions. Components having limited functions shall be tested for those functions in accordance with this standard. Conformance may be established through combination of type (referred to as "design" tests in IEEE Std 1547), production, and commissioning tests. Additionally, conformance to IEEE Std 1547 requires interconnection installation evaluation and periodic tests.

This standard also includes Annex A, which describes test signals and ramp functions used in conducting some tests. Additionally, a bibliography is included as Annex B; it lists documents that are referred to in this standard for informative purposes, but that are not required to implement the procedures defined in this standard.

1.1 Scope

This standard specifies the type, production, and commissioning tests that shall be performed to demonstrate that the interconnection functions and equipment of the distributed resources (DR) conform to IEEE Std 1547.

1.2 Purpose

Interconnection equipment that connects DR to an electric power system (EPS) must meet the requirements specified in IEEE Std 1547. Standardized test procedures are necessary to establish and verify compliance with those requirements. These test procedures must provide both repeatable results, independent of test location, and flexibility to accommodate the variety of DR technologies.

[1]Information on references can be found in Clause 2.

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1.3 Limitations

This standard does not cover testing for safety.

Although this standard does not define a certification process, these tests may be used as part of such a process.

2. Normative references

The following referenced documents are indispensable for the application of this standard. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

The applicability of the following standards is determined by the specific requirements stated in this standard, such as requiring certain sections.

ANSI C37.06, American National Standard for AC High-Voltage Circuit Breakers Rated on a Symmetrical Current Basis—Preferred Ratings and Related Required Capabilities.[2]

ANSI C84.1, American National Standard for Electric Power Systems and Equipment—Voltage Ratings (60 Hz).

IEEE C37.09™, IEEE Standard Test Procedure for AC High-Voltage Circuit Breakers Rated on a Symmetrical Current Basis.[3, 4]

IEEE Std C37.90.1™, IEEE Standard for Surge Withstand Capability (SWC) Tests for Relays and Relay Systems Associated with Electric Power Apparatus.

IEEE Std C37.90.2™, IEEE Standard for Withstand Capability of Relay Systems to Radiated Electromagnetic Interference from Transceivers.

IEEE Std C62.41.2™, IEEE Recommended Practice on Characterization of Surges in Low-Voltage (1000 V and Less) AC Power Circuits.

IEEE Std C62.45™, IEEE Recommended Practice on Surge Testing for Equipment Connected to Low-Voltage (1000 V and Less) AC Power Circuits.

IEEE Std 1547™, IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems.

NEMA MG-1, Motors and Generators.[5]

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3. Definitions and acronyms

For purposes of this standard, the following terms and definitions apply. *The Authoritative Dictionary of IEEE Standards Terms* [B5] should be referenced for terms not defined in this clause.

3.1 ICS boundaries

An ICS consists of system controls, electrical protection, and steady-state control and may include energy conversion and/or generator. The DR may include all or part of the ICS. Figure 1 shows the boundary between the ICS, the EPS, and the energy source.

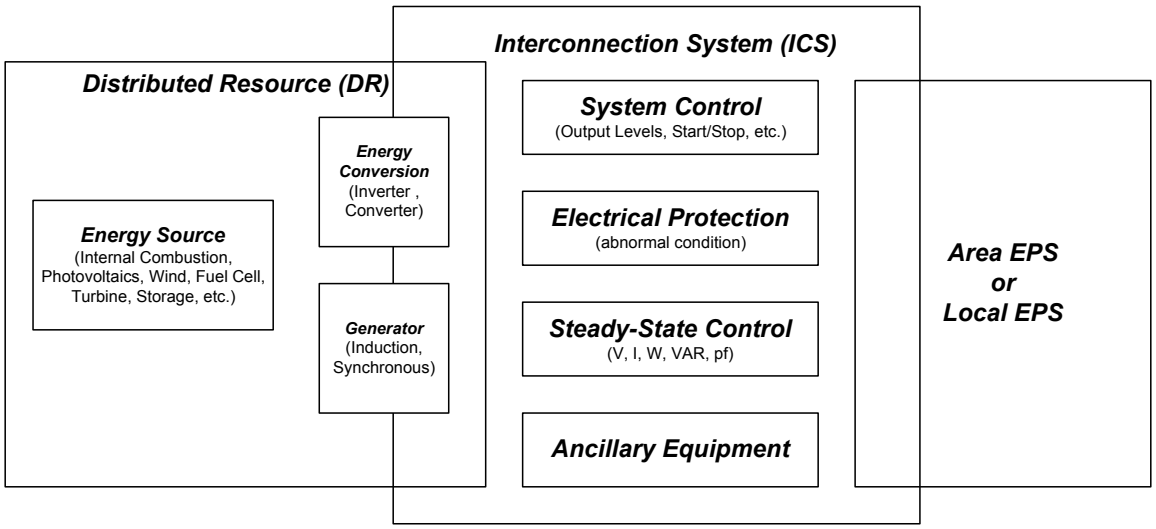


Figure 1—Boundaries between the ICS, the EPS, and the DR

3.2 Definitions

3.2.1 area electric power system (EPS): An EPS that serves local EPSs. Note that, typically, an area EPS has primary access to public rights-of-way, priority crossing of property boundaries, etc., and is subject to regulatory oversight.

3.2.2 clearing time: The time between the start of the abnormal condition and the distributed resources' (DR's) ceasing to energize the area electric power system (EPS). It is the sum of the detection time, any adjustable time delay, the operating time for any interposing devices (if used), and the operating time for the interrupting device (used to interconnect the DR with the area EPS).

3.2.3 commissioning test: A test conducted when the equipment is installed to verify correct operation.

3.2.4 design test: *See:* **type test**.

3.2.5 detection time: The minimum length of time from the inception of the abnormal condition to the change in state of the device or function dedicated to controlling the interrupting device. *Syn:* processing time.

3.2.6 distributed generation (DG): Electric generation facilities connected to an area electric power system (EPS) through a point of common coupling (PCC); a subset of distributed resources (DR).

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3.2.7 distributed resources (DR): Sources of electric power that are not directly connected to a bulk power transmission system. DR includes both generators and energy storage technologies.

3.2.8 electric power system (EPS): Facilities that deliver electric power to a load. Note that EPS may include generation units. *See also:* **area electric power system (EPS)**; **local electric power system (EPS)**.

3.2.9 interconnection system (ICS): the collection of all equipment and functions, taken as a group, used to interconnect a distributed resources (DR) unit to an area electric power system (EPS).

3.2.10 interrupting device: A device capable of being opened and reclosed whose purpose is to interrupt faults and restore service or disconnect loads. These devices can be manual, automatic, or motor-operated. Examples include circuit breakers, motor-operated switches, and electronic switches.

3.2.11 inverter: A machine, device, or system that changes dc power to ac power.

3.2.12 island: A condition in which a portion of an area electric power system (EPS) is energized solely by one or more local EPSs through the associated points of common coupling (PCCs) while that portion of the area EPS is electrically separated from the rest of the area EPS.

3.2.13 local electric power system (EPS): An EPS contained entirely within a single premises or group of premises.

3.2.14 nominal: The value or range of a parameter being within expected norms or being the normal operating level of that parameter.

3.2.15 paralleling device: A device (e.g., circuit breaker) operating under the control of a synchronizing function to electrically connect two energized power sources together.

3.2.16 point of common coupling (PCC): The point where a local electric power system (EPS) is connected to an area EPS.

3.2.17 point of distributed resources (DR) connection: The point where a DR unit is electrically connected in an electric power system (EPS).

3.2.18 production test: A test conducted on every unit of equipment prior to shipment.

3.2.19 signal injection test methods: Test methods where signals are injected into the sense terminals of the equipment under test (EUT). These methods include both primary injection test methods and secondary injection test methods.

3.2.20 simulated area electric power system (EPS): An assembly of voltage and frequency test equipment replicating a utility power source. Where appropriate, the actual area EPS can be used as the simulated area EPS.

3.2.21 simulated utility: *See:* **simulated area electric power system (EPS)**.

3.2.22 total rated-current distortion (TRD): The total root-sum-square of the current harmonics created by the distributed resources (DR) unit operating into a linear balanced load divided by the greater of the test load current demand IL or the rated-current capacity of the DR unit Irated.

3.2.23 trip time: The interval that begins at the leading zero-crossing of the first half cycle of the voltage waveform in which the measured parameter (e.g., frequency, voltage, power) exceeds the trip limit and ends when the equipment under test (EUT) responds as required.

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3.2.24 type test: Test of one or more devices made to a certain design to demonstrate that the design meets certain specifications. *Syn:* design test.

3.3 Acronyms

CT	current transformer
d.p.f.	displacement power factor
DR	distributed resources
EMI	electromagnetic interference
EPS	electric power system
EUT	equipment under test
ICS	interconnection system
PCC	point of common coupling
p.f.	power factor
PUT	parameter under test
RLC	resistance, inductance, and capacitance
rms	root mean square
THD	total harmonic distortion
TRD	total rated-current distortion
VT	voltage transformer

4. General requirements

Implementation of these test procedures shall be conducted in accordance with appropriate safety procedures, sequences, and precautions.

4.1 Test result accuracy

The test results shall verify that the equipment under test (EUT) meets the requirements of IEEE Std 1547 within the manufacturer's specified accuracy.

4.2 Testing environment

The manufacturer shall specify the range of environmental conditions for the EUT. Therefore, tests shall be conducted in an environment that is within the manufacturer's specified environmental operating conditions.

4.3 Measurement accuracy and calibration of the testing equipment

Measurement equipment used to confirm performance of an EUT shall have calibration traceablity. The accuracy of the measuring equipment shall be suitable for the test being conducted.

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4.4 Product information

The setting of limits and the structure of this standard are based on the understanding that the installer and user are responsible for following the installation recommendations of the manufacturer.

The manufacturer shall supply the EUT tester with documentation necessary for the correct installation into a typical system or process in the intended environment. A functional description and a definition of specification limits for the acceptance criteria shall be provided by the manufacturer and noted in the test report.

Any external devices or equipment or special connection requirements necessary to conduct the tests shall be clearly stated (including rationale) in the user documentation. Special requirements can include the amount of network impedance, voltampere burden of the EUT, the use of shielded or special cables, maximum cable length, the use of filters, and the correct bonding to functional earth (grounding). If different devices or connection requirements apply in different environments, this shall also be stated. A list of auxiliary equipment (e.g., options or enhancements) that can be added to the EUT and that can impact the result of EUT tests shall be made available. This information shall also be covered in the test report to clarify the as-tested arrangement(s).

Accuracy and tolerances of device parameters shall be stated by the manufacturers.

4.5 Test reports

The test results shall be documented in a test report. The report shall clearly and unambiguously present all relevant information of the tests (e.g., load conditions, conductor type or routing, functional description, acceptance criteria).

Within the test report, test procedures, as performed, shall be detailed; and engineering considerations, including test modifications and exemptions, shall be justified. When used in conjunction with this standard, the test report shall include sufficient critical operating information to rerun the test and reproduce the results.

Each test method shall be specified; and engineering considerations, including range of operating conditions, shall be justified.

4.6 Testing equipment requirements

4.6.1 Simulated area EPS (utility) source requirements

Where testing allows the use of a simulated area EPS source, the following requirements shall be met:

- The simulated area EPS source shall be capable of confirming the manufacturer's stated performance.
- The voltage harmonics of the simulated area EPS source shall be less than 2.5% total harmonic distortion (THD).
- The individual voltage harmonics of the simulated utility shall be less than 50% of the limits in Table 3 of IEEE Std 1547.
- During the tests, the steady-state voltage of the simulated area EPS source shall not vary by more than ± 1% of the nominal voltage.
- For voltage trip magnitude tests, the voltage change resolution of the simulated utility source shall be within 0.5*a* of the nominal voltage, where *a* is the manufacture's stated accuracy.
- For frequency trip magnitude tests, the frequency change resolution of the simulated utility source shall be within 0.5*a* of the nominal frequency, where *a* is the manufacture's stated accuracy.

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— The number of phase and neutral connections provided by simulated area EPS shall be compatible with the EUT. A multiphase simulated area EPS that provides a neutral connection shall produce phase-to-neutral voltages that are balanced within ± 3% of nominal and phase displacement to within ± 3º. For multiphase simulated area EPSs without a neutral connection, the phase-to-phase voltage balance shall be ± 3% of nominal in magnitude.

— For voltage trip timing tests, the simulated utility source shall be capable of a step change from V_1 to $V_1 + 0.5(V_2 - V_1)$ within the greater of one cycle of the voltage waveform or 1% of the trip time setting of the EUT.[6]

— For frequency trip timing tests, the simulated utility source shall be capable of a step change from f_1 to $f_1 + 0.5(f_2 - f_1)$ within the greater of one cycle of the voltage waveform or 1% of the trip time setting of the EUT.[7]

4.6.2 Measurement system requirements

Each measurement shall have an uncertainty of no more than 0.5 times the accuracy of the EUT. Measurement equipment shall be capable of confirming the manufacturer's stated performance.

5. Type tests

Type tests are performed on a representative unit and may be conducted in the factory, at a testing laboratory, or on equipment in the field. Unless otherwise specified, equipment shall be installed per the manufacturer's specification and operated under nominal operating conditions.

Where the EUT cannot be evaluated using one or more of the test regimens specified in this standard, alternative test regimens agreed to by the manufacturer and the testing agency and accomplishing the same measurements with the same accuracy may be used. When used, the details of such alternative test regimens shall be recorded in the test report along with an explanation of why the alternative test regimen was used.

Signal injection test methods may be used to conduct tests in 5.1, 5.2, 5.3, 5.4, 5.8, and 5.10.

Several test procedures require the EUT be operated at different discrete power levels (e.g., 33%, 66%, and 100% of rated power). Adjustments may be made to the EUT to achieve the discrete power levels, provided that these adjustments do not otherwise affect the performance of the EUT for the parameter under test (PUT). Alternatively, to accomplish testing at discrete power levels, the input source may be power limited to result in the desired EUT output power levels.

IEEE Std 1547 allows for type testing to be performed on complete systems, multifunction relays, discrete devices, or any combination. If type testing is performed on anything other than a fully integrated system, some of the component times in Figure A.1 may not be available. In these cases, production and/or commissioning tests shall be conducted to fully demonstrate the ability of the complete system to comply with the timing required by IEEE Std 1547. As an alternative, that the sum of individual component timings meets the requirement may be shown in the test report.

For the purposes of this standard, multiphase ICSs include single-phase three-wire ICSs.

[6]See Annex A for additional information.
[7]See Footnote 6.

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5.1 Temperature stability

5.1.1 Purpose

This test verifies that the EUT maintains measurement accuracy of parameters over its specified temperature range. EUT functions shall be tested to confirm that they operate within the manufacturer's stated accuracy over the stated operating temperature range. A functional test procedure to exercise each EUT input and output function shall be agreed to by the manufacturer and the testing agency. The functional test procedure shall confirm EUT operation within the manufacturer's stated accuracy for magnitude and time. It is the intent of this test to confirm the manufacturer's specified accuracy over the specified operating temperature range for measurements and timing references used to provide compliance with IEEE Std 1547.

The test consists of two sections. The operational test verifies that the EUT functions per manufacturer's specification over its operating temperature range. The storage test verifies that the EUT can be stored without damage over the manufacturer's specified storage temperature range.

Where protective, monitoring, and control functions can be conveniently separated from the ICS, the remainder of the ICS may be omitted from this test. However, the manufacturer shall provide the testing agency with substantive information to verify that the complete ICS will perform acceptably over the claimed operating temperature range.

5.1.2 Procedure

5.1.2.1 Operational temperature test procedure

To ensure that the equipment has reached the desired temperature, it should be allowed to stabilize at the specified chamber temperature. Stabilized temperature is reached after a minimum of 2.5 hr and when three successive temperature readings taken at 30 min intervals are within 1 °C. For the minimum operating temperature point, the equipment shall remain deengergized until the stable temperature has been achieved.

a) Select test temperatures per the EUT specification. The EUT should be tested at the minimum, nominal (or average of maximum and minimum if not specified), and maximum operating temperatures. If nonlinear response is observed, additional test temperatures should be selected between the minimum and maximum temperatures.

b) The trip and reset parameters to be measured over the temperature range include voltage, current, power, phase angle, frequency, and time function as appropriate for the EUT. The objective is to confirm each subsection of the EUT. The selection of parameters or functions to be evaluated for this test shall be made so that all hardware components (including those that execute software functions) likely to be affected by temperature are evaluated. Where hardware components are common to more that one function, only one of the common functions need be evaluated to confirm accuracy over the specified temperature range.

c) Perform the tests and record the data. Perform a minimum set of tests that will verify that the EUT protective functions will operate properly over the operating temperature range as specified by the manufacturer.

d) At each temperature point selected in step a), repeat each test selected in step b) for a total of five times.

5.1.2.2 Storage temperature test procedure

Select test temperatures per the EUT specification. The EUT should be conditioned at the minimum and maximum storage temperatures. Where the EUT's operating and storage temperatures are the same, this test is not required.

Select the test method. Storage temperature performance can be established in one of two ways:

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— The first method is to review the storage temperature specifications of the individual components of the EUT. If all the components meet the requirements, the EUT meets the requirements.
— The second method is to place the EUT without power for a minimum of 72 hr at each of the temperature extremes. The equipment should be returned to room temperature and proper operation should be verified.

Perform the tests and record the data.

5.1.3 Criteria

5.1.3.1 Operational temperature test

The EUT protective functions shall operate properly over the operating temperature range as specified by the manufacturer.

5.1.3.2 Storage temperature test

The EUT shall function properly after 72 hr at the manufacturer's minimum, nominal, and maximum temperature specifications.

5.1.4 Comments

It may not be necessary or feasible to temperature-test the complete EUT. Per the manufacturer's recommendation, just the components that control the parameters under test need be tested over the specified temperature range. Signal injection testing may be performed with these components per the manufacturer's recommendation.

The EUT should be arranged in the environmental chamber in such a manner that reduces, if not eliminates, opening of the chamber during testing. If the chamber must be left partially open, steps should be taken to minimize heat loss or gain. This is especially important at cold temperatures where opening of the chamber door may cause instant condensation that may affect the test. If the chamber door must be opened during test, allow sufficient time for the temperature to return to the desired test value.

If the EUT has an enclosure, it should be used especially at high temperatures to account for the additional temperature rise due to the enclosure. If including the enclosure is not practical, then the ambient temperature should be increased to a level that is agreed to by the testing agency and EUT manufacturer to account for the additional rise.

Conversely, the use of the enclosure can prevent the equipment from reaching its minimum operating temperature due to the internal rise. To account for this, the equipment should not be energized until the desired low temperature is attained or the temperature is lowered to account for the additional rise. If the manufacturer specifies a cold temperature start-up procedure, that procedure should be followed.

It is recommended that the cold temperature testing be completed first since cooling a heated chamber requires a much longer time than heating a cool chamber.

Care should be taken to mitigate condensation and frosting when performing tests after the cold soak period.

5.2 Test for response to abnormal voltage conditions

If the EUT senses voltage either at the point of common coupling (PCC) with the area EPS or at the point of DR connection as specified in IEEE Std 1547, it may be tested at any convenient load level.

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If the EUT senses voltage at a different point than the PCC with the area EPS or at the point of DR connection as specified in IEEE Std 1547, it shall be tested under load in conjunction with any external isolation transformer supplied or required by the EUT manufacturer.

For a EUT that must be tested under load, these tests may be performed at an output current level convenient to the testing laboratory. When an isolation transformer is provided with or required by the EUT, IEEE 1547 compliance will be based on voltage on the area EPS side of the transformer. Testing under load shall be at both

— Its minimum operating current and
— At both unity power factor (p.f.) and the minimum DR p.f. (leading and lagging) as specified by the manufacturer at as close as possible to 100% full rated output current.

These tests shall be performed at the terminals of the EUT.

Where appropriate, signal injection test methods may be used.

5.2.1 Test for overvoltage

5.2.1.1 Purpose

The purpose of this test is to verify that the DR interconnection component or system ceases to energize the area EPS as specified in IEEE Std 1547 with respect to overvoltage conditions. This test determines the magnitude and trip time for each overvoltage function.

5.2.1.2 Procedure—magnitude

This procedure uses the ramp function defined in Annex A.

a) Connect the EUT according to the instructions and specifications provided by the manufacturer.
b) Set all source parameters to the nominal operating conditions for the EUT.
c) Set (or verify) all EUT parameters to the nominal operating settings. If the overvoltage setting is adjustable, set the EUT to the minimum overvoltage setting, but no less than the nominal voltage plus twice the manufacturer's stated accuracy.
d) Record applicable settings.
e) For single-phase units, adjust voltage to starting point V_b, as defined in Annex A. The source shall be held at this voltage for period t_h.[8] At the end of this period, initiate the ramp using the procedure specified in Annex A. For multiphase units, adjust voltage on one phase to starting point V_b and initiate the ramp using the procedure specified in Annex A. Ensure that remaining phases are held at nominal.
f) Record all voltage magnitudes when the unit trips.
g) Repeat steps d) through f) four times for a total of five tests.
h) For multiphase units, repeat steps d) through g) for each phase individually and all phases simultaneously.
i) If the trip magnitude is adjustable, repeat steps d) through h) at the midpoint and maximum of the range.

5.2.1.2.1 Requirements

If used, the simulated area EPS shall meet the requirements of 4.6.1. The measurement system shall meet the requirements of 4.6.2.

[8]The variable t_h is at least two times the trip time setting. This number may be adjusted to avoid conflict with other trip points.

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If in step h) of the procedure in 5.2.1.2, the simultaneous multiphase test results vary from the individual phase test results by more than the manufacturer's specified accuracy, additional testing may be necessary to verify that the EUT is responding to phase to neutral magnitude changes instead of phase-to-phase magnitude changes.

5.2.1.2.2 Criteria

The EUT shall be considered in compliance if it trips in the overvoltage range specified in IEEE Std 1547.

5.2.1.3 Procedure—trip time

This procedure uses the step function defined in Annex A.

a) Connect the EUT according to the instructions and specifications provided by the manufacturer.
b) Set all source parameters to the nominal operating conditions for the EUT.
c) Set (or verify) all EUT parameters to the nominal operating settings. If the overvoltage trip time setting is adjustable, set it to the minimum.
d) Record applicable settings.
e) Set the source voltage to a value within 10% of, but not exceeding, the overvoltage trip point setting. The source shall be held at this voltage for period t_h.[9] At the end of this period, step the source voltage to a value that causes the unit to trip. Hold this value until the unit trips. For multiphase units, this test may be performed on one phase only.
f) Record the trip time.
g) Repeat steps d) through f) four times for a total of five tests.
h) If the overvoltage time setting is adjustable, repeat steps d) through g) at the midpoint and maximum overvoltage time settings.

5.2.1.3.1 Requirements

If used, the simulated area EPS shall meet the requirements of 4.6.1. The measurement system shall meet the requirements of 4.6.2.

5.2.1.3.2 Criteria

The EUT shall be considered in compliance if the measured trip time is within the clearing time for the overvoltage range specified in IEEE Std 1547.

5.2.2 Test for undervoltage

5.2.2.1 Purpose

The purpose of this test is to verify that the DR interconnection component or system ceases to energize the area EPS as specified in IEEE Std 1547 with respect to undervoltage conditions. This test determines the magnitude and trip time for each undervoltage function.

5.2.2.2 Procedure—magnitude

This procedure uses the ramp function defined in Annex A.

a) Connect the EUT according to the instructions and specifications provided by the manufacturer.
b) Set all source parameters to the nominal operating conditions for the EUT.

[9]See Footnote 8.

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c) Set (or verify) all EUT parameters to the nominal operating settings. If the undervoltage setting is adjustable, set the EUT to the minimum undervoltage setting.

d) Record applicable settings.

e) For single-phase units, adjust voltage to starting point V_b, as defined in Annex A. The source shall be held at this voltage for period t_h.[10] At the end of this period, initiate the ramp using the procedure specified in Annex A. For multiphase units, adjust voltage on one phase to starting point V_b and initiate the ramp using the procedure specified in Annex A. Ensure that remaining phases are held at nominal.

f) Record all voltage magnitudes when the unit trips.

g) Repeat steps d) through f) four times for a total of five tests.

h) For multiphase units, repeat steps d) through g) for each individual phase and all phases simultaneously.

i) If the trip magnitude is adjustable, repeat steps d) through h) at the midpoint and maximum of the range.

5.2.2.2.1 Requirements

If used, the simulated area EPS shall meet the requirements of 4.6.1. The measurement system shall meet the requirements of 4.6.2.

If in step h) of the procedure in 5.2.2.2, the simultaneous multiphase test results vary from the individual phase test results by more than the manufacturer's specified accuracy, additional testing may be necessary to verify that the EUT is responding to phase-to-neutral magnitude changes instead of phase-to-phase magnitude changes.

5.2.2.2.2 Criteria

The EUT shall be considered in compliance if it trips in the undervoltage range specified in IEEE Std 1547.

5.2.2.3 Procedure—trip time

This procedure uses the step function defined in Annex A.

a) Connect the EUT according to the instructions and specifications provided by the manufacturer.

b) Set all source parameters to the nominal operating conditions for the EUT.

c) Set (or verify) all EUT parameters to the nominal operating settings. If the undervoltage trip time setting is adjustable, set it to the minimum.

d) Record applicable settings.

e) Set the source voltage to a value within 10% of, but not exceeding, the undervoltage trip point setting. The source shall be held at this voltage for period t_h.[11] At the end of this period, step the source voltage to a value that causes the unit to trip. Hold this value until the unit trips. For multiphase units, this test may be performed on one phase only.

f) Record the trip time.

g) Repeat steps d) through f) four times for a total of five tests.

h) If the undervoltage time setting is adjustable, repeat steps d) through g) at the midpoint and maximum undervoltage time settings.

[10]See Footnote 8.
[11]See Footnote 8.

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5.2.2.3.1 Requirements

If used, the simulated area EPS shall meet the requirements of 4.6.1. The measurement system shall meet the requirements of 4.6.2.

5.2.2.3.2 Criteria

The EUT shall be considered in compliance if the measured trip time is within the clearing time for the undervoltage range specified in IEEE Std 1547.

5.3 Response to abnormal frequency conditions

5.3.1 Test for overfrequency

5.3.1.1 Purpose

The purpose of this test is to verify that the DR interconnection component or system ceases to energize the area EPS as specified in IEEE Std 1547 with respect to overfrequency conditions. This test determines the magnitude and trip time for each overfrequency function.

5.3.1.2 Procedure—magnitude

This procedure uses the ramp function defined in Annex A.

a) Connect the EUT according to the instructions and specifications provided by the manufacturer.
b) Set all source parameters to the nominal operating conditions for the EUT.
c) Set (or verify) all EUT parameters to the nominal operating settings. If the overfrequency setting is adjustable, set the EUT to the minimum overfrequency setting.
d) Record applicable settings.
e) Adjust the source frequency to starting point fb. The source shall be held at this frequency for period t_h.[12] At the end of this period, initiate the ramp using the procedure specified in Annex A.
f) Record the frequency at which the unit trips.
g) Repeat steps d) through f) four times for a total of five tests.
h) If the overfrequency setting is adjustable, repeat steps d) through g) at the midpoint and maximum overfrequency settings.

5.3.1.2.1 Requirements

If used, the simulated area EPS shall meet the requirements of 4.6.1. The measurement system shall meet the requirements of 4.6.2.

5.3.1.2.2 Criteria

The EUT shall be considered in compliance if it trips in the overfrequency range specified in IEEE Std 1547.

5.3.1.3 Procedure—trip time

This procedure uses the step function defined in Annex A.

a) Connect the EUT according to the instructions and specifications provided by the manufacturer.

[12]See Footnote 8.

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b) Set all source parameters to the nominal operating conditions for the EUT.

c) Set (or verify) all EUT parameters to the nominal operating settings. If the overfrequency trip time setting is adjustable, set it to the minimum.

d) Record applicable settings.

e) Set the source frequency to a value within 1% of, but not exceeding, the overfrequency trip point setting. The source shall be held at this frequency for period t_h.[13] At the end of this period, step the source frequency to a value that causes the unit to trip. Hold this value until the unit trips.

f) Record the trip time.

g) Repeat steps d) through f) four times for a total of five tests.

h) If the overfrequency time setting is adjustable, repeat steps d) through g) at the midpoint and maximum overfrequency time settings.

5.3.1.3.1 Requirements

If used, the simulated area EPS shall meet the requirements of 4.6.1. The measurement system shall meet the requirements of 4.6.2.

5.3.1.3.2 Criteria

The EUT shall be considered in compliance if the measured trip time is within the clearing time for the overfrequency range specified in IEEE Std 1547.

5.3.1.3.3 Comments

For some EUT, the step size past the frequency trip limit should be as small as possible to reduce false results. Large frequency step changes can interfere with EUT phase lock loop operation.

5.3.2 Test for underfrequency

5.3.2.1 Purpose

The purpose of this test is to verify that the DR interconnection component or system ceases to energize the area EPS as specified in IEEE Std 1547 with respect to underfrequency conditions. This test determines the magnitude and trip time for each underfrequency function.

5.3.2.2 Procedure—magnitude

This procedure uses the ramp function defined in Annex A.

a) Connect the EUT according to the instructions and specifications provided by the manufacturer.

b) Set all source parameters to the nominal operating conditions for the EUT.

c) Set (or verify) all EUT parameters to the nominal operating settings. If the underfrequency setting is adjustable, set the EUT to the minimum underfrequency setting.

d) Record applicable settings.

e) Adjust the source frequency to starting point fb. The source shall be held at this frequency for period t_h.[14] At the end of this period, initiate the ramp using the procedure specified in Annex A.

f) Record the frequency at which the unit trips.

g) Repeat steps d) through f) four times for a total of five tests.

[13]See Footnote 8.

[14]See Footnote 8.

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h) If the underfrequency setting is adjustable, repeat steps d) through g) at the midpoint and maximum underfrequency settings.

5.3.2.2.1 Requirements

If used, the simulated area EPS shall meet the requirements of 4.6.1. The measurement system shall meet the requirements of 4.6.2.

5.3.2.2.2 Criteria

The EUT shall be considered in compliance if it trips in the underfrequency range specified in IEEE Std 1547.

5.3.2.3 Procedure—trip time

This procedure uses the step function defined in Annex A.

a) Connect the EUT according to the instructions and specifications provided by the manufacturer.
b) Set all source parameters to the nominal operating conditions for the EUT.
c) Set (or verify) all EUT parameters to the nominal operating settings. If the underfrequency trip time setting is adjustable, set it to the minimum.
d) Record applicable settings.
e) Set the source frequency to a value within 1% of, but not exceeding, the underfrequency trip point setting. The source shall be held at this frequency for period t_h.[15] At the end of this period, step the source frequency to a value that causes the unit to trip. Hold this value until the unit trips.
f) Record the trip time.
g) Repeat steps d) through f) four times for a total of five tests.
h) If the underfrequency time setting is adjustable, repeat steps d) through g) at the midpoint and maximum underfrequency time settings.

5.3.2.3.1 Requirements

If used, the simulated area EPS shall meet the requirements of 4.6.1. The measurement system shall meet the requirements of 4.6.2.

5.3.2.3.2 Criteria

The EUT shall be considered in compliance if the measured trip time is within the clearing time for the underfrequency range specified in IEEE Std 1547.

5.3.2.3.3 Comments

For some EUT, the step size past the frequency trip limit should be as small as possible to reduce false results. Large frequency step changes can interfere with EUT phase lock loop operation.

5.4 Synchronization

The purpose of the tests in this subclause is to demonstrate that the EUT will accurately and reliably synchronize to the area EPS according to the requirements of IEEE Std 1547. Separately excited induction generators shall be tested using the procedure for synchronous generators.

[15]See Footnote 8.

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Two basic test methods are provided:

— Method 1 verifies that a synchronization control function will cause the paralleling device to close only when key synchronization parameters are within allowable limits.

— Method 2 determines the magnitude of the synchronization startup current.

Equipment that can generate voltage independently of the area EPS and is thus capable of out-of-phase paralleling with the area EPS (e.g., a synchronous generator or inverter operating in a stand-alone mode) is tested to verify compliance of its synchronizing capability using Method 1.

Equipment that utilizes energy from the area EPS service to begin operation (e.g., an induction generator) and that may draw high current levels is tested to determine the synchronization current using Method 2. Equipment that generates a voltage inherently synchronized to the area EPS is also tested to determine the synchronization current using Method 2. This current value can then be used along with area EPS impedance at a specific location to estimate the maximum voltage fluctuation related to synchronization.

The EUT addressed in these procedures includes a wide range of capabilities, ranging from discrete components providing control and protection functions to complete generator equipment facilities. The intent of the testing requirement in this subclause is that the user identify the procedure most appropriate for the particular situation and use that procedure to validate equipment performance. IEEE Std 1547 requires that when paralleling with the area EPS, the DR should not cause excessive voltage fluctuation. Therefore, when in doubt, Method 2 should be used. Some equipment with multiple operating modes may have to be tested using both of the basic methods.

Three variations of Method 1 are provided. The first variation (5.4.1) assumes a simulated generator source and would be performed, for example, on a discrete relay or multifunction controller with synchronization control function. The second variation (5.4.2) assumes a real generator source is used. The third variation (5.4.3) is designed for testing of equipment in which the synchronizing functions cannot be switched off or the sensing voltage cannot be conveniently disconnected.

5.4.1 Synchronization control function test using simulated sources (Method 1, variation 1)

5.4.1.1 Purpose

The purpose of these tests is to demonstrate that interconnection equipment will synchronize to the area EPS across an open paralleling device (e.g., a power circuit breaker), within allowable limits of voltage, frequency, and phase-angle difference before the paralleling device is allowed to close. The procedure is intended for a discrete or multifunction interconnection control device that includes a synchronization function and may be used in laboratory tests with simulated generator equipment and a simulated area EPS source.

If the EUT does not include a paralleling device, the acceptability of the ICS for a specific site depends on the speed of operation of the paralleling device to be used with the EUT.

5.4.1.2 Procedure

a) Connect the EUT according to the instructions and specifications provided by the manufacturer.

b) Connect the test equipment to monitor the paralleling device close command, the phase relationship between simulated generator output and area EPS sources, the frequency of each source, and the voltage of each source.

c) Set simulated area EPS source to operate at nominal voltage and frequency. Record applicable settings.

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d) Demonstrate that the equipment will not close outside of the voltage acceptance range defined in IEEE Std 1547, but will close within that acceptance range. By holding the voltage and frequency of the simulated area EPS source at constant nominal values and varying the voltage of the generator source, the test will demonstrate that the EUT will not initiate closing outside of acceptable ranges of voltage and will close within acceptable ranges. The test will demonstrate that the EUT functions properly both from a low voltage that is raised to within an acceptable level and from a high voltage that is lowered to within an acceptable level. The following process may be used for testing the voltage:

1) Set the voltage and frequency of the area EPS source to nominal values.
2) Set the voltage of the simulated generator source to a level above the area EPS source voltage so that the voltage difference is outside the acceptance range, but the generator voltage is below the overvoltage trip limit of the EUT (if so equipped). The voltage difference should be at least twice the manufacturer's stated accuracy.[16]
3) Set and hold the frequency of the simulated generator source to that of the simulated area EPS so that frequency difference and phase angle[17] are within the limits allowed by the requirements of IEEE Std 1547. Include an allowance for EUT accuracy so that frequency and phase angle do not inadvertently keep the EUT from initiating a paralleling device closure.
4) Verify for a period of at least 3 min that the EUT does not initiate closing.
5) Gradually reduce the generator source voltage until the voltage difference is within the acceptance values of IEEE Std 1547 including an allowance for EUT accuracy. The voltage ramp rate should be controlled to allow reliable indication of the point at which paralleling device closure is initiated. A procedure for determining ramp rates is described in Annex A.
6) Record the voltage and frequency for the area EPS and generator sources, as well as the voltage, frequency, and phase-angle differences between the two sources at the point at which the EUT initiates paralleling device closure.
7) Repeat steps a) through f) four times for a total of five sets of readings.
8) Repeat steps a) through g) except with the initial simulated generator source voltage set at a level below the area EPS source voltage so that the voltage difference is outside the acceptance range, but the generator voltage is above the undervoltage trip limit of the EUT.

e) Demonstrate that the equipment will not close outside of the frequency and phase-angle acceptance range defined in IEEE Std 1547, but will close within that acceptance range. By holding the voltage and frequency of the area EPS source constant and varying the frequency of the generator source, the test will demonstrate that the EUT will not initiate paralleling device closure outside of acceptable ranges of frequency difference and phase angle and will initiate paralleling device closure within acceptable ranges. The test will demonstrate that the EUT functions properly starting from both a low frequency that is raised to within an acceptable level and from a high frequency that is lowered to within an acceptable level.

1) Set the voltage and frequency of the area EPS source to nominal values. Set the generator source voltage to that of the area EPS.
2) Set the frequency of the simulated generator source to a level above the area EPS source frequency so that the frequency difference is outside the acceptance range, but the generator frequency is below the overfrequency trip limit of the EUT (if so equipped). The frequency difference should be at least twice the stated accuracy of the EUT.
3) Set and hold the voltage of the simulated generator source to that of the simulated area EPS so that voltage difference is within the limits allowed by the requirements of IEEE Std 1547. Include an allowance for EUT accuracy so that voltage difference does not inadvertently keep the EUT from initiating a paralleling device closure.

[16]If the EUT stated measurement accuracy is 1%, the initial voltage difference should be at least 2% greater than the allowable limit.

[17]If the generator source frequency and utility source frequency are not identical, phase angle will periodically be within allowable limits.

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4) Verify for a period of at least 3 min that the EUT does not initiate paralleling device closure.
5) Gradually reduce the generator source frequency until the frequency difference is within the acceptance values of IEEE Std 1547 including an allowance for EUT accuracy. The frequency ramp rate should be controlled to allow reliable indication of both the frequency and phase angle at which paralleling device closure is initiated. A procedure for determining ramp rates is described in Annex A.
6) Record the voltage and frequency for the area EPS and generator sources, as well as the voltage, frequency, and phase-angle differences between the two sources at the point at which the EUT initiates paralleling device closure.
7) Repeat steps a) through f) four times for a total of five sets of readings.
8) Repeat steps a) through g) except with the initial simulated generator source frequency set at a level below the area EPS source frequency so that the frequency difference is outside the acceptance range, but the generator frequency is above the underfrequency trip limit of the EUT.

5.4.1.3 Requirements

Programmable arbitrary waveform generators (multiphase as necessary) may be used to provide simulated generator and area EPS voltage waveforms. The waveform generator will provide voltage and frequency signals in a form compatible with the EUT.

Simulated generator voltage and frequency control will come either from the EUT or, for passive devices, from a control computer programmed to provide the desired waveforms.

Equipment steady-state operating performance shall meet the manufacturer's standards for speed and voltage stability at no load for at least 15 min.

5.4.1.4 Criteria

The testing shall demonstrate that the equipment complies with the requirements of IEEE Std 1547 for synchronization parameter limits.

Test results shall demonstrate that the EUT will not initiate closure out of range for any parameter during any test.

5.4.1.5 Comments

Since the EUT in this test procedure may not incorporate a paralleling device, the documentation should note that, when applied, the phase angle at the instant of closing would be different from what is recorded during this test due to the closing time required for the anticipated paralleling device. The EUT may incorporate provisions to allow compensation for paralleling device operation time.

If parallel device closing time compensation was used, verify that the synchronization device accurately predicted the proper closing angle prior to the specified phase-angle window. Following is a sample calculation:

Given:

paralleling device closing time = 5 cycles

frequency differential at time of parallel device close command = 0.10 Hz

maximum phase-angle window = 10°

Then:

phase rotation rate = frequency differential × 360° = 0.10 Hz × 360° = $36° s^{-1}$

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paralleling device closing time = 5 cycles @ 60 Hz = 0.0833 s

predictive closing angle = $36°s^{-1} \times 0.0833$ s = 3°

Therefore, if the maximum allowable phase angle at paralleling device closure is 10° and the equipment is approaching synchronization, the initiation point could be 10° + 3° = 13°. If the equipment was moving away from synchronization, maximum deviation at initiation would be 10° – 3° = 7°.

5.4.2 Synchronization control function test using actual generator equipment (Method 1, variation 2)

5.4.2.1 Purpose

The purpose of these tests is to demonstrate that synchronous generator equipment will accurately and reliably synchronize to the area EPS across an open paralleling device (e.g., a power circuit breaker), according to the requirements of IEEE Std 1547.

These procedures may also be used with separately excited induction equipment or with inverter equipment that is able to operate in isolation from the area EPS and to resynchronized with the area EPS.

5.4.2.2 Procedure

a) Connect the EUT according to the instructions and specifications provided by the manufacturer. Installation must include verification of the ratings, phasing, and connection of the current transformers (CTs) and voltage transformers (VTs) (if used) in the system that provides input to the control and protection functions.

b) Connect the test equipment to monitor the paralleling device close command, the phase relationship between sources, the frequency of each source, and all phases of the voltage of the generator and of the area EPS.

c) Verify that the EUT is operating at a stable voltage and frequency. Set equipment to operate at rated voltage and frequency. Verify that the equipment operates within the frequency and voltage regulation specifications of the manufacturer while operating in isolation from the area EPS. Stability should be verified at various load levels up to the maximum that it will be required to carry. Record applicable settings, and record voltage and frequency regulation performance.

d) Measure and record the closing time of the paralleling device. Repeat four times for a total of five tests.

e) Set the generator to the nominal frequency and voltage of the area EPS. Disable paralleling device closure and initiate synchronizing action. Verify that the synchronizing function will correctly operate to close the paralleling device when the generator is properly synchronized. If the paralleling device includes a test position that does not allow connection to the area EPS, use of the test position to verify paralleling device operation is acceptable.

f) Enable paralleling device closing.

g) Demonstrate that the equipment will not close outside of the allowed acceptance range for voltage and will close within the voltage range values required by IEEE Std 1547. The required process holds the frequency of the generator source constant and nearly identical to the area EPS source and, by varying the voltage, will demonstrate that the equipment will not initiate closing out of acceptable ranges of voltage, and will close within acceptable parameters. The test will demonstrate that the equipment functions properly both from a low voltage that is raised to an acceptable level, and from a high voltage that is lowered to within acceptable range. The following process may be used (at various points in the following procedure, it may be necessary to reset various parameters to proceed):

   1) If applicable, disable the synchronizing function.

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2) Set and hold the voltage of the generator to a level so that the voltage difference is outside the acceptance range, but within the acceptable voltage and frequency operating range of the ICS. The level selected should be higher than the acceptance range and high enough so that the accuracy of the EUT will not inadvertently initiate operation.

3) Set and hold the frequency of the generator source to that of the area EPS. Maintain the phase angle to within the acceptance limits of IEEE Std 1547.

4) Verify for a period of at least 3 min that the interconnection equipment does not initiate closing.

5) Gradually reduce the voltage difference to within the acceptance values of IEEE Std 1547. The rate of ramp of the voltage parameter should be controlled to a value that allows reliable indication of the initiation point. A procedure for determining ramp rates is described in Annex A. Record the voltage differential at the time of initiation of closure.

6) Repeat steps a) through e) except with the initial generator voltage below the area EPS source voltage. The level should be lower than the acceptance range and should be selected so that the accuracy of the EUT will not inadvertently initiate operation.

h) Demonstrate that the equipment will not close outside of the acceptance range due to improper frequency sensing or phase-angle sensing and will close within the values of IEEE Std 1547. The required process holds the voltage of the simulated generator source constant and nearly identical to the area EPS source and, by varying the frequency, will demonstrate that the equipment will not initiate closing out of acceptable ranges of frequency and phase angle and will close within acceptable parameters. The test will demonstrate that the equipment functions properly both from a low frequency that is raised to an acceptable level and from a high frequency that is lowered to within acceptable range. The following process may be used:

1) Set the frequency of the generator source to a level so that the frequency difference is outside the acceptance range, but within the acceptable voltage and frequency operating range of the ICS. The level selected should be higher than the acceptance range and high enough so that the accuracy of the EUT will not inadvertently initiate operation.

2) Set the voltage of the generator source to that of the area EPS source.

3) Hold the voltage and frequency constant. Verify for a period of at least 3 min that the interconnection equipment does not initiate closing. (This step may require disabling the automatic synchronizing function of the generator.)

4) Gradually reduce the frequency difference to within the acceptance values of IEEE Std 1547. The ramp rate of the frequency parameter should be controlled to a value that allows reliable indication of the initiation point. A procedure for determining ramp rates is described in Annex A. Record the frequency differential and phase-angle deviation at the time of initiation of closure.

5) Repeat steps a) through d) except with the initial generator frequency below the area EPS source frequency. The level should be lower than the acceptance range and should be selected so that the accuracy of the EUT will not inadvertently initiate operation.

i) Repeat this test procedure four times for a total of five tests.

5.4.2.3 Requirements

If used, the simulated area EPS shall meet the requirements of 4.6.1.

If an actual area EPS source is used, the area EPS source must remain within the undervoltage, overvoltage, underfrequency, and overfrequency trip limits defined by IEEE Std 1547.

Frequency should be set at nominal and maintained within ± 0.05 Hz.

The measurement system shall meet the requirements of 4.6.2.

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5.4.2.4 Criteria

The testing shall demonstrate that the equipment complies with the requirements of IEEE Std 1547 for synchronizing performance. IEEE Std 1547 presumes that the voltage fluctuation requirement is met by successful completion of these tests.

Test results shall demonstrate that contacts will not close out of range during any test.

5.4.2.5 Comments

There are a large number of potential application issues that affect the performance of the synchronizing equipment. In particular, phase rotation of generator sets relative to the grid, phasing of potential transformers serving protection and control equipment, and many other factors. Therefore, it is critical that careful attention be paid to the manufacturer's installation instructions and system design drawings to avoid out-of-phase paralleling of the generator equipment to the area EPS.

5.4.3 Synchronization control function test for equipment with no synchronizing disable capability (Method 1, variation 3)

5.4.3.1 Purpose

The purpose of this test is to demonstrate that the EUT will synchronize to the area EPS across an open paralleling device, within allowable limits of voltage, frequency, and phase-angle difference before the paralleling device is allowed to close. The procedure is intended for equipment that automatically synchronizes when a reference voltage source is available, maintains synchronization prior to connecting with the area EPS, and does not include a means to disable or disconnect the synchronizing function.

5.4.3.2 Procedure

a) Install and adjust the EUT according to the manufacturer's recommendations and specifications.

b) Connect test equipment to monitor the paralleling device close command, the phase relationship between EUT output and area EPS sources, the frequency difference, voltage difference, and phase angle between the sources.

c) Set simulated area EPS source to operate at nominal voltage and frequency. Record applicable settings.

d) Disconnect the area EPS from the EUT.

e) Enable all monitoring equipment. Reapply the area EPS and record all required parameters (i.e., voltage, frequency, and phase-angle differences) during the paralleling operation.

f) Repeat this test procedure four times for a total of five tests.

5.4.3.3 Requirements

If used, the simulated area EPS shall meet the requirements of 4.6.1. The measurement system shall meet the requirements of 4.6.2.

5.4.3.4 Criteria

The testing shall demonstrate that the equipment complies with the requirements of IEEE Std 1547 for synchronization parameter limits.

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5.4.4 Startup current measurement (Method 2)

5.4.4.1 Purpose

The purpose of these tests is to determine the maximum startup (in-rush) current drawn by an EUT (e.g., a line-excited induction generator) or by inverter equipment that does not produce output voltage at the time of connecting to the area EPS. The results of this test may be used along with information for the proposed location to verify that the EUT will not violate the synchronizing or flicker requirements of IEEE Std 1547 as installed.

5.4.4.2 Procedure

Induction generator equipment may be evaluated using NEMA MG-1. (Manufacturer's data are acceptable if available and directly applicable based on the application voltage level.)

Induction generator equipment or inverter equipment may be evaluated using the following procedure:

a) Set up the EUT according to the manufacturer's specifications connected to a simulated or actual area EPS.

b) The input power source to the EUT shall be capable of providing at least 120% of rated input power and any normal startup transients.

c) EUT startup shall follow the manufacturer's specified procedure.

d) Begin with the EUT shutdown.

e) Enable monitoring equipment to record area EPS voltages on all phases (line-to-line and line-to-neutral if it can be connected in that configuration) and to record EUT output current on all phases.

f) Initiate a normal EUT startup procedure.

g) Repeat the test nine times for a total of ten tests.[18]

h) For each test, calculate the startup current. The startup current is the maximum value of root-mean-square (rms) current calculated over any consecutive 5-cycle window during the startup process. The EUT maximum startup current is the maximum value of the startup current obtained on any phase in any of the ten tests.

i) Document the impedance of the source used on the test.[19]

5.4.4.3 Requirements

If used, the simulated area EPS shall meet the requirements of 4.6.1.

The measurement system shall meet the requirements of 4.6.2. Voltage and current waveform measurements shall be recorded at a sample rate of at least 600 Hz per channel to provide at least 10 samples per cycle.

5.4.4.4 Criteria

This test determines the magnitude of current drawn (or sourced) by the EUT at startup so that voltage fluctuation (flicker) calculations can be completed for a specific site. This is a characterization test—there are no specific pass/fail criteria except as applied at a specific site.

[18]The number of tests was selected to assure that a maximum value is obtained.

[19]The Thevenin impedance of the area EPS will have a significant effect on the value of the flicker. An infinite bus will create low flicker values while a high impedance system will result in high flicker values. Impedance of the source can be determined by calculations based on the Thevenin impedance (e.g., source transformer and wiring) or empirically determined by using a load large enough to cause a voltage drop.

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The value reported for the EUT shall be the highest of the ten tests. A graphical representation of the time-current characteristic along with the calculated startup current shall be included in the test report.

5.5 Interconnection integrity

5.5.1 Protection from electromagnetic interference (EMI) test

5.5.1.1 Purpose

The purpose of these tests is to determine the EUT's protection from EMI and to confirm that the results are in compliance with IEEE Std 1547.

5.5.1.2 Procedure

The interconnection equipment of the EUT shall be tested in accordance with IEEE Std C37.90.2. This test shall be applied to one parameter and trip function representative of the EUT utility protective function measurement system.

5.5.1.3 Criteria

The influence of EMI shall not result in a change in state or misoperation of the interconnection functions of the EUT.

5.5.2 Surge withstand performance test

5.5.2.1 Purpose

The purpose of this test is to verify the level of surge withstand protection specified by the manufacturer of the EUT. The EUT shall be tested to verify the level of surge withstand protection as specified by the manufacturer and in accordance with IEEE Std C62.41.2 and/or IEEE Std C37.90.1, as applicable.

5.5.2.2 Procedure

The manufacturer shall specify the location category and exposure level of the tests required by IEEE Std C62.41.2 and/or IEEE Std C37.90.1.

a) Apply IEEE Std C37.90.1 to test appropriate EUT external signal and control circuits.

b) Apply IEEE Std C62.41.2 and IEEE Std C62.45 to test appropriate EUT power circuits.

   The EUT shall be tested in all normal operating modes in accordance with IEEE Std C62.45 for equipment rated less than or equal to 1000 V to confirm that the surge withstand capability is met by using the selected test level(s) from IEEE Std C62.41.2. The test should be conducted while the EUT is operating under nominal power unless it can be shown that the surge protection is not affected by its operational state. Equipment rated greater than 1000 V shall be tested in accordance with the applicable standards as designated by the manufacturer or system integrator.

5.5.2.3 Criteria

The results of these tests shall indicate the interconnection functions of the EUT did not fail, did not misoperate, and did not provide misinformation.

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5.5.3 Dielectric test for paralleling device

The following test is for EUT that operate at 1000 V or less. For systems over 1000 V, the EUT shall be tested in accordance with the power frequency dielectric withstand rating specified in Table 4 of ANSI C37.06 and the procedures specified in 4.4.3.1 of IEEE Std C37.09.

5.5.3.1 Purpose

This test determines if the paralleling device of the EUT, while at normal operating temperature, can withstand for 1 min without breakdown the application of an ac rms test potential of 1000 V plus 220% of the nominal ac rms voltage.

5.5.3.2 Procedure

The unit is to be tested using a 500 VA or larger capacity transformer or dielectric tester, the output voltage of which is variable. The applied potential is to be increased from zero until the required test level is reached and is to be held at that level for 60 s. The increase in applied potential is to be at a substantially uniform rate as rapid as is consistent with correct indication of its value by a voltmeter.

— Exception 1: When a voltmeter is connected across the output circuit to directly indicate the test potential, the transformer is not required to be rated 500 VA or more.

— Exception 2: A dc test voltage of 220% of the nominal ac peak voltage plus 1400 V may be used for the dielectric test.

A low-voltage control circuit or a sensor circuit is not required to be connected during the test. Any circuit that is connected from input to output circuit shall remain connected during the test and provide proper isolation.

5.5.3.3 Criteria

The paralleling device of the EUT shall be capable of withstanding the applied test voltage for 60 s. There shall be no flashovers during the test, and no damage to the insulation shall be observed after the test.

5.5.3.4 Comments

This test should be applied only to the paralleling device as specified in IEEE Std 1547.

5.6 Limitation of dc injection for inverters without interconnection transformers

5.6.1 Purpose

The purpose of this test is to verify that an inverter that connects to the EPS complies with the dc injection limit specified in IEEE Std 1547. This test is conducted on inverters that connect to the EPS without the use of dc-isolation output transformers.

5.6.2 Procedure and data analysis

Operating power levels in this procedure have a tolerance of ± 5%.

a) Connect the EUT according to the instructions and specifications provided by the manufacturer.

b) Set all source parameters to the nominal operating conditions for the EUT.

c) Set (or verify) all EUT parameters to the nominal operating settings.

d) Record applicable settings.

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e) Operate the EUT at 33% of its continuous rated output current[20] and at rated p.f. Allow the EUT to operate for at least 5 min prior to taking any test measurements (or until the EUT temperature stabilizes). The EUT shall operate at the specified current and p.f. for the duration of the test.

f) At the EUT output, measure the rms voltage, rms current, and dc component (frequency less than 1 Hz) of current on all phases. The averaging window for all measurements shall be not less than one cycle and not more than 60 cycles.

g) Record all measurements at a sampling rate of not less than the reciprocal of the selected averaging window[21] for a period of 5 min.

h) Repeat steps e) through g) with the DR operating at 66% and at a level as close to 100% of its rated output current as practical.

For all output current levels tested, the following data analysis is required:

a) Calculate average values of rms current and voltage on each phase. For each measurement, the average shall include every sample point recorded during the 5 min test period.

b) Verify that the average rms current on each phase is within 5% of the intended test point (33%, 66%, and 100%).

c) Verify that the average rms voltage on each phase is within 5% of the nominal voltage.

d) Calculate average values for the magnitude of the dc component of current on each phase. The average shall be taken of the absolute (unsigned) value of every sample point recorded during the 5 min test period.

e) For each phase, divide the average dc component magnitude value by the rated output current of the EUT and multiply the result by 100. Record the final calculated values as the percent dc injection current for each phase.

5.6.3 Requirements

If used, the simulated area EPS shall meet the requirements of 4.6.1 and shall have negligible dc offset.

5.6.4 Criteria

The EUT shall be considered in compliance if all calculated percent dc injection currents are within the limit specified in IEEE Std 1547.

5.6.5 Comments

This test may be conducted as part of the harmonics test.

If a simulated area EPS is used, a dedicated isolation transformer should be used.

5.7 Unintentional islanding

The unintentional islanding test given in 5.7.1 is universally acceptable for all DR ICSs. ICSs intended for use solely with synchronous generators may alternatively use the procedures in 5.7.2. Reverse-power function used for detecting an unintentional island shall be tested in accordance with 5.8, instead of the test in this subclause.

[20]Use the grid-connected current rating for units that offer stand-alone and grid-connected mode.

[21]For block averaging or moving average filters, the averaging window is the period over which the averages are taken. For other filters, the averaging window is the reciprocal of the filter bandwidth in hertz.

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This test addresses several EUT output power levels including EUT set power levels and levels limited by the DR input source.

5.7.1 Unintentional islanding test

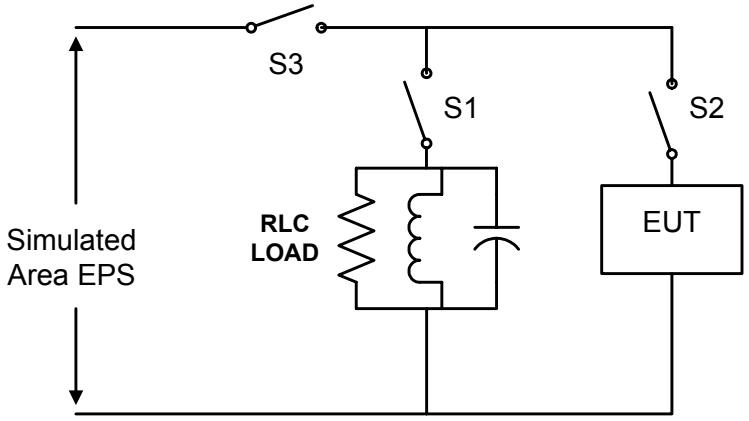
5.7.1.1 Purpose

The purpose of this test is to verify that the DR interconnection component or system ceases to energize the area EPS as specified in IEEE Std 1547 when an unintentional island condition is present. This test determines the trip time for the test conditions specified in 5.7.1.

5.7.1.2 Procedure

This test procedure is designed to be universally applicable to all DRs, regardless of output p.f. Any reactive power compensation by the EUT should remain on during the test.

Where the EUT manufacturer requires an external or separate transformer, the transformer is to be connected between the EUT and resistance, inductance, and capacitance (RLC) load specified in Figure 2[22] and is to be considered part of the product being tested.



NOTES

1—Switch S1 may be replaced with individual switches on each of the RLC load components.

2—Unless the EUT has a unity output p.f., the reactive power component of the EUT is considered to be a part of the islanding load circuit in the figure.

Figure 2—Unintentional islanding test configuration

a) For a single-phase EUT, the test circuit shall be configured as shown in Figure 2. The neutral connection (grounded conductor) of the RLC load, the simulated area EPS, and the EUT shall be unaffected by the operation of switch S3. For a multiphase EUT, the balanced load circuit shown in Figure 2 is to be applied between each phase to neutral for a four-wire configuration or between phases for a three-wire configuration. Switch S3, as shown in Figure 2, shall be gang-operated and multi-pole.

b) Connect the EUT according to the instructions and specifications provided by the manufacturer.

c) Set all EUT input source parameters to the nominal operating conditions for the EUT.

[22]Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement this standard.

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d) Set (or verify) all EUT parameters to the nominal operating settings.

e) Set the EUT (including the input source as necessary) to provide 100% of its rated output power.[23]

f) Record all applicable settings.

g) Set the Simulated EPS to the EUT nominal voltage ± 2% and nominal frequency ± 0.1 Hz.

h) Adjust the islanding load circuit in Figure 2 to provide a quality factor Q_f of 1.0 ± 0.05 (when Q_f is equal to 1.0, the following applies: $P_{qL} = P_{qC} = 1.0 \times P$).[24] The value of Q_f is to be determined by using the following equations as appropriate:

$$Q_f = R\sqrt{\frac{C}{L}}$$

or

$$Q_f = \frac{\sqrt{P_{qL} \times P_{qC}}}{P}$$

where

Q_f is the quality factor of the parallel (RLC) resonant load,

R is the effective load resistance (Ω),

C is effective load capacitance (F),

L is effective load inductance (H),

P_{qL} is the reactive power per phase consumed by the inductive load component (VARS),

P_{qC} is the reactive power per phase consumed by the capacitive load component (VARS),

P is the real output power per phase of the unit (W),

f is frequency.

The inductance and capacitance are to be calculated using the following equations:

$$L = \frac{V^2}{2 \times \pi \times f \times P \times Q_f}$$

$$C = \frac{P \times Q_f}{2 \times \pi \times f \times V^2}$$

where

L is effective load inductance (H),

V is the nominal voltage across each phase of the RLC load (V) (for loads connected phase to phase, V is the nominal line voltage; for loads connected phase to neutral, V is the nominal phase voltage),

[23]EUT provided with or intended for use with specific defined input sources that can not provide the input power range described in this test shall be tested within the limitations of the specified or supplied input source. Under these circumstances the test may be performed with the actual source or a simulated source. Test results will be applicable only to the combination of the EUT and specified source, and the test report should reflect this limitation.

[24]Based on the equation Q_f = Tan(ArcCos(d.p.f.)), where d.p.f is the displacement power factor, a Q_f of 2.5 is equivalent to an uncorrected load d.p.f of 0.37, a Q_f of 1.8, uncorrected load d.p.f. of 0.48, and a Q_f of 1, uncorrected load d.p.f. of 0.707. Area EPS circuits typically operate above 0.75 d.p.f. in steady-state conditions; therefore, Q_f = 1 (d.p.f.=0.707) is below the load d.p.f. that the DR is expected to be islanded with. For a point of comparison, the current draft of IEC 62116 [B4] uses a Q_f of 0.65 (d.p.f. of 0.84). A lower value of Q will allow DR manufacturers to use perturbation schemes that are potentially less detrimental to power quality.

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P is the real output power per phase of the unit (W),

Q_f is the quality factor of the parallel (RLC) resonant load,

C is the effective load capacitance (F),

f is frequency.

The reactive load is balanced so that the resonant frequency f of the island circuit is within the underfrequency and overfrequency trip settings of the EUT and as close to nominal frequency as possible.

When tuning for the current balance in this step with a nonunity output p.f. EUT, there will be an imbalance between the L and C load components to account for the EUT reactive current. The EUT reactive output current shall be measured and algebraically added to the appropriate reactive load component when calculating Q_f.

i) Close switch S1, switch S2, and switch S3, and wait until the EUT produces the desired power level.

j) Adjust R, L, and C until the fundamental frequency current through switch S3 is less than 2% of the rated current of the EUT on a steady-state basis in each phase.[25]

k) Open switch S3 and record the time between the opening of switch S3 and when the EUT ceases to energize the RLC load.

l) The test is to be repeated with the reactive load (either capacitive or inductive) adjusted in 1% increments or alternatively with the reactive power output of the EUT adjusted in 1% increments from 95% to 105% of the initial balanced load component value. If unit shutdown times are still increasing at the 95% or 105% points, additional 1% increments shall be taken until trip times begin decreasing.

m) After reviewing the results of the previous step, the 1% load setting increments that yielded the three longest trip times shall be subjected to two additional test iterations. If the three longest trip times occur at nonconsecutive 1% load setting increments, the additional two iterations shall be run for all load settings in between.

n) Repeat steps d) through m) with the test input source adjusted to limit the EUT output power to 66%. This value is allowed to be between 50% and 95% of rated output power and is intended to evaluate the EUT at less than full power and under the condition where the available output is determined or limited by the input source. If the EUT does not provide this mode of operation, then set the EUT to control the output power to the specified level.

o) Repeat steps d) through m) with the EUT output power set via software or hardware to 33% of its nominal rating with the test input source capable of supplying at least 150% of the maximum input power rating of the EUT over the entire range of EUT input voltages. For units that are incapable of setting or commanding an output power level, the EUT output power shall be limited via the input power source. For units that are incapable of operating at 33%, the EUT shall be tested at the lowest output power the EUT will support. This step is intended to evaluate the EUT at low power and under the condition where the available output is determined or limited by the EUT control setting. If the EUT does not provide this mode of operation, then set the input source to meet the specified output power level.

5.7.1.3 Requirements

Where the EUT requires a separate test input source to conduct this test, that source shall be capable of supplying at least 150% of the maximum input power rating of the EUT over the entire range of EUT input voltages.

[25]Certain anti-islanding algorithms will sufficiently perturb the fundamental frequency current through switch S3 so that the 2% limit cannot be achieved on a continuous basis. Averaging of the rms current over a number of cycles in a manner that captures the quiescent magnitude of this current shall be utilized for determination of matched load during this quiescent period.

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The RLC load shall be tuned so that the fundamental frequency current through switch S3 is less than 2% of the rated current of the unit under test on a steady-state basis in each phase.

The test and measurement equipment shall record each phase current and each phase-to-neutral or phase-to-phase voltage, as appropriate, to determine fundamental frequency real and reactive power flow over the duration of the test. Anti-aliasing filters and sampling frequencies appropriate to the measurement of the fundamental frequency component shall be applied. The minimum measurement accuracy shall be 1% or less of rated EUT nominal output voltage and 1% or less of rated EUT output current.

The equations for Q_f are based upon an ideal parallel RLC circuit. For this reason, noninductive resistors, low loss (high Q) inductors, and capacitors with low effective series resistance and effective series inductance shall be utilized in the test circuit. Real and reactive power should be instrumented in each of the R, L, and C legs of the load so that these parasitic parameters (and parasitics introduced by variacs or autotransformers) are properly accounted for when calculating Q_f. Iron core inductors, if used, shall not exceed a current THD of 2% when operated at nominal voltage. Power ratings of resistors should be conservatively chosen to minimize thermally induced drift in resistance values during the course of the test.

5.7.1.4 Criteria

A test is successful when the DR ceases to energize the test load within the timing requirements of IEEE Std 1547 after switch S3 is opened.

If any of these tests results in islanding for longer than the specified time, the unit fails the test.

The actual trip time for each test shall be recorded.

A single failure of any of these tests is considered a failure of the entire test sequence.

5.7.1.5 Comments

An area EPS source means any source capable of maintaining an island within the recommended voltage and frequency window. An engine-generator with voltage and frequency control and without islanding protection can be considered an area EPS source for the purpose of this test. However, because of the uncertainty associated with the need to sink both real and reactive power from the DR, this test can be performed most conveniently with an area EPS connection, rather than a simulated area EPS.

Harmonic currents flow between the area EPS, the capacitor, and the DR, complicating the situation by making it appear that current is flowing when the fundamental frequency component of current has been reduced to zero. Thus it is important, when adjusting inductive and capacitive reactance, to use instruments that can display only the fundamental frequency component of current and power.

It is often advantageous to adjust the inductance first because that measurement is low in harmonics. The capacitance is added second so that the voltage is stable when the resistance is added. The resistive parallel load is then added and adjusted. Note that this resistance will be in addition to the resistance that will inherently be part of the inductive load.

The maximum recorded trip times may prove useful in area EPS system protection coordination studies and should be presented with other EUT product literature.

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5.7.2 Unintentional islanding test for synchronous generators

5.7.2.1 Purpose

The purpose of this test is to verify that a DR interconnection component or system ceases to energize the area EPS as specified in IEEE Std 1547 when an unintentional island condition is present. This test is for applications where synchronous generators are connected to the EPS. This test determines the trip time for the test conditions specified in 5.7.2.

5.7.2.2 Procedure

a) For a single-phase EUT, the test circuit shall be configured as shown in Figure 3. For a three-phase EUT, the balanced load circuit shown in Figure 3 is to be applied between each phase to neutral for a four-wire configuration or between phases for a three-wire configuration. Switch S1, as shown in Figure 3, shall be gang-operated and three-pole. The grounding of the load and simulated area EPS side of the EUT shall be unaffected by the position of switch S1.

b) Connect the EUT according to the instructions and specifications provided by the manufacturer.

c) Set all source parameters to the nominal operating conditions for the EUT.

d) Set the islanding load circuit in Figure 3 to a real load of 5% (or minimum load as specified by the manufacturer) and unity 1.0 p.f.

e) Record all applicable settings.

f) Adjust the output of the synchronous generator to match the test load in power and p.f. until the fundamental frequency current through switch S1 is less than 2% of the rated current of the unit under test on a steady-state basis in each phase.

NOTE—Certain anti-islanding algorithms will sufficiently perturb the fundamental frequency current through switch S1 so that the 2% limit cannot be achieved on a continuous basis. Averaging of the rms current over a number of cycles in a manner that captures the quiescent magnitude of this current shall be utilized for determination of matched load during this quiescent period.[26]

g) Open switch S1 and record the time between the opening of switch S1 and when the EUT ceases to energize the load.

h) Repeat test four times for a total of five times.

i) Repeat steps d) through h) for the following combinations:

— Maximum real load at unity p.f.

— Maximum real load at rated p.f. lagging

— Maximum real load at rated p.f. leading

5.7.2.3 Requirements

The test and measurement equipment shall record each phase current and each phase-to-neutral or phase-to-phase voltage, as appropriate; to determine fundamental frequency real and reactive power flow over the duration of the test. Anti-aliasing filters and sampling frequencies appropriate to the measurement of the fundamental frequency component shall be applied. The minimum measurement accuracy shall be 1% of rated EUT nominal output voltage and 1% of rated EUT output current.

[26]Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement this standard.

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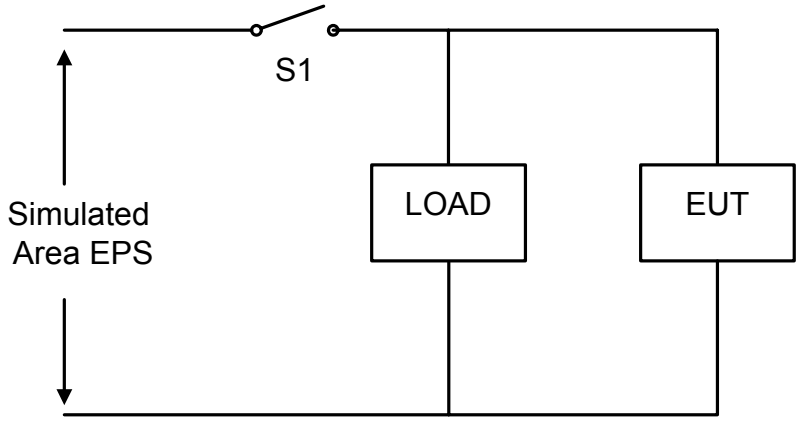


Figure 3—Unintentional islanding test configuration for synchronous generators

5.7.2.4 Criteria

A test is successful when the DR ceases to energize the test load within the timing requirements of IEEE Std 1547 after switch S1 is opened.

If any of these tests results in islanding for longer than the specified time, the unit fails the test.

The actual trip time for each test shall be recorded.

A single failure of any of these tests is considered a failure of the entire test sequence.

5.7.2.5 Comments

An area EPS source means any source capable of maintaining an island within the recommended voltage and frequency window. An engine-generator with voltage and frequency control and without islanding protection can be considered an area EPS source for the purpose of this test. However, because of the uncertainty associated with the need to sink both real and reactive power from the DR, this test can be performed most conveniently with an area EPS connection, rather than a simulated area EPS.

The maximum recorded trip times may prove useful in area EPS system protection coordination studies and should be presented with other EUT product literature.

A grid intertied synchronous generator will typically regulate real power (in kilowatts) irrespective of grid frequency, and it will regulate reactive power (in kilovars) or p.f. regardless of voltage level on the grid. The control systems inherent in synchronous machines may possibly maintain an unintentional island, but this condition depends on the load applied being closely matched to the synchronous generator output.

Note also that the change in kilowatts requires a change in the fuel rate to the engine, and the change in the kilovar load requires a change in the excitation rate in the synchronous generator. Because the excitation rate can be changed much faster than the fuel rate, the protection scheme for unintentional island detection should consider the characteristics required for proper operation in compliance with the requirements of IEEE Std 1547.

The synchronous machine can maintain ac output when islanded, but the frequency of the output is not related to the inductive and capacitive nature of the loads on the machine as it is in some inverter-based machines. Furthermore, the test load of Figure 3 needs reactive elements to achieve the p.f.s as required for

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step i) of the procedure in 5.7.2.2. Consequently, the testing procedure for unintentional island testing for synchronous machines is different from the procedure for other DR equipment.

It is possible that the synchronous machine may operate differently at one of its control limits from the way it operates at others. The test procedure for synchronous machines verifies that the unintentional islanding protection of the synchronous machine is effective over the operating range of the equipment for both the fuel and the excitation control.

5.8 Reverse power (for unintentional islanding)

IEEE Std 1547 requires DR units to cease to energize the area EPS during unintentional islanding conditions. One of the ways in which this requirement may be met is with reverse-power protection. The DR installation may contain reverse or minimum import power-flow protection, sensed between the point of DR connection and the PCC, which will disconnect or isolate the DR if power flow from the area EPS to the local EPS reverses or falls below a set threshold.

5.8.1 Reverse-power magnitude test

5.8.1.1 Purpose

This test is performed to characterize the accuracy of the reverse-power protection magnitude setting(s) of the EUT. The reverse-power protection accuracy of the EUT shall be specified prior to beginning the tests.

5.8.1.2 Procedures

a) Connect EUT according to the instructions and specifications provided by the manufacturer.

b) Set the source and DR voltages and the DR current(s) to the nominal operating conditions for the EUT.

c) Set (or verify) all EUT parameters to the nominal operating settings (refer to Appendix A for additional detail).

d) Record applicable settings.

e) Referring to the reverse-power magnitude test described in Annex A, adjust the current to starting point I_b. Initiate a phase-angle step function from 0° to 180°. The current shall be held at this magnitude and phase angle for period t_h.[27] At the end of this period, initiate the current ramp function.

f) Record the current magnitude when the EUT trips.[28]

g) Return the current to nominal magnitude I_N and phase angle $\theta = 0°$ (and reset the EUT as necessary).

h) Repeat steps e) through g) four times for a total of five tests.

i) For multiphase systems, repeat steps e) through h) for each phase individually and all phases simultaneously.

5.8.1.3 Criteria

The EUT is expected to trip within the specified accuracy for all tests. The test results may be used to characterize or verify the protection level accuracy relative to manufacturer specifications, interconnection standards, periodic verification of calibration, and so on.

[27] See Footnote 8.

[28] Because the source voltage is 1.0 per unit and the phase relationship between the source voltage and current is 180°, the reverse-power trip magnitude will be directly proportional to the current magnitude at the trip point.

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5.8.2 Reverse-power time test

5.8.2.1 Purpose

This test is performed to characterize the accuracy of the reverse-power time-delay setting(s) of the EUT. The reverse-power protection time-delay accuracy of the EUT shall be specified prior to beginning the tests.

5.8.2.2 Procedures

a) Connect the EUT according to the instructions and specifications provided by the manufacturer.
b) Set the source and DR voltages and the DR current(s) to the nominal operating conditions for the EUT.
c) Set (or verify) all EUT parameters to the nominal operating settings (refer to Annex A for additional detail).
d) Record applicable settings.
e) Referring to the reverse-power time test described in Annex A, adjust the current to starting point I_b. Initiate a phase-angle step function from 0° to 180°. The current shall be held at this magnitude and phase angle for period t_h.[29] At the end of this period, initiate the current step function.
f) Record the time between the initiation of the step function and the occurrence of the EUT's expected response.
g) Return the current to nominal magnitude I_N and phase angle $\theta = 0°$ (and reset the EUT as necessary).
h) Repeat steps e) through g) four times for a total of five tests.
i) For multiphase systems, repeat steps e) through h) for each phase individually and all phases simultaneously.

5.8.2.3 Criteria

The EUT is expected to respond within the specified accuracy for all tests. The test results may be used to characterize or verify the protection level accuracy relative to manufacturer specifications, interconnection standards, periodic verification of calibration, and so on.

5.9 Open phase[30]

5.9.1 Purpose

The purpose of this test is to verify that the ICS ceases to energize the area EPS upon loss of an individual phase at the PCC or at the point of DR connection.

5.9.2 Procedure

Single-phase two-wire ICSs shall be subjected to steps a) through e) only. Multiphase and single-phase three-wire ICSs shall be subjected to steps a) through f). If the EUT requires the use of an isolation transformer, it will be tested with the isolation transformer.

a) Connect the EUT in accordance with the instructions and specifications provided by the manufacturer through individual phase conductor disconnects on each ungrounded phase to a simulated area EPS.
b) Set DR and simulated area EPS source parameters to the nominal operating conditions for the EUT.

[29] See Footnote 8.

[30] This test is intended to demonstrate compliance with the individual phase requirement of the cease-to-energize functionality test of IEEE Std 1547. It is noted that loss of a phase is a common area EPS occurrence.

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c) Open one phase conductor disconnect while the EUT is operating at the greater of
   — 5% of rated output current or
   — The EUT's minimum output current.
d) Record the clearing time.
e) Repeat steps c) through d) four times for a total of five tests.[31]
f) Repeat steps c) through e) for all remaining phase conductor disconnects.

5.9.3 Requirements

If used, the simulated area EPS shall meet the requirements of 4.6.1. The measurement system shall meet the requirements of 4.6.2.

5.9.4 Criteria

After the disconnect is opened, the EUT shall cease to energize all output terminals connected to the simulated area EPS within the timing requirement of IEEE Std 1547 for unintentional islanding.

5.9.5 Comments

CAUTION

With multiphase EUT, it is advisable to predetermine if opening one phase at a time could cause a ferroresonant overvoltage. Where the EUT is connected to the simulated area EPS through an isolation transformer, opening one or two phases between the transformer and the simulated area EPS, and the subsequent cease-to-energize response by the EUT, will result in the transformer being energized by only one or two phases, one of several necessary conditions for ferroresonance. Ferroresonant overvoltages can be several times greater than nominal voltage and should be avoided.

5.10 Reconnect following abnormal condition disconnect

5.10.1 Purpose

The purpose of this test is to verify the functionality of the DR interconnection component or system reconnect timer, which delays the DR reconnection to the area EPS following a trip event.

5.10.2 Procedure

a) Connect the EUT according to the instructions and specifications provided by the manufacturer to a simulated area EPS. Set all input source parameters and EPS parameters to the nominal operating conditions for the EUT.
b) With the EUT operating inside the normal EPS voltage and frequency operating range of the unit, step-change the simulated area EPS voltage to 5% beyond one of the voltage trip limits.[32] Confirm that the EUT ceases to energize the simulated area EPS.
c) Adjust the voltage so that it is beyond the reconnect voltage by twice the manufacturer's stated tolerance. The simulated area EPS voltage source shall maintain the abnormal voltage for two times the reconnect time delay. Verify that the EUT does not reenergize the simulated area EPS.

[31]The reconnect time may be adjusted for testing convenience. The reconnect time test is given in 5.10.

[32]A voltage trip was picked for illustration. The protective functions listed in step h) can be tested in any order.

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d) Step-change or change the voltage to be within 1 s, back into the product's nominal operating voltage range. Measure the reconnect time between when nominal operating voltage is restored and when the product initiates the exportation of current.

e) The EUT shall not reconnect to the simulated area EPS source for at least the manufacturer's reconnect time delay within the manufacturer's stated tolerance.

f) The EUT shall not reconnect to the simulated area EPS source unless the area EPS voltage and frequency have been restored to the voltage and frequency ranges specified in IEEE Std 1547 and have remained within those ranges for the full specified reconnect time period.

g) To verify that the timer resets for additional voltage excursions within the reconnect time, retest with an abnormal voltage step-change event that is introduced during the reconnect countdown period. While the unit is counting down to reconnect, step the voltage to a value 5% outside of the manufacturer's specified normal operating voltage for the trip time setting plus twice the manufacturer's stated timer accuracy, and then return to the normal operating voltage. The unit shall restart its reconnect timer and not reconnect until the grid voltage has been within the specified range for the specified reconnect time.

h) The tests shall be conducted to confirm that both voltage and frequency are within the requirements of IEEE Std 1547.

i) The tests shall be conducted for voltage and frequency, both over and under.

5.10.3 Requirements

If used, the simulated area EPS shall meet the requirements of 4.6.1. The measurement system shall meet the requirements of 4.6.2.

5.10.4 Criteria

The reconnect time delay shall meet the requirements of IEEE Std 1547 within the manufacturer's stated accuracy.

5.10.5 Comments

This test may be performed in conjunction with the overvoltage, undervoltage, overfrequency, and underfrequency tests.

5.11 Harmonics

The purpose of this test is to measure the individual current harmonics and total rated-current distortion (TRD) of the DR interconnection component or system under normal operating conditions. The results shall comply with the requirements of IEEE Std 1547. Self-excited induction generators shall be tested using the procedure for synchronous generators.

5.11.1 Harmonics test for inverters

This test is for an inverter-based ICS. If the EUT requires the use of an isolation transformer, it will be tested with the isolation transformer. The harmonics measurement point will be at the isolation transformer connection to the area EPS source.

A resistive load equal to the output power of the EUT may be placed between the EUT and the simulated area EPS.

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5.11.1.1 Procedure

a) Connect the EUT according to the instructions and specifications provided by the manufacturer to a simulated area EPS. Set all input source parameters and EPS parameters to the nominal operating conditions for the EUT.

b) Operate the EUT at 33% of output rated current.

c) With the EUT operating at normal operating temperature and inside the normal EPS voltage and frequency operating range of the unit, for each phase measure the individual current harmonics and output current TRD through the first 40 harmonics. When the EUT has a harmonic spectrum that is varying in time, the harmonic calculation shall use an averaging window of sufficient length to accurately represent the average level of harmonic current.

d) Repeat for an output load current I_L of 66% and at a level as close to 100% of the rated output current as practical. Operating power levels in this procedure have a tolerance of ± 5%.

5.11.1.2 Requirements

The measurement equipment shall be capable of capturing and processing the data in a manner to ensure that the results are representative of the average TRD over a period of time that is a multiple of any periodic or repetitive output waveform transient.

The DR shall be operated in parallel with a predominantly inductive voltage source with a short-circuit current capacity I_{SC} of not less than 20 times the DR rated output current at fundamental frequency as specified in IEEE Std 1547.

When an EUT's input power source voltage and frequency parameters affect the output power quality, the tests are to be performed with the least favorable input parameters.

The simulated area EPS shall not exhibit dependence upon the product being tested or use algorithms to cancel or correct the simulated area EPS waveform in response to the harmonics generated by the product being tested.

5.11.1.3 Criteria

The individual current harmonics and TRD shall not exceed the limits specified in IEEE Std 1547.

For multiphase EUT, each of the phases shall comply with the specified limits.

5.11.1.4 Comments

Steps may be necessary to ensure that measured harmonics exceeding the allowable levels in IEEE Std 1547 are not caused by characteristics of the simulated area EPS.

5.11.2 Harmonics test for synchronous generators

Synchronous generator harmonics can be verified either by the voltage harmonics test presented in this subclause or by the current harmonics test in 5.11.3.

5.11.2.1 Procedure

a) Connect the synchronous generator EUT to a rotating source capable of operating the machine at a steady-state frequency within ± 0.25% of nominal conditions. Set the voltage and frequency to the nominal operating levels for the facility under question.

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b) Connect a resistive load bank to the synchronous generator. Verify that the load bank provides a balanced resistive load to the synchronous generator. The load bank shall be capable of operating continuously at the full load rating of the EUT.

c) With the EUT operating at nominal voltage and frequency and at full load, for each phase measure the individual voltage harmonics through the first 40 harmonics. If the EUT has a harmonic spectrum that is varying in time, the harmonic calculation shall use an averaging window of sufficient length to accurately represent the average level of harmonic voltage.

d) Measure harmonics from line to neutral on machines operated as three-phase/four-wire sources and line to line for machines operated as three-phase/three-wire sources.

5.11.2.2 Requirements

The measurement equipment shall be capable of capturing and processing the data in a manner to ensure that the results are representative of the average THD over a period of time that is a multiple of any periodic or repetitive output waveform transient.

5.11.2.3 Criteria

The test shall demonstrate that the individual harmonic voltage levels and the total harmonic voltage produced by the generator set are within the requirements of IEEE Std 1547.

5.11.2.4 Comments

The synchronous generator is tested at 100% of the full load rating because this is considered the worse-case condition.

5.11.3 Harmonics test for induction generators

5.11.3.1 Procedure

a) Connect the EUT according to the instructions and specifications provided by the manufacturer to a simulated area EPS. Set all input source parameters and EPS parameters to the nominal operating conditions for the EUT.

b) Operate the EUT at 100% of the rated output current.

c) With the EUT operating at nominal voltage and frequency and at full load, for each phase measure the individual current harmonics and output current TRD through the first 40 harmonics. When the EUT has a harmonic spectrum that is varying in time, the harmonic calculation shall use an averaging window of sufficient length to accurately represent the average level of harmonic current.

5.11.3.2 Requirements

The measurement equipment shall be capable of capturing and processing the data in a manner to ensure that the results are representative of the average TRD over a period of time that is a multiple of any periodic or repetitive output waveform transient.

The DR shall be operated in parallel with a predominantly inductive voltage source with a short-circuit current capacity I_{SC} of not less than 20 times the DR rated output current at fundamental frequency.

The simulated area EPS shall not exhibit dependence upon the product being tested or use algorithms to cancel or correct the simulated area EPS waveform in response to the harmonics generated by the product being tested.

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5.11.3.3 Criteria

The individual current harmonics and TRD shall not exceed the limits specified in IEEE Std 1547.

For a multiphase unit, each of the phases shall comply with the specified limits.

5.11.3.4 Comments

Steps may be necessary to ensure that measured harmonics exceeding the allowable levels in IEEE Std 1547 are not caused by characteristics of the simulated area EPS.

A resistive load equal to the output power of the EUT may be placed between the EUT and the simulated area EPS.

The induction generator is tested at 100% of the full load rating because this is considered the worse-case condition.

5.12 Flicker

Given the site dependence of flicker, there are no type tests available to determine if a given DR will meet the flicker requirements. The synchronization test procedure provided in 5.4.3 is intended to characterize the maximum current flow to or from the DR under a nonfaulted condition. The results of that test can be used, along with local line impedance information, to determine if a DR might present a flicker nuisance (i.e., in a "flicker calc"). Mitigating action must be taken if measurements show that DR-induced voltage fluctuations exceed those allowed in IEEE Std 1547.

6. Production tests

Production tests verify the operability of every unit of interconnect equipment manufactured for customer use. These tests assume that the equipment has met the applicable requirements of Clause 5 and may be conducted as a factory test or performed as part of a commissioning test. Tests are performed to verify manufacturers' settings rather than specific requirements in IEEE Std 1547 since that standard allows adjustability of set points and it is of value to have the unit factory set and tested at specific settings. If any tests from Clause 5 have not been previously completed, they may be included in the production test regimen.

For any of the tests to be conducted in this clause, function settings need be recorded only once. The report shall provide a list of final settings.

At the discretion of the manufacturers, production tests may use the corresponding tests from Clause 5 in place of the procedures listed in this clause.

For the purposes of this standard, multiphase ICSs include single-phase three-wire ICSs.

ICSs with adjustable set points shall be tested at a single set of set points as specified by the manufacturer. Production tests shall include the following as applicable:

— Response to abnormal voltage (see 6.1)

— Response to abnormal frequency (see 6.2)

— Synchronization (see 6.3)

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6.1 Response to abnormal voltage

6.1.1 Purpose

The purpose of this test is to verify that the DR interconnection component or system responds to abnormal voltage conditions as required. Trip setting shall be as specified by the manufacturer.

6.1.2 Procedure

a) Connect the EUT according to the instructions and specifications provided by the manufacturer.
b) Verify all simulated area EPS parameters are at nominal operating conditions for the EUT.
c) Set the EUT to the manufacturer's trip voltage and time settings as applicable. Verify that all of the other EUT settings are at their factory set points.
d) Record applicable settings.
e) Select one of the undervoltage or overvoltage protective functions for test.[33]
f) Adjust the voltage to a point at least twice the manufacturer's stated accuracy outside the abnormal voltage trip setting.[34] Record the rms voltage magnitude and trip time.
g) For multiphase units perform this test on each phase, adjusting one phase at a time.
h) Repeat steps e) through g) for all of the undervoltage and overvoltage protective functions.

6.1.3 Criteria

The test results are acceptable if the EUT trips in the ranges specified by the manufacturer.

6.2 Response to abnormal frequency

6.2.1 Purpose

The purpose of this test is to verify that the DR interconnection component or system responds to abnormal frequency conditions as required. Trip setting shall be as specified by the manufacturer.

6.2.2 Procedure

a) Connect the EUT according to the instructions and specifications provided by the manufacturer.
b) Verify all simulated area EPS parameters are at nominal operating conditions for the EUT.
c) Set the EUT to the manufacturer's trip frequency and time settings as applicable. Verify that all of the other EUT settings are at their factory set points.
d) Record applicable settings.
e) Select one of the underfrequency or overfrequency protective functions for test.[35]
f) Adjust the frequency to a point at least twice the manufacturer's stated accuracy outside the abnormal frequency trip setting.[36] Record the frequency and trip time.
g) Repeat steps e) through f) for all of the underfrequency and overfrequency protective functions.

[33]The EUT may have one or more undervoltage protective functions and/or one or more overvoltage protective functions.

[34]The test shall be designed so that the EUT trips due to the selected abnormal voltage protective function and not due to another protective function of the EUT. The test design should include selection of appropriate voltage level. The trip magnitude and time settings may be verified using a single test waveform in one test or using different test waveforms in two separate tests.

[35]The EUT may have one or more underfrequency protective functions and/or one or more overfrequency protective functions.

[36]The test shall be designed so that the EUT trips due to the selected abnormal frequency protective function and not due to another protective function of the EUT. The test design should include selection of appropriate frequency level. The trip magnitude and time settings may be verified using a single test waveform in one test or using different test waveforms in two separate tests.

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6.2.3 Criteria

The test results are acceptable if the EUT trips in the ranges specified by the manufacturer.

6.3 Synchronization

The purpose of this test is to verify that the DR interconnection component or system will connect the DR only when the voltage, frequency, and phase-angle differences are acceptable or will not induce flicker on the area EPS. Equipment that is using the startup (in-rush) current method is exempt from this production test. Two procedures are offered: one for equipment that does not include provisions for switching off the synchronizing function and another for equipment that can be manipulated to control the synchronization process.

Settings shall be as specified by the manufacturer and shall be within the requirements of IEEE Std 1547.

6.3.1 Synchronization production test

6.3.1.1 Procedure

a) Install and adjust the EUT per the manufacturer's recommendations and specifications.
b) Connect the test equipment to monitor the paralleling device close command, the phase-angle relationship between EUT output and area EPS sources, the frequency difference, and voltage difference.
c) Set the simulated area EPS source to operate at nominal voltage and frequency. Record applicable settings.
d) Verify that the EUT is operating properly when connected to the simulated area EPS.
e) Disconnect the area EPS from the EUT.
f) Enable all monitoring equipment. Reapply the area EPS and record all required parameters (i.e., voltage, frequency, and phase-angle differences) during the paralleling operation.

6.3.1.2 Criteria

The test results are acceptable if the EUT operates in the ranges specified by the manufacturer and within the requirements of IEEE Std 1547.

6.3.2 Optional test for equipment with synchronizing disable function

6.3.2.1 Procedure

a) Connect the EUT according to the instructions and specifications provided by the manufacturer.
b) Set the parameters of the two sources to nominal operating conditions, but with the voltage and frequency differences outside of the acceptable range for synchronism.
c) Set the voltage difference, frequency difference, and phase-angle difference of the EUT as specified by the manufacturer. Verify that all of the other EUT settings are at their factory set points.
d) Record applicable settings.
e) Verify synchronizing performance with respect to frequency difference
    1) Adjust the voltage difference of the sources to within the acceptable range for synchronism.
    2) Adjust the frequency difference to a point at least twice the manufacturer's stated accuracy outside the acceptable frequency difference.
    3) Wait for at least two passes through synchronism.

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4) Step the frequency difference to a point at least twice the manufacturer's stated accuracy within the acceptable range for synchronism.
5) Record the voltage, frequency, and phase-angle differences at the time of DR connection (for complete interconnect systems) or at the initiation of the EUT output device signal (for ICS components).

f) Set the parameters of the two sources to nominal operating conditions, but with the voltage and frequency differences outside of the acceptable range for synchronism.
g) Verify synchronizing performance with respect to voltage difference
1) Adjust frequency difference of the sources to within the acceptable range for synchronism.
2) Adjust the voltage difference to a point at least twice the manufacturer's stated accuracy outside the acceptable voltage difference. Wait for two passes through synchronism.
3) Step the voltage to a point at least twice the manufacturer's stated accuracy within the acceptable range for synchronism.
4) Record the voltage, frequency, and phase-angle differences at the time of DR connection (for complete interconnect systems) or at the initiation of the EUT output device signal (for ICS components).

6.3.2.2 Criteria

The test results are acceptable if the EUT operates in the ranges specified by the manufacturer and within the requirements of IEEE Std 1547.

6.4 Documentation

The production test documentation shall include the manufacturer's model number, serial number, functional software and firmware versions (where applicable), testing date, test settings, manufacturer's stated accuracies, and production test results. This information shall be provided with the equipment.

7. Commissioning test

7.1 General

The commissioning test shall be conducted after the ICS is installed and is ready for operation. An individual qualified in testing protective equipment (e.g., professional engineer, factory-certified technician, licensed electrician with experience in testing protective equipment) should perform or directly supervise commissioning tests. Where the operation of the ICS is integrated with and dependent upon the operation of the area EPS, the commissioning test should be coordinated with and agreed to by the area EPS operator. The area EPS operator may require that he or she witness the commissioning test as described in this clause or may require documentation from the equipment owner describing which tests were performed and their results.

A commissioning test report shall be produced and shall contain the results of all tests and a listing of the final ICS settings. Once complete and accepted, the commissioning test will not have to be repeated.

For the purposes of this standard, multiphase ICSs include single-phase three-wire ICSs.

7.1.1 Purpose

The commissioning test shall be performed to verify that the completed and installed ICS meets the requirements of IEEE Std 1547.

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7.1.2 Procedure

All tests shall be performed based on written procedures. Test procedures are commonly provided by equipment manufacturers or system integrators and approved by the equipment owner and area EPS operator. The written commissioning test procedure shall include the following:

— Verification and inspections (see 7.2)
— Field-conducted type and production tests (see 7.3)
— Unintentional islanding functionality test (see 7.4)
— Cease-to-energize functionality test (see 7.5)
— Revised settings (see 7.6)

7.2 Verifications and inspections

a) Confirm that the equipment and its installation comply with the interconnection installation evaluation in IEEE Std 1547.
b) Record applicable settings.
c) Visually inspect system grounding implementation according to the requirements of IEEE Std 1547.
d) Visually inspect and verify operability of isolation device, if required.
e) Verify that polarities, burdens, and ratios of field-wired CTs and VTs are correct and in accordance with the design.
f) Through visual inspection, continuity test, or insulation resistance test, verify that field-installed power and control wiring is in compliance with drawings and manufacturer requirements.
g) Interconnection protective devices that have not previously been tested as part of the ICS with their associated interrupting devices (e.g., contactor or circuit breaker) shall be tested to verify that the associated interrupting devices open when the protective devices operate. Interlocking circuits between protective and interrupting devices shall be similarly tested unless they have been tested during production tests.
h) On three-phase systems, check the phase rotation of both area EPS and DR and verify that they are compatible as installed.
i) Verify functionality of all monitoring provisions required by IEEE Std 1547.

7.3 Field-conducted type and production tests

Determine which type and production tests as required in Clause 5 and Clause 6 have not been conducted and if any type testing is required due to changes in software, firmware, or hardware. Conduct these tests in accordance with the procedures given in Clause 5 and Clause 6.

7.4 Unintentional islanding functionality test

7.4.1 Reverse-power or minimum power test

If a reverse-power or minimum power function is used as a method to prevent unintentional islanding, it shall be tested by signal injection test methods, by adjusting the DR output and local loads, or by other suitable methods to verify that the function is met and that the DR ceases to energize.

7.4.2 Non-islanding functionality test

An ICS certified to 5.7 is considered non-islanding and need be tested only to 7.5.

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7.4.3 Other unintentional islanding test methods

If neither 7.4.1 nor 7.4.2 is applicable, the ICS shall be tested in accordance with procedures provided by the manufacturer or system integrator.[37]

7.5 Cease-to-energize functionality test

The cease-to-energize functionality test verifies that the load-interrupting device operates or the equipment ceases to energize the output terminals that are connected on all phases to the area EPS when commanded by the ICS and does not restart/reconnect for the required time delay.

An ICS that meets the requirements of 5.9 and 7.4.1 satisfies the requirements of this subclause.

The following procedure may be adjusted dependent on an agreement between the area EPS authority and the system installer.

7.5.1 Procedure

Single-phase two-wire ICSs need to be subjected to steps a) through e) only. Multiphase and single-phase three-wire ICSs that satisfy the requirements of 5.9 need to be subjected to steps a) through e) only.

a) Operate the DR interconnected with the area EPS at an output power level available and convenient[38] at the time of testing.

b) Disconnect all ungrounded phases from the area EPS simultaneously using a device other than the interconnection component that provides the cease-to-energize function.

c) Verify that the ICS ceases to energize the output terminals connected to the area EPS.

d) After a convenient period, reclose the selected disconnect.

e) Verify that the ICS does not reenergize output terminals connected to the area EPS for the required restart/reconnect time delay.

CAUTION

With multiphase EUT, it is advisable to predetermine if opening one phase at a time could cause a ferroresonant overvoltage. Where the EUT is connected to the simulated area EPS through an isolation transformer, opening one or two phases between the transformer and the simulated area EPS, and the subsequent cease-to-energize response by the EUT, will result in the transformer being energized by only one or two phases, one of several necessary conditions for ferroresonance. Ferroresonant overvoltages can be several times greater than nominal voltage and should be avoided.

f) With the DR operating, disconnect one phase conductor from the area EPS using a device other than the interconnection component that provides the cease-to-energize function.

g) Verify that the ICS ceases to energize the output terminals connected to the area EPS.

h) After a convenient period, reclose the selected disconnect.

i) Repeat steps f) through h) for the remaining phase conductors.

[37] Some examples by which this requirement may be met are as follows:

— The DR aggregate capacity is less than one-third of the minimum load of the local EPS.

— The DR contains other non-islanding means, e.g., a transfer trip or governor and excitation controls that maintain constant power and constant p.f.

[38] This test is not intended to be conducted at any specific power level and recognizes that DR output may vary with environmental conditions (e.g., solar photovoltaic, wind, renewable fuels).

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7.6 Revised settings

Settings affecting ICS response (e.g., response to abnormal voltage or frequency) that have been changed after factory testing shall be verified. Verification may be performed by any of the following methods:

- Using signals injected into the voltage and current sense circuits
- Applying waveforms
- A test connection using a simulated area EPS
- Varying the set points to show that the device trips at the measured (actual) area EPS parameter
- Observing displayed settings
- Confirming jumper or other physical settings
- Using other methods as prescribed by a manufacturer's written procedure

8. Periodic interconnection tests

At the time of commissioning, a written periodic interconnection test procedure should be agreed upon by the equipment owner and the area EPS operator. Periodic interconnection test procedures are typically provided by the equipment manufacturer. The procedure shall describe a test process that will verify that all interconnection-related protective functions and associated batteries are functional, but it need not replicate the test procedures in Clause 5, Clause 6, and Clause 7. The interval between periodic tests shall be specified by the manufacturer, system integrator, or the authority having jurisdiction over the DR interconnection. Written test reports or a log for inspection shall be maintained.

If changes are made to functional software or firmware of the ICS and if such software or firmware has not been previously type-tested, then perform the applicable tests in Clause 5, Clause 6, and Clause 7. Also, if a hardware component of the ICS has been modified in the field, replaced, or repaired with parts different from the tested configuration and if such hardware has not been previously type-tested, then perform the applicable tests in Clause 5, Clause 6, and Clause 7. If such software, firmware, or hardware has been previously type-tested or if settings have been changed, then conduct the tests in Clause 6 and Clause 7 applicable to the changes made.

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Annex A

(normative)

Test signals

The test signals in this annex are generic functions that can be used for ramp or step tests to determine a particular set point. These are used in several of the tests in Clause 5 including undervoltage, overvoltage, underfrequency, overfrequency, synchronization magnitude difference, synchronization frequency difference, and synchronization phase difference. Note that the examples show positive ramp or step for high-magnitude parameter excursions. The ramp or step will be negative for low-magnitude parameter excursions (e.g., undervoltage, underfrequency).

A.1 Magnitude test (ramp function)—general

The test signal described in this subclause is used to characterize the accuracy of the magnitude setting for relevant protection parameters.

Vary the PUT (e.g., voltage or frequency) according to the magnitude ramp function defined in this subclause. Only the PUT shall be varied. Therefore, all other parameters shall be held at nominal values. The ramp shall take the form of Equation (A.1).

$$p(t) = m(t - t_0) + P_b \tag{A.1}$$

where

p is the PUT,
m is the slope of the ramp function,
t is the time of the response (s),
t_0 is the time at the beginning of the event,
P_b is the starting point of the ramp function (in units of the PUT).[39]

The slope m is defined by Equation (A.2). The slope m is positive for overvoltage and overfrequency testing and negative for undervoltage and underfrequency testing.

$$m = \frac{(0.5 \times a)}{(2 \times z)} \tag{A.2}$$

where

z is the time-delay setting (s) for the PUT plus the manufacturer's stated detection time (s),
a is the manufacturer's stated accuracy of the PUT.

Figure A.1 illustrates the terms and concepts described after the figure.

[39]The starting point P_b shall be within 10% of, but not exceed, the trip point magnitude.

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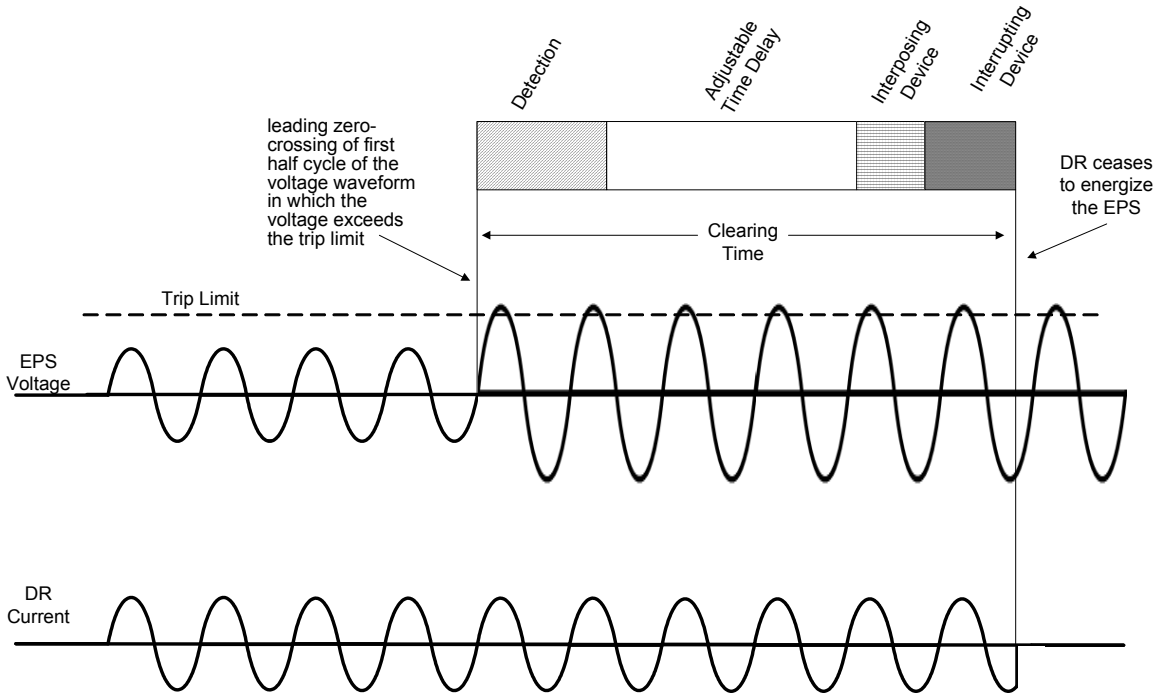


Figure A.1—Illustrative example of detection and clearing time

detection time: The minimum length of time from the inception of the abnormal condition to the change in state of the ICS's output dedicated to controlling the interrupting device. This is often on the order of 8 to 16 ms. *Syn:* processing time.

adjustable time delay: The intentional time added to the detection time in order to provide the desired clearing time. This may be adjustable from zero to several seconds.

interposing device time: The delay introduced in systems that include an auxiliary interface device, often an electromechanical hinged-armature relay. This is often on the order of 8 to 16 ms.

interrupting device time: Typically, the solenoid-initiated (trip) movement of the spring-loaded mechanism of the main current-carrying contacts of a circuit breaker plus any power arc interruption time (nonvacuum) that is dependant on the time to the next current zero-crossing. Interrupting device time varies widely from one half cycle to several cycles. For inverters, this would be the time needed to stop the bridge firing function and to cease energy outflow, which may be essentially zero time.

clearing time: The sum of the detection time, the adjustable time delay, the interposing devices time (if used), and the interrupting device time.

trip time: The interval that begins at the leading zero-crossing of the first half cycle of the voltage waveform in which the measured parameter (e.g., frequency, voltage, power) exceeds the trip limit and ends when the EUT responds as required. The trip time includes any time delay(s) used in conjunction with the ICS's protection functions. Depending on the EUT, the trip time can be a component of or equivalent to the clearing time.

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Figure A.2 is a graphical representation of a ramp function used for a high-magnitude parameter test of the PUT (e.g., overvoltage, overfrequency). In the figure, p represents the magnitude of the PUT, t represents time, P_N is the nominal condition of the PUT, P_T is the trip magnitude of the PUT, t_0 is the start time of the ramp, and t_s is the start of the hold time[40] t_h for the test signal at starting point P_b.

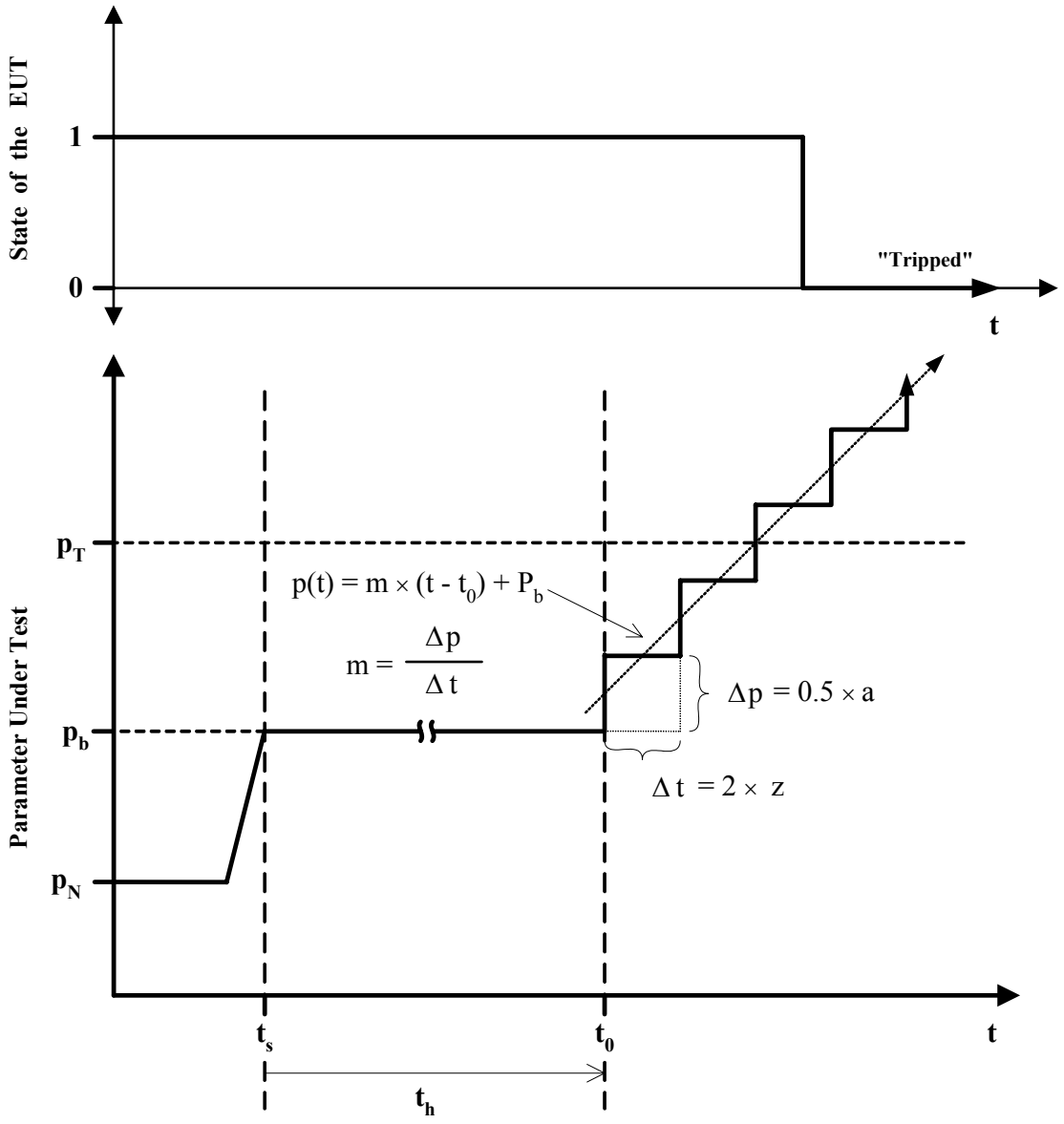


Figure A.2—Graphical representation of magnitude test using ramp function for PUT

When the ramp function conflicts with a design characteristic or settings of the EUT, an alternative method that is agreeable to the manufacturer and the testing agency may be used.

[40]The hold time t_h is at least two times the time-delay setting of the PUT. This number may be adjusted to avoid conflict with other trip points.

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A.2 Time test (step function)—general

The test signal described in this subclause is used to characterize the accuracy of the time-delay setting for relevant protection parameters.

Vary the PUT according to the magnitude step function defined herein. Only the PUT shall be varied. Therefore, all other parameters shall be held at nominal values. The time test signal shall take the form described in Equation (A.3).

$$p(t) = A \times u(t - t_i) + P_b \quad \text{(A.3)}$$

where

p is the magnitude of the PUT,
t is time (s),
A is a scaling factor,[41]
$u(t)$ is the unit step function,[42]
P_b is the starting point of the step function (in units of the PUT).[43]

Figure A.3 is a graphical representation of the function used for a time test of the PUT. In the figure, p represents the magnitude of the PUT, t represents time, t_t is the trip time, P_N is the nominal condition for the PUT, P_T is the trip magnitude of the PUT, P_U is the final value of the step function, t_i is the start of the step function, t_0 is the start time used for calculating the trip time, t_r is the rise time of the test signal from $(t_0 - t_i)$,[44] and t_s is the start of the hold time[45] t_h for the test signal at starting point P_b.

When the step function conflicts with a design characteristic or settings of the EUT, an alternative method that is agreeable to the manufacturer and the testing agency may be used.

A.3 Reverse-power magnitude test (ramp function)

The test signal described in this subclause is used to characterize the accuracy of the reverse-power magnitude protection setting.

Vary the current test signals (i.e., magnitude and phase angle) according to the ramp function defined in this subclause. Only the current test signals shall be varied. Therefore, the voltage test signal shall be held at nominal values. The current test signal magnitude i and phase angle θ shall take the form described in Equation (A.4) and Equation (A.6).

$$i(t) = m(t - t_0) + I_b \quad \text{(A.4)}$$

where

i is the current magnitude,
m is the slope of the ramp function,
t is time (s),

[41]The scaling factor A shall be chosen so that P_U is at least 110% (90% for under value tests) of P_T. Exception: for frequency tests, the scaling factor A shall be chosen so that P_U is at least 101% (99% for under value tests) of P_T.
[42]$u = 0$ for $t < 0$ and $u = 1$ for $t \geq 0$.
[43]See Footnote 39.
[44]The rise time t_r shall be less than the larger of 1 cycle or 1% of the time-delay setting of the PUT.
[45]See Footnote 40.

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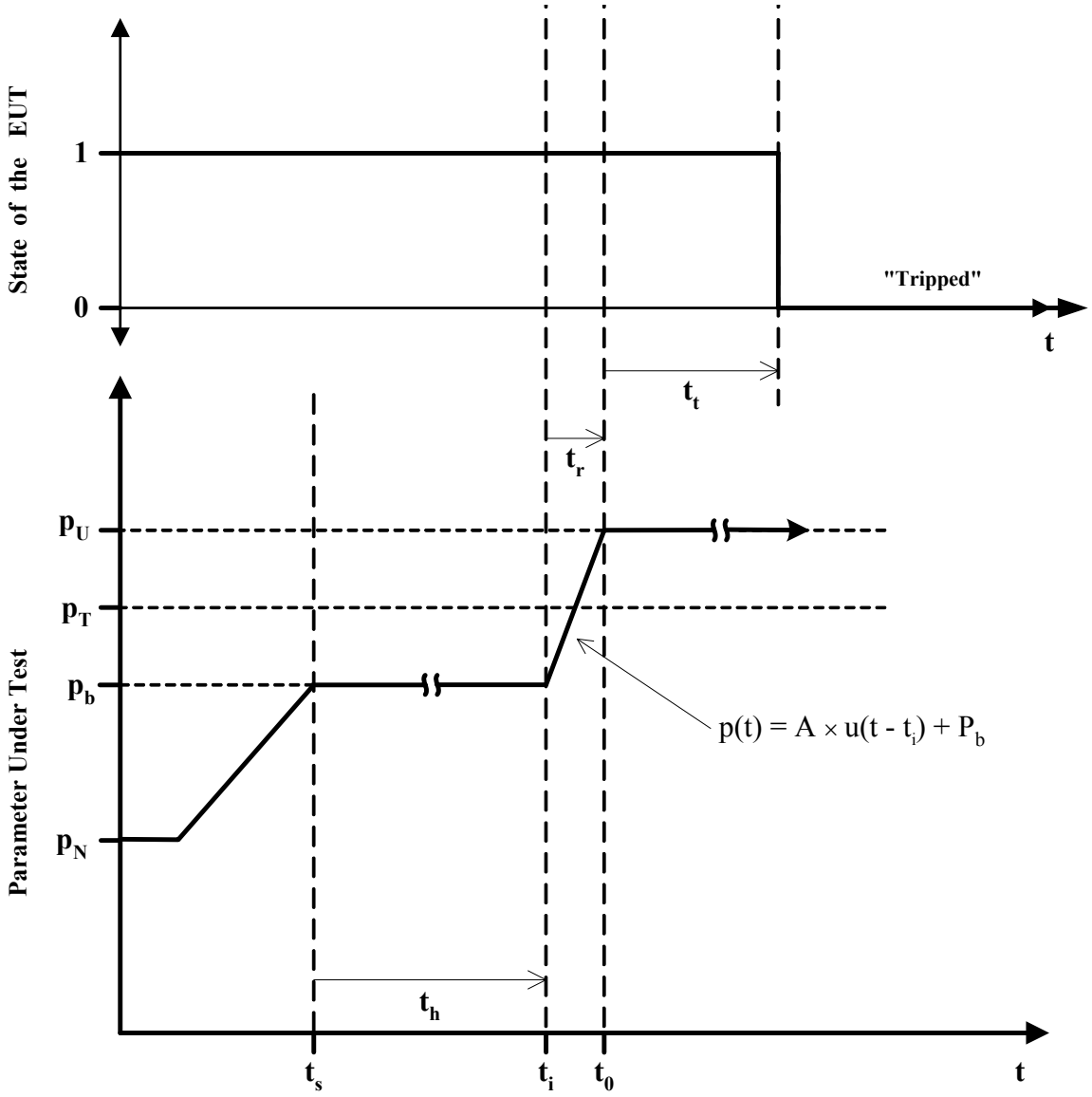


Figure A.3—Graphical representation of time test using step function for PUT

t_0 is the start time of the ramp,

I_b is the starting point of the ramp function.[46]

The slope m is defined by Equation (A.5).

$$m = \frac{(0.5 \times a)}{(2 \times z)} \quad \text{(A.5)}$$

where

z is the time-delay setting (s) for the reverse-power protection parameter plus the manufacturer's stated detection time (s),

a is the manufacturer's stated accuracy of the reverse-power protection parameter.

[46]The starting point I_b shall be within 10% of, but not exceed, the trip point magnitude. At low settings, I_b may be zero.

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The current phase angle θ defined as the phase difference between the voltage and current test signals shall be varied according to Equation (A.6).

$$\theta(t) = -180 \times u(t - t_s) \quad \text{(A.6)}$$

where

θ is the current phase angle,
t_s is the time when the phase-angle change occurs,
t is time (s).

Figure A.4 is a graphical representation of a reverse-power magnitude test using the current magnitude ramp function coupled with a current phase-angle step function. In the figure, i represents the current magnitude, θ represents the phase angle of the current test signal, t represents time, I_N is the nominal current condition, I_T is the trip magnitude,[47] t_0 is the start time of the ramp, and t_s is the instant when the phase transition occurs and the hold time[48] t_h for the test signal starts at starting point I_b.

When the ramp function conflicts with a design characteristic or settings of the EUT, an alternative method that is agreeable to the manufacturer and the testing agency may be used.

A.4 Reverse-power time test (step function)

The test signal described in this subclause is used to characterize the accuracy of the time-delay setting for reverse-power protection parameter.

Vary the current test signals (i.e., magnitude and phase angle) according to the test function defined in this subclause. Therefore, the voltage test signal shall be held at nominal values. The current test signal magnitude i and phase angle θ shall take the form described in Equation (A.7) and Equation (A.8).

$$i = A \times u(t - t_i) + I_b \quad \text{(A.7)}$$

where

i is the current test signal magnitude,
t is time (s),
A is a scaling factor,[49]
I_b is the starting point of the step function.[50]

$$\theta(t) = -180 \times u(t - t_s) \quad \text{(A.8)}$$

where

θ is the current phase angle,
t_s is the time when the phase-angle change occurs,
t is time (s).

[47]For the reverse-power magnitude test, the reverse-power trip magnitude will be a function of the magnitude of the current test signal because the voltage magnitude is at nominal and the phase difference between the voltage and current test signals, θ, is 180°. Where the accuracy of the measurement is affected by p.f., design of the test regimen shall accommodate various power factors.

[48]See Footnote 40.

[49]The scaling factor A shall be chosen so that I_u is at least 110% of I_T.

[50]See Footnote 39.

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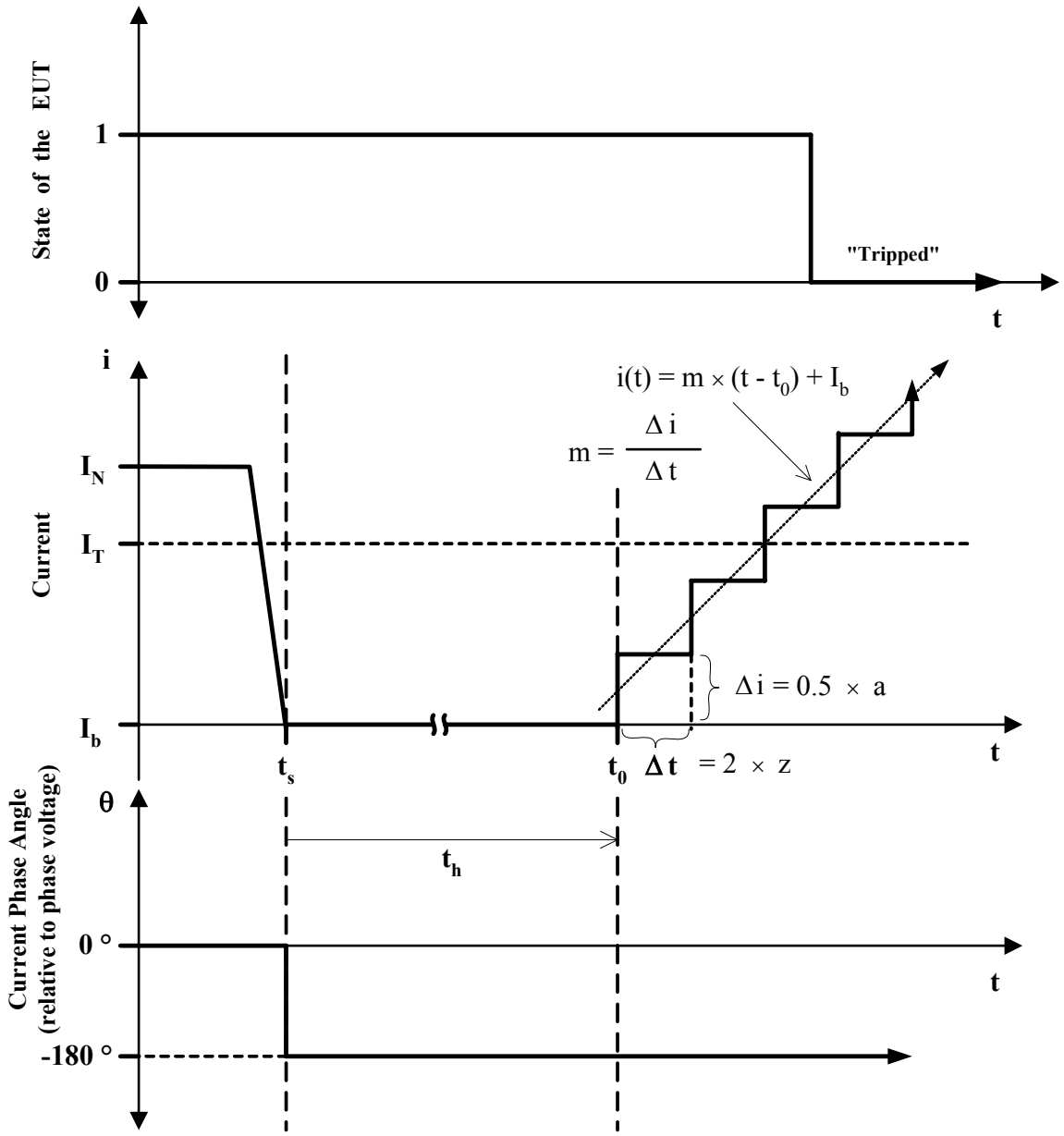


Figure A.4—Graphical representation of reverse-power magnitude test using current magnitude ramp function coupled with current phase-angle step function

Figure A.5 is a graphical representation of the functions used for a reverse-power time test. In the figure, i represents the current test signal, θ represents the phase angle of the current test signal, t represents time, t_t is the trip time, I_N is the nominal current magnitude, I_T is the trip magnitude,[51] I_b is the starting point of the current-magnitude step function, I_U is the final value of the current-magnitude step function, t_0 is the start time used for calculating the trip time, t_i is the start of the current-magnitude step function, t_r is the rise time

[51]For the reverse-power time test, the reverse-power trip magnitude will be a function of the magnitude of the current test signal, because the voltage magnitude is at nominal and the phase difference between the voltage and current test signals, θ, is 180°.

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of the test signal from $(t_0 - t_i)$,[52] t_s is the instant when the phase transition occurs and the hold time[53] t_h for the test signal starts at I_b.

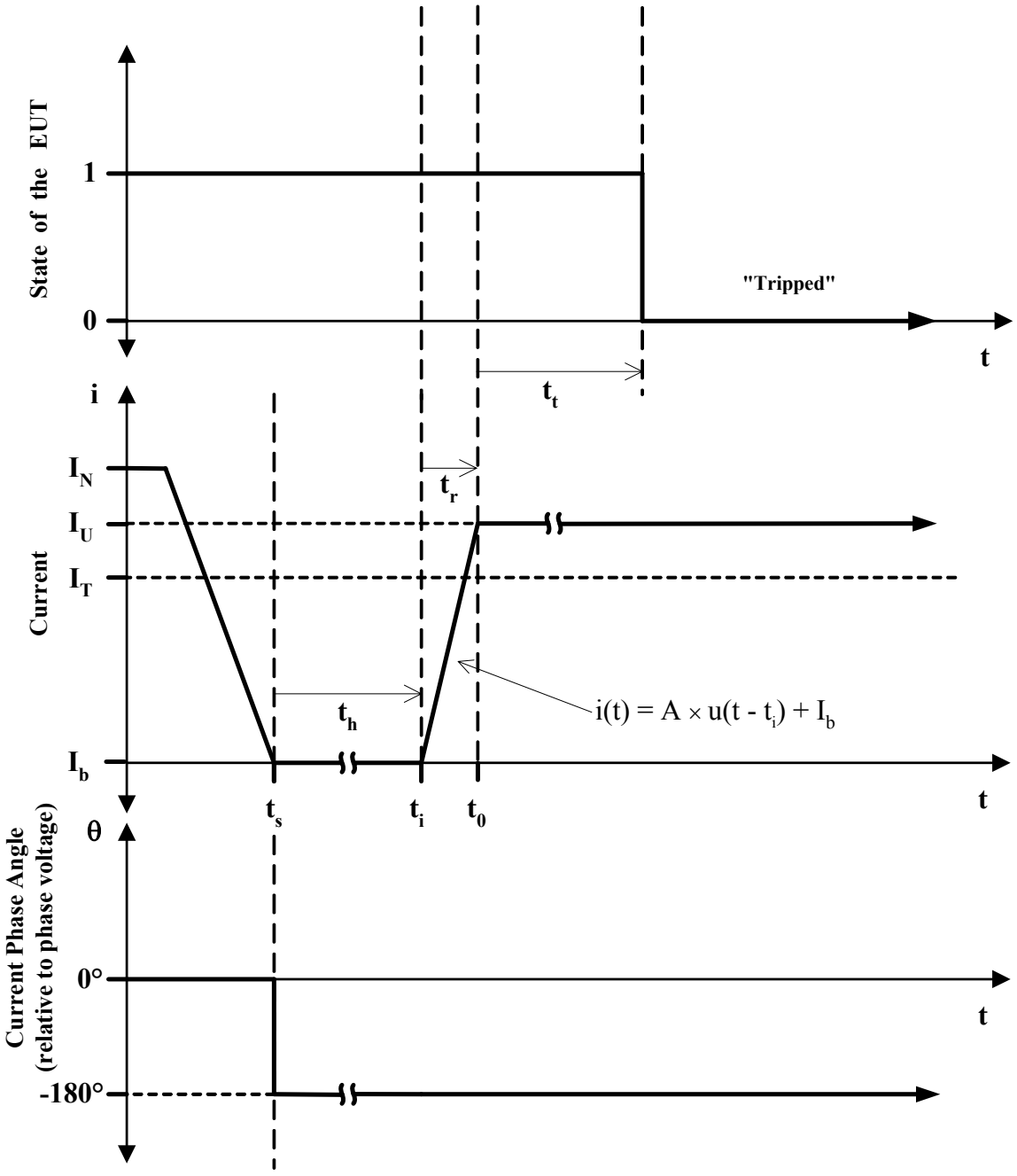


Figure A.5—Graphical representation of reverse-power time test using current magnitude step function coupled with current phase-angle step function

When the step functions conflict with a design characteristic or settings of the EUT, an alternative method that is agreeable to the manufacturer and the testing agency may be used.

[52]The rise time t_r shall be less than the larger of 1 cycle or 1% of the time-delay setting of the PUT.

[53]See Footnote 40.

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Annex B

(informative)

Bibliography

The specifications refer to provisions that do not constitute provisions of this standard. They are listed to provide additional useful information. At the time of publication, the editions indicated were valid. All standards and specifications are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the references listed below.

[B1] IEC TR3 61000-3-7, Electromagnetic Compatibility (EMC)—Part 3: Limits—Section 7: Assessment of Emission Limits for Fluctuating Loads in MV and HV Power Systems—Basic EMC Publication.[54]

[B2] IEC 61000-4-15, Electromagnetic Compatibility (EMC)—Part 4: Testing and Measurement Techniques—Section 15: Flickermeter—Functional and Design Specifications.

[B3] IEC 61400-21, Wind Turbine Generator Systems—Part 21: Measurement and Assessment of Power Quality Characteristics of Grid Connected Wind Turbines.

[B4] IEC 62116, Testing Procedure of Islanding Prevention Measures for Utility Interactive Photovoltaic Inverters.

[B5] IEEE 100, *The Authoritative Dictionary of IEEE Standards Terms*, Seventh Edition, New York, Institute of Electrical and Electronics Engineers, Inc.[55]

[B6] IEEE P1547.2™, Draft Application Guide for IEEE Std 1547, Interconnecting Distributed Resources with Electric Power Systems.[56]

[B7] IEEE P1547.3™, Draft Guide for Monitoring, Information Exchange, and Control of Distributed Resources Interconnected with Electric Power Systems.

[B8] IEEE P1547.4™, Draft Guide for Design, Operation, and Integration of Distributed Resource Island Systems with Electric Power Systems.

[B9] IEEE P1547.5™, Draft Technical Guidelines for Interconnection of Electric Power Sources Greater Than 10 MVA to the Power Transmission Grid.

[B10] IEEE P1547.6™, Draft Recommended Practice for Interconnecting Distributed Resources with Electric Power Systems Distribution Secondary Networks.

[B11] IEEE Std C37.108™, IEEE Guide for the Protection of Network Transformers.

[B12] IEEE Std C57.12.44™, IEEE Standard Requirements for Secondary Network Protectors.

[B13] IEEE Std 120™, IEEE Master Test Guide for Electrical Measurements in Power Circuits.

[54]IEC publications are available from the Sales Department of the International Electrotechnical Commission, Case Postale 131, 3, rue de Varembé, CH-1211, Genève 20, Switzerland/Suisse (http://www.iec.ch/). IEC publications are also available in the United States from the Sales Department, American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY 10036, USA.

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[B14] IEEE Std 519™, IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems.

[B15] IEEE Std 929™, IEEE Recommended Practice for Utility Interface of Photovoltaic (PV) Systems.

[B16] IEEE Std 1001™, IEEE Guide for Interfacing Dispersed Storage and Generation Facilities with Electric Utility Systems.

[B17] IEEE Std 1453™, IEEE Recommended Practice for Measurement and Limits of Voltage Fluctuations and Associated Light Flicker on AC Power Systems.

[B18] UL 1741, Static Inverters and Change Controllers for Use in Photovoltaic Power Systems.[57]

[57]UL standards are available from Global Engineering Documents, 15 Inverness Way East, Englewood, Colorado 80112, USA (http://global.ihs.com/).

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