IEEE Standard for Futurebus+® Spaceborne Systems—Profile S

Sponsor

Bus Architecture Standards Committee
of the
IEEE Computer Society

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Abstract: In the Futurebus+® series of standards, tools with which high-performance bus-based systems may be developed are provided. This architecture provides a wide range of performance scalability over both cost and time for multiple generations of single- and multiple-bus multiprocessor systems. This document, a companion standard to the ISO/IEC 10857: 1994 (ANSI/IEEE Std 896.1, 1994 Edition) Futurebus+® Logical Layer Specification, builds on the logical layer by adding requirements for a spaceborne profile. It is to this profile that products will claim conformance. Other specifications may be required in conjunction with this standard.
Keywords: bus architecture, Futurebus+®, spaceborne computers, spaceborne modules, spaceborne systems

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Introduction

(This introduction is not part of IEEE Std 896.10-1997, IEEE Standard for Futurebus+® Spaceborne Systems—Profile S.)

Overview

Space systems have traditionally pursued point solutions for implementation of digital computers and controllers without regard for accepted commercial standards or component commonality. Stringent size, weight, power, performance factors, and environmental requirements have driven space system developers to these point solutions. The problem with the traditional approach is that the space qualification of multiple unique implementations is expensive and does not permit the reuse of common-function components on multiple missions.

This document provides a standard open architecture framework for implementing spaceborne computer systems while addressing spacecraft unique restrictions. It brings forth several issues not previously defined, namely: (1) establishing common printed circuit board form factors, (2) enabling the prototyping of flight hardware with relatively low-cost commercial equivalents, (3) permitting component reuse across multiple missions, and (4) allowing reduction in the time required to move state-of-the-art technology into existing and new applications. A low-power, high-performance standard backplane tailored specifically for space applications is defined.

This standard, along with the companion IEEE Std 1101.7-1995, *IEEE Standard for Space Applications Module, Extended Height Format E Form Factor (ANSI)*; IEEE Std 1101.3-1993, *IEEE Mechanical Standard for Conduction-Cooled and Air-Cooled 10 SU Modules (ANSI)*; and IEEE Std 1156.4-1997, *IEEE Standard for Environmental Specifications for Spaceborne Computer Modules*, comprise a complete set of standards for implementing spaceborne computer systems that will satisfy a broad range of applications. Compatibility with the Futurebus+ logical layer [ISO/IEC 10857: 1994 (ANSI/IEEE Std 896.1, 1994 Edition)] and provisions for the adoption of the fault tolerance extensions in IEEE Std 896.9-1994, *IEEE Standard for Fault Tolerant Extensions to the Futurebus+® Architecture*, were key elements in this development.

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IEEE Standard for Futurebus+® Spaceborne Systems—Profile S

1. Overview

1.1 Scope

This interface standard establishes a modular open architecture for spaceborne computing systems employing digital computers, processors, and other electronic modules. It provides for the integration and interoperability of diverse sets of electronic modules for the purpose of configuring various types of spaceborne computer systems. This standard specifies the electrical, logical, mechanical, thermal, and input/output interfaces necessary to allow modules developed to this standard to operate together in an integrated system or subsystem. In particular, the issues unique to spaceborne systems, such as size, weight, power, environment, reliability, and fault tolerance, are addressed. This common interface standard will allow the development of cost-effective, reliable, fault tolerant modules that will have broad application across the range of space vehicles.

1.2 Applicability

The applicability of this standard includes all spaceborne computing systems in spacecraft or launch vehicles of any mission duration or environment.

1.3 Background to the standard

This standard is the top-level document specifying a family of interoperable high-performance backplane bus connected modules. As such, this standard is built upon the collected work of many other standards. A decision was made early on in the creation of this standard not to repeat verbatim specifications carried in lower-level standards but instead to accurately reference them in this document. Most specifications in this document beyond references to other standards represent new or changed specifications. As much rationale as possible has been included throughout this standard; however, it will be next to impossible to fully understand this standard without a cursory understanding of the underlying standards.

To make full use of this standard, one needs to obtain or be familiar with the content of most if not all of the referenced IEEE standards. These are listed in 2.1.1. This standard is built upon the Futurebus+® family of standards and the Serial Bus (IEEE Std 1394-1995) standard. One should review the logical layer as defined in ISO/IEC 10857: 1994 and the physical layer as defined in IEEE Std 896.2-1991 to understand the basic Futurebus+ protocol. Since all Profile S modules will be fault tolerant at the bus level, one should next look

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at the extensions to the Futurebus+ that are added by IEEE Std 896.9-1994. At about this time, one will probably need more understanding of the Control and Status Register (CSR) architecture as defined in ISO/IEC 13213: 1994. This is the basis of both the Futurebus+ and Serial Bus. Serial Bus is a mostly stand-alone document, and this standard specifies the backplane version for use on Profile S modules and should be looked at next. At this point, the only additional requirement is an understanding of the physical form factors and the environment. The environment is specified in IEEE Std 1156.4-1997. Two form factors have been specified for Profile S modules—SEM-E Stretch (IEEE Std 1101.7-1995) and 10 SU (IEEE Std 1101.3-1993). With at least a cursory understanding of the contents of these standards, one can now more fully appreciate and use this document.

1.4 Structure of the standard

Clause 4 presents in table form a summary of most of the content of this standard. After this, Clause 5 details the Futurebus+ logical layer, Clause 6 the utility signals, Clause 7 the fault tolerance aspects of the Futurebus+ and utility signals, and Clause 8 the Serial Bus. Clause 9 maps the CSRs from all the underlying standards (both Futurebus+ and Serial Bus) into a consistent group to be used across all Profile S modules. The majority of the new information here introduces an error correcting configuration of Futurebus+. Clause 10 provides the physical layer detail for a SEM-E Stretch module, and Clause 11 gives the same for a 10 SU module. Clause 17 provides a second connector variation for the SEM-E Stretch form factor. These subclauses provide the interoperable pinout definitions on each of these form factors. Since the electrical characteristics are different (lower power) in this standard than the standard backplane transceiver logic (BTL) called out in IEEE Std 896.2-1991, Clause 12 gives the specifications for compatible operation. Clause 13 provides the detail of the power distribution. Clause 14 details the environmental requirements and mostly references the user to IEEE Std 1156.4-1997. Clause 15 collects in one place the recommended practices for the use of the Space Profile. Clause 16 provides a guide for manufacturers of Profile S modules, giving required and recommended data that should be provided for the best use of a Profile S module. Finally, a bibliography of works of interest is included in Annex A.

1.5 How to use this standard

This document may be used in different ways by different users for specific purposes. If one is a silicon implementor, ISO/IEC 10857: 1994, IEEE Std 896.2-1991, IEEE Std 896.9-1994, and IEEE Std 1394-1995 provide most of the information one needs. This standard provides two new major areas of interest. The first is the new electrical requirements, which are applicable to all Profile S modules. These have been defined these so that protocol chips and functions that meet the above bus standards will work with parts made to the new electrical standards as a direct replacement for BTL in order to leverage off much higher volumes that drive the development of the protocol chips. Clause 12 provides the areas of the most interest. The second new area of interest is the Error Correcting configuration definition. Much of the new function in this standard is directed to this bus implementation. It has been blended, wherever possible, with equivalent parts of the existing standards. Someone trying to implement silicon to support the Error Correcting configuration should pay particular attention to the logical layer extensions and the CSRs to decide where to implement these signals.

To the module or system builder, this document provides the interconnect in either Clause 10, 11, or 17. While SEM-E Stretch provides what most users need today with its 32-bit bus capabilities, the forward-thinking system builder may want to start with 10 SU to have many more I/Os today and a more expandable form factor for the future. A system builder should review the excellent Failure Modes and Effects Analysis (FMEA) in IEEE Std 896.9-1994 as a starting point for performing the various analyses required to determine the overall fault tolerance capability of the system. A functional fault analysis (i.e., an analysis of error classes and how they are handled at each error containment region) is a recommended front-end system engineering activity. A Profile S module is a natural error containment region. The error handling scenarios provided in IEEE Std 896.9-1994 provide most of the potential interface error classes. These may then be extended to include the actual complete view of the error classes at each bus's level in the system.

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To the device driver writer, the detailed CSR definitions in Clause 9 as well as those referenced in IEEE Std 896.9-1994, ISO/IEC 10857: 1994, and ISO/IEC 13213: 1994, are important. Error scenarios in IEEE Std 896.9-1994 indicate what shall be logged in each error case and provide a structure for handling the many types that may be injected. This standard adds spare signals to the Error Correcting configuration that provide another recovery method for this bus. The various registers provided for diagnostics and fault injection may be used to create those services. These CSRs were developed based on collective contributions from telecommunications, military, commercial, and space users. Wherever possible, CSRs were reused from other profiles rather than invented anew. The device driver writer should check upon availability of device drivers for these profiles as a way to reuse much of their content and then personalize it to Profile S.

Finally, the user of modules built to this standard should specify exactly what is required but leave as much optional as possible. This will enable a smaller set of interoperable modules to serve a larger application space. One area where this is especially true is in pinouts. Space users have always created unique solutions in the past. Because of this heritage, the working group could not specify just one pinout or one I/O configuration and expect anyone to use it. But having 44 different module classes identified introduces complexity in interoperability between modules. Many of these are naturally interoperable. But unique requirements can be placed on a module that will make it interoperable only with its own class. A good way to look at this is to lay out requirements over more than one application or over more than one time period. Look for commonality and look at the areas where growth is desired. Try to specify what will work for the first and what could be used as at least a foundation for the second. Specifying individual needs with a global view should enable more reuse. In the future, one can take a collection of previous application modules and put together a quick prototype similar to what is possible today with buses like VME.

1.6 Why use this standard

This standard was developed so that a scalable high-performance commercial standard (Futurebus+) could be applied and used in spacecraft applications. The major problems considered to make this possible are those that apply to any space system: size, weight, power, fault tolerance, and radiation.

The commercial Futurebus+ is a strong foundation on which to build this spaceborne standard. It provides high performance that is scalable; significant configuration options in message passing, arbitration, and transaction variety; a standardized register interface, backplane interoperability, and cache coherency; and a commercial base upon which to build.

In the size and weight area, two standard form factors and a matching high density connector for each that pack a maximum amount of pins into the smallest area possible have been specified. A variety of pinout configurations to enable this to be used in small 1–5 slot applications equally as well as in large 15+ slot applications has been provided. Using Futurebus+ and its built in scalability and personalization features, one may build a range of backpanels that either emphasize bus bandwidth, external I/O control and status, or a combination of both.

A major challenge in bringing Futurebus+ to space was to reduce the power of each module's transceivers. A new electrical specification has been developed that maintains the incident wave switching properties of BTL yet cuts the power required by over 80% per slot with only a small degradation in performance. Although not electrically compatible with BTL, it is expected that there will be transceivers built that are compatible with the commercial protocol chips available today. Space profile boards may be separately powered due to the cold-spareable properties of the electrical interface.

In the fault tolerance area, all extensions provided by IEEE Std 896.9-1994 have been incorporated, and three different levels of bus fault tolerance have been defined. An application can use the one that best matches the rest of its subsystem, detection, and latency requirements. A Level 0 sublevel is provided to match current silicon. A Profile S module's Futurebus+ interface will be single point fault tolerant. It will also have the diagnostic capability of any telecommunication system due to the strong influence of the tele-

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communications profile on this work. Therefore, one may build a system that has full access to telemetry data on the module. One may also build a system that autonomously attempts recovery from errors.

Finally, all Profile S modules shall be built to meet environmental performance levels for the environments specified in IEEE Std 1156.4-1997. This should greatly reduce the uniqueness of each program in the environmental area. Radiation is one of the major categories addressed by IEEE Std 1156.4-1997, and three levels of radiation tolerance are specified.

This standard has been written to provide applicable specifications today that will go a long way toward standardizing the space computer industry at the board interface level, just as VME boards are standard for many ground applications.

2. References

2.1 Referenced documents

There are several standards that are referenced by the work being done on Futurebus+ documents. While the companion standards are stand-alone, i.e., can be referenced by other bus specifications, these standards must be referenced to ensure intermateable and interoperable systems. This standard shall be used in conjunction with the following standards. When the following standards are superseded by an approved revision, the revision shall apply. These standards are listed below:

2.1.1 IEEE standards

IEEE Std 896.2-1991, IEEE Standard for Futurebus+®—Physical Layer and Profile Specification (ANSI) *(includes IEEE Std 896.2a-1994).*[1]

IEEE Std 896.3-1993, IEEE Recommended Practices for Futurebus+® (ANSI).

IEEE Std 896.4-1993, IEEE Standard for Conformance Test Requirements for Futurebus+® (ANSI) *(includes IEEE Std 896.4a-1995).*

IEEE P896.6, Draft Standard for Futurebus+®—Telecommunications Profile (D3, Dec. 1994).[2]

IEEE Std 896.9-1994, IEEE Standard for Fault Tolerance Extensions to the Futurebus+® Architecture (ANSI).

IEEE Std 1101.3-1993, IEEE Mechanical Standard for Conduction-Cooled and Air-Cooled10 SU Modules (ANSI).

IEEE Std 1101.4-1993, IEEE Standard for Military Module, Format E Form Factor (ANSI).

IEEE Std 1101.7-1995, IEEE Standard for Space Applications Module, Extended Height Format E Form Factor (ANSI).

IEEE Std 1156.1-1993, IEEE Standard for Microcomputer Environment Specifications for Computer Modules (ANSI).

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IEEE Std 1156.4-1997, IEEE Standard for Environmental Specifications for Spaceborne Computer Modules.

IEEE Std 1212.1-1993, IEEE Standard for Communicating Among Processors and Peripherals Using Shared Memory (Direct Memory Access—DMA) (ANSI).

IEEE Std 1394-1995, IEEE Standard for a High Performance Serial Bus (ANSI).

ISO/IEC 10857: 1994 (ANSI/IEEE Std 896.1, 1994 Edition), Information technology—Microprocessor systems—Futurebus+®—Logical protocol specification *(includes IEEE Std 896.1a-1991)*.[3]

ISO/IEC 13213: 1994 (ANSI/IEEE Std 1212, 1994 Edition), Information technology—Microprocessor systems—Control and Status Registers (CSR) Architecture for microcomputer buses.

ISO/IEC 14536: 1995 (ANSI/IEEE Std 896.5, 1995 Edition), Information technology—Microprocessor systems—Futurebus+®—Profile M (Military) *(includes 896.5a-1994)*.

2.1.2 Military standards

MIL-STD-1540C, Military Standard Test Requirements for Launch, Upper-Stage, and Space Vehicles, United States Air Force, 15 September 1994.[4]

MIL-STD-1547, Electronic Parts, Materials, and Processes for Space and Launch Vehicles, United States Air Force, 1 Dec. 1987.

MIL-STD-1553B, Aircraft Internal Time Division Command Response Multiplex Data Bus, Notice 2-8 Sep. 1986.

MIL-STD-1773, Fiber Optic Mechanization of an Aircraft Internal Time Division Command/Response Multiplex Data Bus, Notice 1-2 Oct. 1989.

2.1.3 EIA standards

EIA IS E700A, 396 Pin Connector Keying.[5]

EIA IS 22, 372 Pin Connector Keying.

EIA PN 2933A, 556 Pin Connector Keying.

2.2 Conflicting standards

Should any of the above standards conflict as to the implementation of CSRs, the precedence shall be resolved with the following priority: this standard, IEEE Std 896.9-1994, ISO/IEC 10857: 1994, IEEE Std 896.2-1991, IEEE Std 1394-1995, and ISO/IEC 13213: 1994.

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[3]ISO/IEC (ANSI/IEEE) publications are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA. They are also available from IEC Sales Department, Case Postale 131, 3 rue de Varembé, CH-1211, Genève 20, Switzerland/Suisse.

[4]Military standards and handbooks are listed in the Department of Defense Index of Specifications and Standards (DODISS). Copies of the DODISS are available on a yearly subscription basis from the Director, Navy Publications and Printing Office, 700 Robbins Avenue, Philadelphia, PA 19111-5093, USA.

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3. Definitions

3.1 Special word usage

3.1.1 may: A keyword that indicates flexibility of choice with no implied preference.

3.1.2 not supported: Profile-Compliant systems or modules may not respond, or may respond inappropriately, to the existence or assertion of the feature under discussion.

3.1.3 optional, option: Refers to the implementation or use of a function that is not required. Options may be Futurebus+-specific, profile-specific, vendor-specific, or unit-specific. The latter two are not discussed or specified in profiles, and may be implemented provided they do not conflict in any way with profiles or other standards, have no effect on required levels of interoperability, and are fully documented in product specifications. Futurebus+-specific options are those that are specified in Futurebus+ documents. Reference shall be made to the appropriate standard, with wording such as "if implemented, this option shall meet the requirements specified in (document and subclause)." An example of a Futurebus+-specific option is distributed arbitration. Similarly, a profile-specific option is one that is specified in detail in the profile. Any profile-compliant design implementing that function shall do it as specified in the profile. Availability of an option shall not be required for the correct operation of a profile-compliant module or system; modules implementing an option should be able to default to operation with the option disabled. Availability of an option should be specified in a documented capability read-only memory (ROM) bit in Control and Status Register (CSR); a corresponding read/write bit should be available to turn the function on or off.

3.1.4 prohibited: Profile-Compliant systems or modules shall not exhibit or assert the behavior or function under discussion. Modules compliant with multiple profiles may implement a function prohibited by a profile provided that function is disabled in systems compliant with that profile, or provided they do not direct prohibited transactions at modules compliant with that profile.

3.1.5 required or mandatory: All profile-compliant modules or systems shall implement the specified feature or function.

3.1.6 shall: A keyword that indicates a mandatory requirement. Designers must implement all such mandatory requirements to ensure interoperability with other IEEE Std 896.10-1997 compliant designs.

3.1.7 should: A keyword that indicates flexibility of choice with a strongly preferred implementation. The phrase "it is recommended" is used interchangeably with the keyword *should*.

3.1.8 supported: Profile-Compliant systems or modules shall respond appropriately to the existence or assertion of the specified feature or function. The profile or a referenced Futurebus+ standard shall specify the appropriate functional behavior or design.

3.2 Bus line and signal conditions

3.2.1 activate: (A) The action of applying signals to a group of bus lines. (B) The state of a group of bus lines when they carry signals.

3.2.2 assert: (A) The action of applying a logic 1 signal to a bus line. (B) The state of a bus line when the signal it carries represents a logic 1.

3.2.3 * (asterisk): When appended to a signal's name, the suffix "*" (asterisk) indicates that the logic 1 state of the signal is represented by a less positive voltage than the logic 0 state.

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3.2.4 bus line: The medium for the transmission of signals. Futurebus+ Spaceborne Profile uses both open collector and push-pull drivers to match whether a signal is expected to be driven by more than one board simultaneously. A bus line is driven by only one board for those signals that are push-pull. A bus line may be driven by several boards simultaneously for those signals that are open collector. Therefore, the signal carried by the bus line is the combination of signals applied to that line from each board in the open collector case or from the one board in the push-pull case.

3.2.5 release: (A) The action of applying a logic 0 signal to a bus line. (B) The state of a bus line when the signal it carries represents a logic 0.

3.2.6 signal names: The simplified alphanumeric notation used to represent a group of lines or signals. For example, where a group of bus lines are represented by the same letters, the lines within the group are numbered, e.g., **AD0**, **AD1**, **AD2**, etc. In order to represent a group of lines or signals in more convenient form, the notation **AD[31..0]** is used. Also, the notation **AD[ ]** is used to refer to all of the lines within the group.

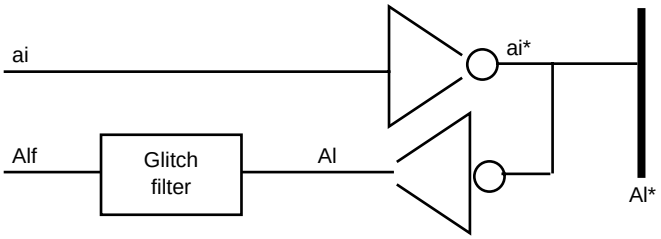

Figure 3-1—Signal naming convention

The signal that a module applies to the module-side input of its driver is designated by a lowercase label, e.g., **ai.** The signal that a specific module applies to a bus line is designated by a lowercase label with an asterisk, e.g., **ai*.** The signal that appears on a bus line as the result of the combined signals applied to it by all modules is designated by an uppercase label with an asterisk, e.g., **AI***.

When appended to a signal name, the suffix “f” (filtered) refers to the bus line signal after it has passed through a receiver and a wire-or glitch filter (integrator). For example, **AIf** refers to the signal on the **AI*** line, after it has passed through an inverting receiver to become **AI** and the wire-or glitch filter to become **AIf.**

3.3 Futurebus+ terminology

3.3.1 Application Environment Profile (AEP): A document that describes functional requirements and points to existing standards, selecting and binding options within those standards. An implementor who then designs a specific module and/or system should be reasonably assured that another designer’s (manufacturer’s or supplier’s) modules will properly function within the same system. This includes all aspects of definition: mechanical, electrical, protocol, environmental, and system considerations.

3.3.2 backplane: An electronic circuit board and connectors used to interconnect modules together electrically. The backplane connects selected pins of the connectors, thus providing the medium for the transfer of signals needed for the operation of the bus.

3.3.3 backplane bus: A means to connect circuit modules using common signal traces on a backplane and a standard set of rules.

3.3.4 big endian: A method of storing multibyte data in a byte-addressable memory such that the most significant byte of the data is stored at the lowest address.

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3.3.5 bus bridge: A bus bridge is an interconnect between two or more buses that provides signal and protocol translation from one bus to another. The buses may adhere to different bus standards for mechanical, electrical, and logical operation (such as a bus bridge from Futurebus+ to VMEbus or to Multibus II).

3.3.6 command_reset: An initialization event that is initiated by a write to the **RESET_START** CSR.

3.3.7 CSR: Control and Status Register.

3.3.8 geographical address: A unique identifier statically assigned to each slot by the backplane.

3.3.9 glitch filter: As explained in ISO/IEC 10857: 1994, this filters out a fundamental transmission line effect found in bused backplane implementations. The effect is commonly called the *wire-OR glitch*.

3.3.10 immediate entry: A read-only memory (ROM) entry that provides a 24-bit immediate data value.

3.3.11 intermateable: Mechanical compatibility between modules with the backplane, card cage, and system into which they are inserted. Sometimes includes compatibility in the assignment of power and ground pins.

3.3.12 interoperate, interoperability: Compatibility of modules with each other or with the system/backplane into which they are inserted. When a pair of such units is said to *interoperate*, (a) they cannot suffer damage as a consequence of being powered and functioning in the same system; (b) the modules and the system will each be able to perform the basic function for which they were designed; (c) the modules will be able to communicate with each other using specified Futurebus+ transactions.

Some modules or backplanes will have optional features not shared by others in the same system, so they need to be able to default to the smaller common set in order to communicate with each other. A module or system working in such a reduced-capability mode may suffer performance degradation that may be severe, but will still be interoperable in that system.

3.3.13 key: When used in the context of a read-only memory (ROM) entry, a key is an 8-bit field whose value identifies a ROM location as an immediate entry, offset entry, leaf entry, or subdirectory entry. This is a term used (but not defined) in ISO/IEC 13213: 1994.

3.3.14 leaf entry: A read-only memory (ROM) entry that specifies the address of a variable-length data block.

3.3.15 little addressian: A description of the physical location of data-byte addresses on a multiplexed address/data bus. On such a bus, the data-byte with the smallest address is multiplexed (in time or space) with the least significant byte of the address.

3.3.16 little endian: A method of storing multibyte data in a byte addressable memory such that the least significant byte of the data is stored at the lowest address.

3.3.17 live insertion: The process of inserting boards into a backplane when power is on. Insertion of boards into a backplane can be performed when power is off or when power is on.

3.3.18 LSB: Least significant bit.

3.3.19 monarch processor: The processor that is selected to partially initialize the local-bus resources and fetch the initial boot code.

3.3.20 MSB: Most significant bit.

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3.3.21 node: A set of Control and Status Register (CSR) addresses (including identification read-only memory and reset command registers) that are initially defined in a 4 kB (minimum) initial node address space. Each node can be reset independently (a reset of one node has no effect on other nodes).

3.3.22 node ROM: A range of register addresses that are mapped to address offsets 1024 to 2047. In ISO/IEC 13213: 1994 this is known as ROM_WINDOW.

3.3.23 offset entry: A read-only memory (ROM) entry that provides a 24-bit offset value. The offset values specifies the location of a Control and Status Register (CSR) that provides a 32-bit parameter.

3.3.24 Profile S module: The assembled unit, containing a Futurebus+ interface and one or two nodes complying with Profile S, which is inserted into a compatible Futurebus+ slot.

3.3.25 Profile S system: The assembly of hardware elements made up of, at a minimum, the Profile S compliant backplane, card cage, and a power supply. Modules complying with other profiles may operate compatibly with Profile S systems and modules if they meet Profile S mechanical requirements, and if their features constitute an identity or a superset of those mandated in this profile.

3.3.26 root directory: A region in read-only memory (ROM) specified in ISO/IEC 13213: 1994 whose size is identified in the first location of the root directory and whose contents include ROM entries that may be identified using the ROM key.

3.3.27 SEM-E Stretch: A mechanical module equivalent in design to the module defined by IEEE Std 1101.4-1993. The height of this module has been extended beyond the measurement given in IEEE Std 1101.4-1993. The complete mechanical specifications for the SEM-E Stretch can be found in IEEE Std 1101.7-1995.

3.3.28 serial bus: A peripheral interconnect and an alternate diagnostic and control path.

3.3.29 slot: A mechanical location on a backplane.

3.3.30 subdirectory entry: A read-only memory (ROM) entry that specifies the address of another ROM subdirectory.

3.3.31 system configuration process: The software that initializes the system. The monarch processor executes the system configuration process.

3.3.32 system reset: As specified in ISO/IEC 10857: 1994, this is an initialization event initiated when any module asserts the **re*** signal for 100 to 200 ms. The equivalent term for this event, found in ISO/IEC 13213: 1994, is *power_reset*.

3.3.33 unit: A subcomponent of a node that provides a processing, memory, or I/O functionality. After the node has been initialized (typically by generic software), the unit provides the register interface that is accessed by I/O driver software. The units normally operate independently of each other, and do not affect the operation of the node upon which they reside. Note that one node could have multiple units (for example, processor, memory, and SCSI controller).

3.3.34 write one to clear: A method used to clear specific bits in a register. For example, if a write one to clear register contained 0xFFFFFFFF and the value 0x00800000 was written into it, the contents of the register would become 0xFF7FFFFF. (In 4.3 this method is spelled out as R/C.)

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3.4 Conventions

— Hexadecimal numbers in this specification are represented by the notation 0x####, where each "#" is an integer from 0–9 or a letter from A–F.
— Binary numbers in this specification are represented by a sequence of 1s and 0s with subscript 2 (e.g., $10 = 0{\times}A = 1010_2$).
— All other numbers in the specification are decimal numbers.
— Superscript (e.g., 2^{32}) indicates "to the power of."
— All register names and bit names are uppercase.
— Futurebus+ is little endian.
— CSRs are big endian.
— For all CSRs in this specification, the bit position of each data bit when reading or writing the CSR from the Futurebus+ may be determined by overlaying Figure 3-2 on the CSR figure.

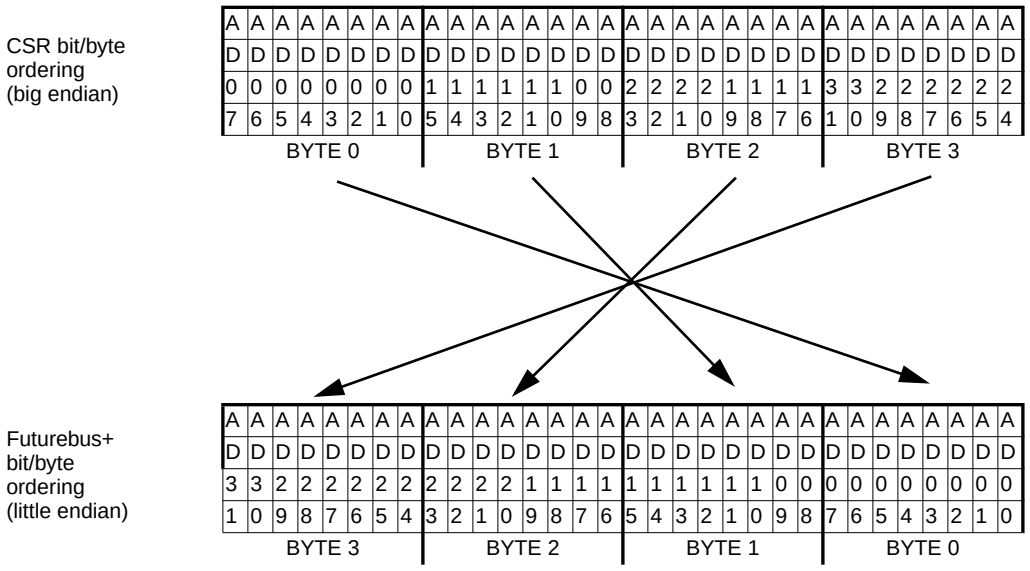

Figure 3-2—CSR bit positions

3.5 Syntax

In Clause 9, fields within the CSRs are denoted in uppercase, bold notation using the following convention:

OWNING-MODULE.CSR-NAME.CSR-FIELD where the optional **OWNING-MODULE** attributes may be one of MASTER, if the MASTER attribute is validly true in the context; or SLAVE, if the MASTER attribute is validly false in the context; or MODULE, if the MASTER attribute is irrelevant in the context. **CSR-NAME** is a valid CSR. **CSR-FIELD** is defined as contiguous bits within **CSR-NAME**.

Symbols used in equations obey the syntax and precedence noted in 2.4 of ISO/IEC 10857: 1994. In addition, the change in the state of fields within CSRs is noted with the following convention:

OWNING-MODULE.CSR-NAME.CSR-FIELD<-new-state where the left-hand side of the expression denotes the field that shall be updated with the right-hand side of the expression as a result of execution of the expression.

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3.6 Futurebus+ logo

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Figure 3-3—896.10 logo



Figure 3-4—896 logo

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4. Profile S reference specification

4.1 Introduction

This clause specifies those aspects of a class of modules, backplanes, and chassis required to guarantee interoperability at the physical (mechanical, electrical, and environmental) layer. This profile also specifies the logical layer and guarantees interoperability between modules with common features. Two form factors are specified for Profile S modules, SEM-E Stretch and 10 SU, as shown in Table 4-1. SEM-E Stretch modules are further subdivided between two connector sizes. The major difference between the three form factor options is the number of pins available in each backplane connector. The logical layers are almost identical: the few differences that occur in module and backplane address and data path width are pinout related. All form factors support a 32-bit bus width. Higher-Performance bus widths are available based on the number of connector pins.

Table 4-1—Space profile form factors

Form factor	Standard	Connector pins	Bus width
SEM-E Stretch	IEEE Std 1101.7-1995	396	32, (64)
SEM-E Stretch	IEEE Std 1101.7-1995	372	32, (64)
10 SU	IEEE Std 1101.3-1993	556	32, (64), (128)

SEM-E Stretch and 10 SU modules may be designed to work in other profile systems that utilize similar logical and the same physical (mechanical and electrical) definitions. When designing a module that is compliant with multiple profiles, one must carefully compare the logical functions.

All Profile S modules are fault tolerant as specified by IEEE Std 896.9-1994. However, this profile specifies three levels of fault tolerance centered around their recovery latency for handling hard errors detected on the bus, as shown in Table 4-2. A subset of the first two levels is also specified (Level 0) that matches current silicon and is more fault tolerant than ISO/IEC 10857: 1994 and IEEE Std 896.2-1991 yet not as complete as the levels specified herein.

Table 4-2—Space profile fault tolerance levels

Fault tolerance level	Bus error removal	Hard error replacement
Single Futurebus+	Detect, Retry	Entire subsystem
Dual Futurebus+	Detect, Retry, Swap Bus	Entire bus
Error Correcting Futurebus+	Detect, Correct, Retry, Swap Signal	Signal

The Single Futurebus+ will detect all single point errors and support retry in order to remove transient bus errors. If the bus is found to have a hard error, then that bus subsystem is either no longer capable of using the Futurebus+ or must use it in a degraded mode.

The Dual Futurebus+ level provides two identical Futurebus+ buses on the same physical backplane. One is normally active at a time although the use of both simultaneously is also permitted. If the detection and retry is unsuccessful in removing an error from a bus, the subsystem (through its monarch or through some form

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of distributed decision-making capability) may decide to switch to the second bus. As in the Single Futurebus+, either bus could be utilized with errors in various degraded modes depending on the types of hard errors encountered.

The Error Correcting Futurebus+ corrects all single errors immediately upon detection. If an error continues to be detected after the initial correction, then it may be removed by sparing the pin in error as indicated by the syndrome bits. As in the case of a Dual Futurebus+, this sparing shall be directed by the Bus Monarch or by some form of distributed decision-making among bus masters.

Table 4-3 shows the relationships between the three fault tolerance variations, bus widths, and form factors.

Table 4-3—Space profile bus widths

Bus width	Single Futurebus+	Dual Futurebus+	Error Correcting Futurebus+
32 bits	SEM-ES/10 SU	SEM-ES/10 SU	SEM-ES/10 SU
64 bits	SEM-ES/10 SU	10 SU	10 SU
128 bits	10 SU	Not supported	Not supported
256 bits	Not supported	Not supported	Not supported

The four variants of the three levels of fault tolerance have been combined into a single footprint for each form factor. However, for a given subsystem backpanel, only one of these fault tolerance levels may be implemented. The Profile S Futurebus+ signal set common to all configurations is designated FB+1. The Profile S Futurebus+ signal set providing the second bus on a given backpanel is designated FB+2. The Profile S Futurebus+ signal set providing the error correcting bus on a given backpanel is designated as the normal signals, with A and B copies.

The Profile S Serial Bus signal set common to all configurations is designated SB-1. The Profile S Serial Bus signal set providing the second bus on a given backplane is designated SB-2.

All Profile S modules shall provide signals in addition to the base Futurebus+. These include various utility signals and one or two Serial Buses. The Serial Buses provide an alternate access path in the event of an error as well as a diagnostic and test interface. One set of functional utility and Serial Bus signals accompanies a Single Futurebus+. A second set accompanies the Dual Futurebus+. In the Error Correcting configuration, the functional utility signals and the Serial Bus signals are simply duplicated due to their nonfunctional usage. Only one copy of the test signals is present in all configurations.

Profile S User I/O should be through the backplane. Since most I/O in spacecraft is point to point and not bused between backpanel modules, and due to the large number of unique I/O solutions in existing space systems, this profile has not attempted to lay out all possible options for I/O. In cases when a bus such as MIL-STD-1553B is identified as having widespread use throughout the space community, it will be defined as an option in this profile. Otherwise I/O are left to the discretion of the module and system designers with the caveat that I/O modules must be interchangeable for a class of Profile S modules as defined in Table 4-4. Each class will have its own unique keying as defined in 10.3.5, 11.3.5, and 17.3.5. There are 44 possible module types with the options shown in Table 4-4. It is strongly suggested that implementors concentrate on a subset of module types to maximize the interchangeability of solutions and use new types only when absolutely necessary.

ISO/IEC 10857: 1994 and IEEE Std 896.2-1991 incorporate features required for fault tolerant, real-time, secure, testable, reliable, and maintainable systems. IEEE Std 896.3-1993 and IEEE Std 896.9-1994 provide

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additional guidelines and insight into the implementation of these features. Many of these features are required to complete a well-defined system. When implementing a specific feature included in IEEE Std 896.3-1993 and not overridden in IEEE Std 896.9-1994 or this document, that feature shall be implemented as defined in IEEE Std 896.3-1993.

Table 4-4—Profile S module classes

Profile S class	Form factor	Fault tolerance	Width (bits)	Special functions
0–15	SEM-E Stretch (either connector)	Single Futurebus+ Dual Futurebus+ Error Correcting Futurebus+	32 or 64 32 32	None, 1553B, central arbiter, or both
100–127	10 SU	Single Futurebus+ Dual Futurebus+ Error Correcting Futurebus+	32, 64, or 128 32 or 64 32 or 64	None, 1553B, central arbiter, or both

4.2 Target applications

Profile S is specifically designed for spaceborne applications; hence, modules are strictly conduction cooled. Minimum size, weight, and power as well as the ability to tolerate harsh radiation, shock, and vibration environments are primary concerns for implementors of spaceborne computing systems. Logical functionality is specified to ensure interoperability.

4.3 Reference tables

Table 4-5 lists the features of the SEM-E Stretch and 10 SU logical layer and indicates whether the referenced specification is required (mandatory) or optional. Table 4-6 lists the physical features of SEM-E Stretch and 10 SU in a similar manner. Fault Tolerant requirements not part of the fault tolerant subset (Level 0) are indicated by "(L0-opt)".

Table 4-5—Profile S logical layer requirements

Function		Single Futurebus+	Dual Futurebus+	Error Correcting Futurebus+
Arbitration[a]				
Central/Distributed		Required	Required	Required
Central Arbiter		Optional	Optional	Optional
Arbitrated Messages		Optional	Optional	Optional
SEM-E Stretch form factor module address width				
FB+ 1	32	Required	Required	Required
	64	Optional	Not supported	Not supported
FB+ 2	32	Not supported	Required	Not supported
	64	Not supported	Not supported	Not supported
10 SU form factor module address width				
FB+ 1	32	Required	Required	Required
	64	Optional	Optional	Optional
FB+ 2	32	Not supported	Required	Not supported
	64	Not supported	Optional	Not supported

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Table 4-5—Profile S logical layer requirements *(continued)*

Function		Single Futurebus+	Dual Futurebus+	Error Correcting Futurebus+
SEM-E Stretch form factor module data path width				
FB+ 1	32	Required	Required	Required
	64	Optional	Not supported	Not supported
	128	Not supported	Not supported	Not supported
FB+ 2	32	Not supported	Required	Not supported
	64	Not supported	Not supported	Not supported
	128	Not supported	Not supported	Not supported
10 SU form factor module data path width				
FB+ 1	32	Required	Required	Required
	64	Optional	Optional	Optional
	128	Optional	Not supported	Not supported
FB+ 2	32	Not supported	Required	Not supported
	64	Not supported	Optional	Not supported
	128	Not supported	Not supported	Not supported
SEM-E Stretch form factor backplane width				
FB+ 1	32	Required	Required	Required
	64	Optional	Not supported	Not supported
	128	Not supported	Not supported	Not supported
FB+ 2	32	Not supported	Required	Not supported
	64	Not supported	Not supported	Not supported
	128	Not supported	Not supported	Not supported
	256	Not supported	Not supported	Not supported
10 SU form factor backplane width				
FB+ 1	32	Required	Required	Required
	64	Optional	Optional	Optional
	128	Optional	Not supported	Not supported
FB+ 2	32	Not supported	Required	Not supported
	64	Not supported	Optional	Not supported
	128	Not supported	Not supported	Not supported
	256	Not supported	Not supported	Not supported
Triplicated control lines		Not supported	Not supported	Required
Split transactions				
Requesters		Optional	Optional	Optional
Responders		Optional	Optional	Optional
Locked operation		Optional	Optional	Optional
Lock commands				
Mask & Swap		Required[b]	Required[b]	Required[b]
Compare & Swap		Required[b]	Required[b]	Required[b]
Fetch & Add Big		Optional	Optional	Optional
Fetch & Add Little		Optional	Optional	Optional
Broadcast				
Masters		Optional	Optional	Optional
Slaves		Optional	Optional	Optional
Broadcall				
Masters		Not supported	Not supported	Not supported
Slaves		Not supported	Not supported	Not supported
Cache coherence		Optional	Optional	Optional

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Table 4-5—Profile S logical layer requirements *(continued)*

Function	Single Futurebus+	Dual Futurebus+	Error Correcting Futurebus+
Message passing	Optional	Optional	Optional
Packet mode	Optional	Optional	Optional
Transaction types[c]			
Read Unlocked	Required	Required	Required
Write Unlocked	Required	Required	Required
Address-Only Unlocked	Required	Required	Required
Locked			
Read Locked	Optional	Optional	Optional
Write Locked	Optional	Optional	Optional
Address Only Locked	Optional	Optional	Optional
Read partial	Optional	Optional	Optional
Write partial	Optional	Optional	Optional
Read Partial Locked	Optional	Optional	Optional
Write Partial Locked	Optional	Optional	Optional
Cache Coherent:[d]			
Write Response	Optional*	Optional*	Optional*
Read Response	Optional*	Optional*	Optional*
Write No-acknowledge	Optional*	Optional*	Optional*
Read Invalid	Optional*	Optional*	Optional*
Write Invalid	Optional*	Optional*	Optional*
Read Shared	Optional*	Optional*	Optional*
Copyback	Optional*	Optional*	Optional*
Read Modified	Optional*	Optional*	Optional*
Invalidate	Optional*	Optional*	Optional*
Shared Response	Optional*	Optional*	Optional*
Modified Response:	Optional*	Optional*	Optional*
Tag bits[e]			
Modules	Not supported	Not supported	Not supported
Backplanes	Not supported	Not supported	Not supported
Serial Bus			
Modules SB-1	Required	Required	Required
SB-2	Optional	Required	Required
Backplanes SB-1	Required	Required	Required
SB-2	Optional	Required	Required
Utility signals			
Modules	Optional	Optional	Optional
Backplanes	Optional	Optional	Optional

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Table 4-5—Profile S logical layer requirements *(continued)*

Function	Single Futurebus+	Dual Futurebus+	Error Correcting Futurebus+
Error detection[f]			
BP: Even Parity	Required	Required	Not supported
Error Correcting Code[g]	Not supported	Not supported	Required
CP: Even Parity	Required	Required	Not supported
Error Correcting Code	Not supported	Not supported	Required
ABP: Even Parity	Optional	Optional	Not supported
Error Correcting Code	Not supported	Not supported	Optional
Protocol Monitoring[h]	Required (L0-opt)		
Parallel Protocol Handshake	Optional (L0-opt)		
Arbitrated Messages	Optional (L0-opt)	Required (L0-opt)	Required
Synchronization	Required (L0-opt)	Optional (L0-opt)	Optional
Preemption	Required (L0-opt)	Optional (L0-opt)	Optional
Request and Grant	Required (L0-opt)	Required (L0-opt)	Required
End of Tenure	Not supported	Required (L0-opt)	Required
GC: Error Correcting Code	Required	Required (L0-opt)	Required
Geographical Addr Parity[i]		Not supported	Required
Duplicated Signals[j]		Required	Required
TED	Required (L0-opt)	Required (L0-opt)	Required
SLD	Required (L0-opt)	Required (L0-opt)	Required
RED	Required (L0-opt)	Required (L0-opt)	Required
Reflected Protection[k]			
CM	Required (L0-opt)	Required (L0-opt)	Required
ST	Required (L0-opt)	Required (L0-opt)	Required
RF	Required (L0-opt)	Required (L0-opt)	Required
Timeout:[l]			
Transaction	Required (L0-opt)	Required (L0-opt)	Required
Split Transaction[m]	Optional (L0-opt)	Optional (L0-opt)	Optional
Arbitration	Required (L0-opt)	Required (L0-opt)	Required
Central Arbiter	Required (L0-opt)	Required (L0-opt)	Required
Distributed Arbitration	Optional (L0-opt)	Optional (L0-opt)	Optional
Bus Activity	Required (L0-opt)	Required (L0-opt)	Required
Error isolation, logging, and diagnostics			
Logging all detected errors[n]	Required (L0-opt)	Required (L0-opt)	Required
Enable/Disable transceivers	Required (L0-opt)	Required (L0-opt)	Required
MAINT_MONITORS	Required (L0-opt)	Required (L0-opt)	Required
Diagnostic data registers	Required (L0-opt)	Required (L0-opt)	Required
Critical reg write protection	Required (L0-opt)	Required (L0-opt)	Required
Error removal and recovery			
Hardware Retry[o]	Required (L0-opt)	Required (L0-opt)	Required
Software Retry[p]	Optional	Optional	Optional
Spare Lines[q]	Not supported	Not supported	Optional
Dual Buses	Not supported	Required	Not supported
CSRs per Clause 9	Required	Required	Required

[a]Arbitration is not necessary for slave-only modules.

[b] If Locked Operation is implemented, these lock commands are required.

[c]CSRs must be accessible while waiting for a split response, i.e., CSR access should not return busy.

[d]* —For Cache Coherent Implementations.

[e]No pinout location defined in this profile.

[f]If Distributed Arbitration is used, ABP, arbitrated message, distributed arbitration timeout, and synchronization options are required except those marked “L0-opt”.

[g]Error correcting codes are defined in this profile.

[h]Protocol monitoring is defined in IEEE Std 896.9-1994.

[i]Geographical Address Parity is defined in IEEE Std 896.9-1994.

[j]Duplicated Signals are defined in IEEE Std 896.9-1994.

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[k]Reflected protection is defined in IEEE Std 896.9-1994.
[l]Timeouts are defined in ISO/IEC 10857: 1994, IEEE Std 896.2-1991, and IEEE Std 896.9-1994.
[m]If split transactions are used, timeout is also required.
[n]Defined in IEEE Std 896.9-1994.
[o]Hardware Retry is defined in IEEE Std 896.9-1994.
[p]Software Retry is defined in IEEE Std 896.2-1991.
[q]Spare lines and dual buses are defined in this profile.

4.4 Profile S interoperability

SEM-E Stretch and 10 SU modules may be designed to work in other profile systems that utilize similar logical and the same physical (mechanical and electrical) definitions. When designing a module that is to be compliant with multiple profiles, one must carefully compare the logical functions.

Table 4-6—Profile S physical layer requirements

Function	10 SU	SEM-E Stretch	Mandate
Module	IEEE Std 1101.3-1993	IEEE Std 1101.7-1995	
Height	215 mm (8.465 in)	150 mm (5.880 in)	Required
Depth	162 mm (6.375 in)	218 mm (8.570 in)	Required
Module pitch	IEEE Std 1101.3-1993	IEEE Std 1101.7-1995	
Slot width	20 mm (0.787 in)	19 mm (0.750 in)	Required
Connector type[a]	IEEE Std 1101.3-1993	IEEE Std 1101.7-1995	
Power			Required
Signal			Required
Keying			Required
Module connector pinout[b]	IEEE Std 896.10-1997	IEEE Std 896.10-1997	
Single Futurebus+			Required
Dual Futurebus+			Optional
Error Correcting Futurebus+			Optional
Digital Power			Required
IEEE 1394 Serial Bus			Required
Utility signals			Required
MIL STD-1553B			Optional
Local interconnects			Optional
User-Defined I/O			Optional
Fiber			Optional
Central arbitration			Required
Distributed arbitration			Optional
28 V			Optional[c]
Backplane connector pinouts	IEEE Std 896.10-1997	IEEE Std 896.10-1997	
Single Futurebus+			Required
Dual Futurebus+			Optional
Error Correcting Futurebus+			Optional
Digital Power			Required
IEEE 1394 Serial Bus			Required
Utility			Required
MIL-STD-1553B			Optional
Local interconnects			Optional
User-Defined I/O			Optional
Fiber			Optional
Central arbitration			Required
Distributed arbitration			Optional[d]
28 V			Required

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Table 4-6—Profile S physical layer requirements *(continued)*

Function	10 SU	SEM-E Stretch	Mandate
Module header	IEEE Std 1101.3-1993	IEEE Std 1101.7-1995	Optional
Insertion/Extraction levers or holes	IEEE Std 1101.3-1993	IEEE Std 1101.7-1995	Required
Backplane electrical	IEEE Std 896.10-1997	IEEE Std 896.10-1997	
Power supply			3.3 V ± 5%
Supply/Reference			2.1 V ± 5%
Output low (V_{ol} max.) (FB+)			1.1 V
Output low (V_{ol} min.) (FB+)			0.2 V
Output high (V_{oh} min.) (FB+)			2.0 V
Output high (V_{oh} max.) (FB+)			3.0 V
Input low (V_{il} min.) (FB+)			1.3 V
Input low (V_{il} max.) (FB+)			1.45 V
Threshold voltage (FB+)			1.55 V
Input high (V_{ih} min.) (FB+)			1.65 V
Input high (V_{ih} max.) (FB+)			1.8 V
Output low (V_{ol} max.) (TTL)			0.4 V
Output low (V_{ol} min.) (TTL)			
Output high (V_{oh} min.) (TTL)			
Output high (V_{oh} max.) (TTL)			2.4 V
Input low (V_{il} min.) (TTL)			
Input low (V_{il} max.) (TTL)			0.8 V
Threshold voltage (TTL)			
Input high (V_{ih} min.) (TTL)			2.0 V
Input high (V_{ih} max.) (TTL)			
Backpanel impedance (unloaded)			67 Ω
Transceiver loading[e]			< 7pF
Mechanical pitch	20 mm (0.787 in)	19 mm (0.75 in)	
Electrical pitch[f]	40 mm (1.574 in)	38 mm (1.5 in)	
Push-Pull signals			
Electrical pitch	20 mm (0.787 in)	19 mm (0.75 in)	
Wire-or signals			
Signal transceivers[g]	IEEE Std 896.10-1997	IEEE Std 896.10-1997	
Wire-Or termination			33 Ω
Push-Pull termination			Active to 2.1 V, 1.0 V
Module loading	IEEE Std 896.10-1997	IEEE Std 896.10-1997	
Stub length L_{stub}			51 mm (2 in) max.
Stub impedance Z_{stub}			67 Ω
Environment performance	IEEE Std 1156.4-1997	IEEE Std 1156.4-1997	
Nonoperating			Level I min.
Operating—Thermal			Level I min.
Mechanical			Level I min.
Op./Nonop.-humidity/pressure			Level I min.
Radiation			Level I min.
Conduction cooling	IEEE Std 1101.3-1993	IEEE Std 1101.7-1995	Required
Module/Backplane keying	IEEE Std 1101.3-1993	IEEE Std 1101.7-1995	Required
User-Defined I/O[h]			Optional

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Table 4-6—Profile S physical layer requirements *(continued)*

Function	10 SU	SEM-E Stretch	Mandate
Module voltages and power[i]	IEEE Std 896.10-1997	IEEE Std 896.10-1997	
5 V			Optional
3.3 V			Optional
2.1 V			Optional
28 V			Optional
Backplane voltages and power[i]	IEEE Std 896.10-1997	IEEE Std 896.10-1997	
5 V			Required
3.3 V			Required
2.1 V			Required
28 V			Required
Live insertion	IEEE Std 896.2-1991	IEEE Std 896.2-1991	Not supported

[a]1 A max. per pin.
[b]User shall implement exactly one of the following: A Single Futurebus+, a Dual Futurebus+, or an Error Correcting Futurebus+.
[c]Pins reserved.
[d]Recommended.
[e]Goal: 5 pF.
[f]Folded backpanel.
[g]15 pF max. load.
[h]Connector Sections C through H.
[i]Product specification shall state voltages and currents required under all specified environmental conditions.

4.5 Conformance testing

The conformance test requirements of IEEE Std 896.4-1993 shall be used for the conformance test requirements of this standard wherever applicable.

IEEE Std 896.4-1993 defines the conformance test requirements for the protocols identified in ISO/IEC 10857: 1994 and IEEE Std 896.2-1991 for Futurebus+ modules, backplanes, and systems. It does not address any of the extensions in the IEEE Std 896.9-1994 Fault Tolerance Extensions or those in this standard. Similar conformance testing to cover these extensions should be used.

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5. Detailed specification, Futurebus+ logical layer

This clause provides the detailed explanations and requirements of the Futurebus+ logical layer summarized in Table 4-5.

5.1 Arbitration

Arbitration applies only to modules that are not slave-only.

5.1.1 Central arbitration

All Profile S modules and backplanes that are not slave-only shall support the central arbitration mechanism specified in Clauses 4 and 5 of ISO/IEC 10857: 1994. Modules may implement up to 256 different priority levels. A Profile S backplane may contain wiring for one or more central arbiters, but is only required to reserve the central arbitration pins at the module level. A Profile S system is not required to contain a central arbiter.

Modules that modify their arbitration priority “on the fly” via arbitrated messages shall do so in a way that does not delay their ability to arbitrate. Use of any arbitrated messages is optional.

5.1.2 Distributed arbitration

In some applications, distributed arbitration is preferred. Distributed arbitration as defined in Clause 5 of ISO/IEC 10857: 1994 may be implemented optionally. The mechanism for switching between central and distributed arbitration is controlled by enabling and disabling the arbitration control registers in the CSRs and/or via arbitrated messages.

At initialization, systems that have a central arbiter shall assert the preemption signal (**PE***), otherwise arbitration is distributed. Systems capable of both central and distributed arbitration may be configured by the monarch during the configuration process or at run time to use either arbitration mechanism. System integrators shall ensure only one mechanism is employed at a time.

5.2 Parallel protocol

Clause 6 of ISO/IEC 10857: 1994 specifies the Futurebus+ parallel protocol. The protocol supports 32 or 64 bits of address and 32, 64, 128, or 256 bits of data. SEM-E Stretch modules shall implement 32-bit addressing and may optionally implement 64-bit addressing. SEM-E Stretch modules shall implement 32-bit data capability and may optionally implement 64-bit data capability. One hundred twenty-eight or 256 bit data widths are not supported by SEM-E Stretch modules. 10 SU modules shall implement 32-bit addressing and may optionally implement 64-bit addressing. All 10 SU modules shall implement 32-bit data capability and may optionally implement 64-bit or 128-bit data capability. Two hundred fifty-six bit data widths are not supported by 10 SU modules.

SEM-E Stretch and 10 SU modules shall declare their supported bus widths in the **MODULE_LOGICAL_CAPABILITY** register as defined in ISO/IEC 10857: 1994, 7.1.2.1.1. For compatibility with other profiles and each other, SEM-E Stretch and 10 SU modules shall default to 32-bit data path width.

SEM-E Stretch backplanes shall be bused and terminated for data path widths of 32-bits. SEM-E Stretch 64-bit backplanes are optional for a Single Futurebus+ system. 10 SU backplanes shall be bused and terminated for data path widths of 64-bits. 10 SU 128-bit backplanes are optional for a Single Futurebus+ system.

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Clause 2 of ISO/IEC 10857: 1994 describes the Futurebus+ signal requirements. Conformance to this profile requires implementation of the full signal set (i.e., signals listed in Table 2-1 of ISO/IEC 10857: 1994) with the exception of Tag Bits and Tag Parity.

5.2.1 Transaction types

Profile S modules can support any combination of the parallel transaction types needed for a specific module's functions. A module shall assert beat error (**BE***) and record a capability error in the CSR error register when specifically addressed with a transaction for which it has no capability.

Following is the list of possible transactions:

- Read Unlocked
- Write Unlocked
- Address Only Unlocked
- Read Locked
- Write Locked
- Address Only Locked
- Read Partial
- Write Partial
- Read Partial Locked
- Write Partial Locked
- Write Response
- Read Response
- Write No Acknowledge
- Read Invalid
- Write Invalid
- Read Shared
- Copyback
- Read Modified
- Invalidate
- Shared Response
- Modified Response

Use of busy: Modules should use **busy** status only to indicate that resources are full or in use. A module shall not assert **busy** to postpone a read response. It should limit the number of outstanding read requests so its return-data buffer space cannot overflow.

Use of splits: Transactions may be split. Split transaction responses shall not be split. All CSRs shall be accessible while waiting for a split response. Splits shall not be initiated by masters.

Packet mode: Profile S modules may optionally use packet mode.

5.2.2 Cache coherence

Cache coherence is an option for Profile S modules. If a module is designed to support cache coherence, it may operate in 32-bit data width or 64-bit data width. Modules that do not support cache transactions shall lie outside the cache coherence domain of the system and not take part in transactions involving cache coherence protocols. All Profile S modules that implement backplane cache coherence shall implement the full cache coherence protocols and all relevant transaction types. System implementors are responsible for correct interoperation between the modules within and outside the cache coherence domain. Only one cache line width should be used per cache domain.

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5.2.3 Message passing

Message passing is optional for Profile S modules and systems. If modules with and without message passing are mixed in a system, modules not supporting message passing shall not take part in transactions involving message passing protocols. System implementors are responsible for correct interoperation between modules with and without message passing capability.

5.2.4 Tag bits

Profile S modules are not required to implement, use, or respond to Tag Bits or Tag Parity. Profile S systems or modules shall not rely on Tag Bits for correct operation.

NOTE—If Tag Bits are used, their function may be incompatible with that of the same signals from another module that is still compliant with Profile S. System implementors should ensure that modules employ Tag Bits in a compatible and interoperable manner.

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6. Utility Signals

Utility Signals are discrete lines used to distribute information where there is a unique requirement that cannot be satisfied by use of the Futurebus+ or the Serial Bus. Examples include low latency requirements or support for special radiation hardened hardware. Reservation of the pin assignments of the Utility Signals is required and, if the functions are implemented, they shall be implemented in accordance with this standard.

Functional Utility Signals are duplicated in the Dual Futurebus+ and triplicated in the Error Correcting configurations. Test Utility signals are not duplicated in any configuration. The Utility Signals are specified below.

6.1 Trigger 0 (TR0*) and Trigger 1 (TR1*)

Trigger 0 (**TR0***) and Trigger 1 (**TR1***) are discretes that may be programmed to be driven by any module(s). Any module may monitor these triggers. The action that a module takes upon receipt of a trigger signal is programmed via the Futurebus+ (**TR0*** only) or the Serial Bus (**TR0*** and **TR1***). Typical functions accomplished with a trigger are stopping or starting a collection of processors in a precise time-synchronized fashion and relating events in different modules by triggering the trace stack resources.

TR0* and **TR1*** signals shall be active low for a minimum of 50 ns.

TR0* and **TR1*** are not duplicated in the Dual Futurebus+ or the Error Correcting configurations.

6.2 Run (RUN*)

Run (**RUN***) is a discrete signal that shall cause the processor to go to a run mode only when it transitions from an inactive to an active level. Holding the **RUN*** signal at an active level shall not keep the processor in run mode if a Stop is generated during this time. The **RUN*** discrete has the same effect as a write to the **CONTINUE_EXECUTION** bit in the **UCIF_CONTROL** register.

RUN* shall be active low for a minimum of 50 ns.

RUN* is not duplicated in the Dual Futurebus+ or the Error Correcting configurations.

6.3 Nuclear Event Detect (NED*)

The assertion of **NED*** indicates that a nuclear event has occurred and that circumvention of TREE (Transient Radiation and its Effects on Electronics) should be initiated. A nuclear event may be natural (solar flare) or man-made. It is intended that the circumvention be accomplished by (1) draining all power supplies and other modules, if necessary, (2) having the Nuclear Event Detection module initiate hardened timers and set hardened CSRs for the purpose of restarting power, (3) restarting the system hardware, (4) restarting the system software, and (5) distinguishing between power and input/output glitches that are associated with the nuclear event. In systems implementing **NED*** shutdown, system start-up software should poll a hardened standard unit address to determine if the start-up is due to recovery from an **NED*** or for other reasons. The location of these various hardened elements is user-configurable and beyond the scope of this standard. If any elements of the TREE circumvention are on a Profile S module, it is expected they will use the **NED*** signal in their operation. Typically non-TREE circumvention logic on Profile S modules may use an active **NED*** to disable all outputs or hold all logic in reset.

NED* shall be an active low signal. **NED*** shall be asserted only by a Nuclear Event Detection module for a minimum of 50 ns. It shall use TTL levels instead of FB+ to enable it to be driven from a source that may not have access to FB+ transceivers.

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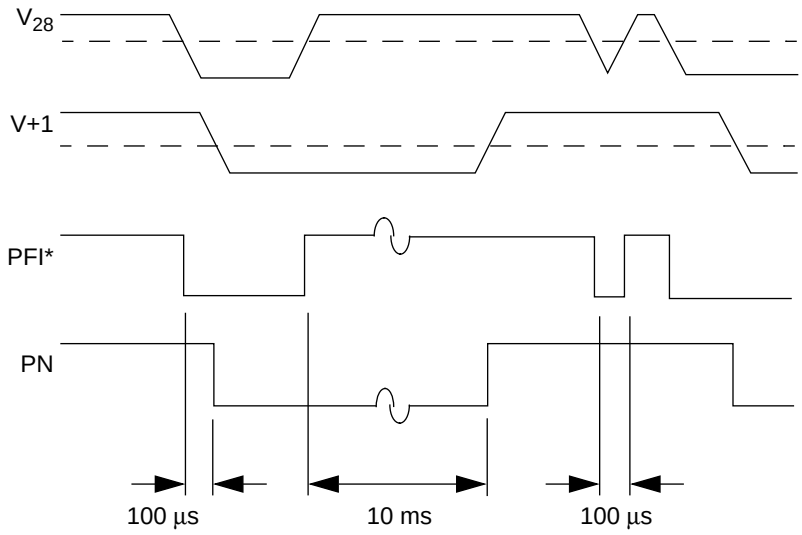
All logic associated with detecting, generating, and distributing this signal in a Nuclear Event Detection module should be hardened against radiation upset to the expected level of the Nuclear Event (most likely level IVa of IEEE Std 1156.4-1997), otherwise this signal may be invalid.

NED* is duplicated in the Dual Futurebus+ configuration. These signals are designated **1-NED*** and **2-NED***. When the Dual Futurebus+ is used, the module shall be configurable to accept either or both **1-NED*** or **2-NED***, depending upon which bus is active.

NED* is triple modular redundant in the Error Correcting configuration. These signals are designated **NED***, **NEDA***, and **NEDB***. At least two of these three signals must be active to indicate that a nuclear event has occurred.

6.4 Power Failure Imminent (PFI*)

The assertion of **PFI*** indicates that input power to the power supply or to the power conditioning unit is not within acceptable ranges and that the power supply output may consequently fall out of regulation (see Figure 6-1). Regulated power supply output voltage at rated current shall be available for at least 100 µs after the assertion of **PFI***. **PFI*** shall be released upon recovery of nominal power supply input power, provided that **PFI*** has been asserted for a minimum of 100 µs. **PFI*** shall not be asserted for less than 100 µs. It shall use TTL levels instead of FB+ to enable it to be driven from a power supply that may not have access to FB+ transceivers.



NOTE—Dotted line represents the power supply output threshold voltage.

Figure 6-1—Power supply monitoring signal

PFI* shall be an active low signal that is usually asserted by the power supply.

PFI* is duplicated in the Dual Futurebus+ configuration. These signals are designated **1-PFI*** and **2-PFI***. When the Dual Futurebus+ is used, the module shall be configurable to accept either or both **1-PFI*** or **2-PFI***, depending upon which bus is active.

PFI* is triple modular redundant in the Error Correcting configuration. These signals are designated **PFI***, **PFIA***, and **PFIB***. At least two of these three signals must be active for a module to recognize **PFI*** as active.

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6.5 Power Normal (PN)

This discrete is an active high wire or signal. It shall use TTL levels instead of FB+ to enable it to be driven from a power supply that may not have access to FB+ transceivers. Power Normal is active when dc power has stabilized and stays within the voltage tolerances (see Figure 6-1). Power Normal is inactive while dc power is coming up and until dc power has stabilized for at least 10 ms. At that time, the Power Normal signal shall become active. The Power Normal signal shall remain active until a voltage-out-of-tolerance condition occurs and that causes Power Normal to go inactive. Power Normal shall provide the Futurebus+ modules with a constant reset while power is coming up and holds a constant reset while power is going down.

The Power Normal discrete is active high and is normally generated by the power supply that monitors the dc regulators and the input power. If no regulated power is supplied on a backplane, **PN** shall remain inactive.

PN is duplicated in the Dual Futurebus+ configuration. These signals are designated **1-PN** and **2-PN**. When the Dual Futurebus+ is used, the module shall be configurable to accept either or both **1-PN** or **2-PN**, depending upon which bus is active.

PN is triple modular redundant in the Error Correcting configuration. These signals are designated **PN**, **PNA**, and **PNB**. At least two of these three signals must be active for a module to recognize **PN** as active.

6.6 System Reset (SR*)

The System Reset signal provides a way to tell a module to run an abbreviated reset instead of a full reset such as after the receipt of an active Power Normal (**PN)**. It shall use TTL levels instead of FB+ to enable it to be driven from a power supply or other source that may not have access to FB+ transceivers. If System Reset is desired, the System Reset discrete shall be held active for a minimum of 10 μs.

SR* shall be active low.

SR* is duplicated in the Dual Futurebus+ configuration. These signals are designated **1-SR*** and **2-SR***. When the Dual Futurebus+ configuration is used, the module shall be configurable to accept either or both **1-SR*** or **2-SR***, depending upon which bus is active.

SR* is triple modular redundant in the Error Correcting configuration. These signals are designated **SR***, **SRA***, and **SRB***. At least two of the these three signals must be active for a module to recognize **SR*** as active.

6.7 Utility Spares (UPSP* and UWSP)

Two spare pins are provided in the Error Correcting configuration to cover the following utility signals: **NED***, **NEDA***, **NEDB***, **PN**, **PNA**, **PNB**, **PFI***, **PFIA***, **PFIB***, **SR***, **SRA***, and **SRB***. **UPSP*** covers the push-pull TTL signals (**NED***, **NEDA***, **NEDB***, **PFI***, **PFIA***, **PFIB***, **SR***, **SRA***, and **SRB*)**. **UWSP** covers the wire-OR TTL signals **(PN**, **PNA**, and **PNB).** These pins are selected to replace an active line using the **SPARE_UTILITY_PP** and **SPARE_UTILITY_WW** bits in **SP_ENABLE_SPARES_I** CSR 680. **UPSP*** and **UWSP** are implemented only for Error Correcting configurations.

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7. Fault tolerance aspects of the parallel protocol and utility signals

A common requirement for any space system is some level of fault tolerance. This is usually allocated from the top down as the system is designed and defined. Since fault tolerance is but one aspect of a system that is traded at each level of the hierarchy, by the time one reaches the backplane bus such as Futurebus+, allocations and strategies may already be in place to handle errors at a higher level. On the other hand, recovery latency requirements may be such that an error must be removed rapidly and thus require some form of error removal at the bus level. Profile S provides the bus with mechanisms to support a spectrum of fault tolerance applications from simply detecting and logging errors to operating through errors. An application designer must decide which is appropriate for his or her system and then specify and implement that level of fault tolerance. See Clause 1 of IEEE Std 896.9-1994 for a detailed discussion of the various fault tolerance applications supported by this profile. A subset of this capability of the Single Futurebus+ and Dual Futurebus+ configuration named Level 0 is allowed. These are marked throughout this clause.

7.1 Error detection

All of the aforementioned fault tolerance applications rely on near-100% detection of errors in order to know when an error has occurred so that appropriate action can be taken. A system that does not detect its errors cannot be termed fault tolerant of those errors. IEEE Std 896.9-1994 guarantees near-100% detection of errors on a Futurebus+ and is used as the basis for this document's fault tolerance applications. The following subclauses describe the Futurebus+ error detection mechanisms that are part of one or more fault tolerance applications.

7.1.1 Even parity

In all fault tolerance applications except the Error Correcting configuration, Profile S modules shall use parity to protect the Address/Data lines (**AD[31..0]***, **AD[63..0]***, or **AD[127..0]***) and Command lines (**CM[7..0]***) as defined in IEEE Std 896.9-1994.

In all fault tolerance applications implementing distributed arbitration except the Error Correcting configuration, Profile S modules shall use even parity to protect the arbitrated message lines (**AB[7..0]***) as defined in IEEE Std 896.9-1994.

All Profile S modules shall use even parity to protect the Geographic Address (**GA[5..0]***) as defined in IEEE Std 896.9-1994.

All Profile S Error Correcting configuration modules shall use even parity to protect the Bus Grant Code lines (**GC[5..0]***).

7.1.2 Error correcting codes

The error correction codes and techniques used provide for the detection of all single line errors (as defined in 7.1.3 and 7.1.4) and their correction with no software intervention. The techniques and codes used provide at least single error detection and correction for each of the lines that make up Futurebus+.

These techniques assume that only one bit covered by a checker can fail and be corrected. These techniques place no additional electrical requirements on the Futurebus+ specification. To ensure that there are no single points of failure from the input of the bus driver to the output of the bus receiver, partitioning to driver and receiver should be made such that a single enable line controls only one driver or receiver in a check group. All mechanisms are initialized in the disabled state. Each mechanism is enabled by its corresponding CSR. Upon detection of an error, bits in the corresponding CSR are set indicating failure type and syndrome of the error. The error CSRs can be cleared by the module software.

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All Error Correcting configuration Profile S modules shall use error correcting codes to protect the 32-bit Address/Data **AD[31..0]*** with the Bus Code lines **BC[7..0]***, and the Command lines **CM[7..0]*** with the Command Code lines **CC[4..0]***.

Additionally, if a 64-bit Address/Data module is implemented, the module shall use the Bus Code lines **BC[7..0]*** to protect **AD[63..0]*** (10 SU only).

If distributed arbitration is implemented in an Error Correcting configuration Profile S module, the Arbitrated Message **AB[7..0]*** shall be protected by the Arbitrated Bus Code **ABC[4..0]***.

7.1.2.1 Sixty-Four-Bit SEC/DED/SBD

To provide single fault detection and correction for data and detection of b-bit symbol faults (b is the variable length of the symbol detection capability), single error correction, and double error detection with single b-bit symbol detection (SEC-DED-SbBD) codes, are used as the standard methods. The (72,64) code has been widely used throughout industry since the number of check bits required equal the number of parity bits typically used for this size data structure. The (72,64) code used here also provides detection of 3-bit byte or 4-bit byte failures. In addition, this code seems to provide the optimal balance between signal lines and internal logic complexity. For this reason, even with wider data structures, the code is generated on 8-byte boundaries.

The parity check matrix is given by Tables 7-1 and 7-2. Correctable and uncorrectable errors shall be indicated by storing a code in the corresponding CSR (**SP_TMR_HOLD_I** (CSR 456), or **SP_TMR_HOLD_II** (CSR 460)) for each type of failure. The syndrome of the failure shall be stored in a CSR (**SP_ECC_HOLD** (CSR 452)).

This code does not detect all triple or four bit errors, only those that occur within symbols. From the three-bit point of view **D63**..**D61**, **D60**..**D58**, ..., B**C2**..B**C0** should be wired as symbols on a module. All three-bit errors within a symbol will be detected. From the four-bit point of view **D63**..**D60**, **D59**..**D56**, ..., B**C3**..B**C0** should be wired as symbols on a module. All four-bit errors within a symbol will be detected. In a 32- or 64-bit system, it is not possible to get full 8- or 9-bit symbol detection.

Note that Profile S does not support an Error Correcting 128- or 256-bit configurations. In all cases, controls and other common logic should be divided into separate signals at the highest level of full symbol coverage as early as possible to have the highest detection probabilities.

Table 7-1—Parity check matrix of Odd-Weight-Column (72,64) SEC-DED code

Syndrome bit	D63 ... D56	D55 ... D48	D47 ... D40	D39 ... D32	D31 ... D24
7	11111111	11111111	+++1+++1	+++1+++1	++1+++1+
6	1+++1+++	1+++1+++	11111111	11111111	+++1+++1
5	+1+++1++	+1+++1++	1+++1+++	1+++1+++	11111111
4	++1+++1+	++1+++1+	+1+++1++	+1+++1++	1+++1+++
3	+++1+++1	+++1+++1	++11++11	++11++11	+111+111
2	++++1111	++++1111	++++1111	++++1111	++++1111
1	++++++++	11111111	++++++++	11111111	++++++++
0	1111++++	++++1111	111++++1	+++1111+	11++++11

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Table 7-2—Parity check matrix of Odd-Weight-Column (72,64) SEC-DED code

Syndrome bit	D23 ... D16	D15 ... D08	D07 ... D00	BC7 ... BC0
7	++1+++1+	+++1+++1	+++1+1++	1+++++++
6	+++1+++1	1+++1+++	1+++++1+	+1++++++
5	11111111	+1+++1++	+1+++++1	++1+++++
4	1+++1+++	++1+++1+	++1+1111	+++1++++
3	+111+111	++++++++	++++1111	++++1+++
2	++++1111	11111111	++++++++	+++++1++
1	11111111	1111++++	11111111	++++++1+
0	++1111++	++++1111	1111+111	+++++++1

7.1.2.2 Eight-Bit SEC/DED

For the 8-bit wide buses over which Error Correcting configuration (ECC) codes are to be used (such as the arbitrated message bus), a full 5-bit Odd-Weight-Column single error correction/double error detection code shall be used.

A full 5-bit Odd-Weight-Column single error correction/double error detection code will also provide detection of a full 8-bit symbol error over the data or two 4-bit symbol errors over the data, along with a 5-bit symbol error over the ECC code. The parity check matrix is given by Table 7-3. Correctable and uncorrectable errors shall be indicated by storing a code in the corresponding CSR [**SP_TMR_HOLD_I** (CSR 456), or **SP_TMR_HOLD_II** (CSR 460)] for each type of failure. The syndrome of the failure shall be stored in a CSR [**SP_ECC_HOLD** (CSR 452)].

Table 7-3—Parity check matrix of Odd-Weight-Column (13,8) SEC-DED code

Syndrome bit	D07 ... D00	xC4 ... xC0
4	111+1+1+	1++++
3	1111+++1	+1+++
2	++1111++	++1++
1	1+++1111	+++1+
0	+1+1+111	++++1

7.1.3 Triple modular redundant (TMR) lines

Triple modular redundancy is guaranteed to detect all single bit errors on lines that are covered by it. In this method, comparisons are made in groups of two of the three lines by sampling the signals after the end of the glitch filter period and after the skew between lines has settled out. The value agreeing on two of the three lines is assumed to be the correct value for those lines.

Profile S modules that choose to implement the Error Correcting configuration shall protect the following signals through the use of two extra copies of each signal:

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- Status **ST[7..0]*** shall be protected with **STA[7..0]*** and **STB[7..0]***.
- Capability **CA[2..0]*** shall be protected with **CAA[2..0]*** and **CAB[2..0]***.
- Address Handshakes **AS***, **AK***, and **AI***, shall be protected with **ASA***, **ASB***, **AKA***, **AKB***, **AIA***, and **AIB***.
- Data Handshakes **DS***, **DK***, and **DI***, shall be protected with **DSA***, **DSB***, **DKA***, **DKB***, **DIA***, and **DIB***.
- End of Tenure **ET*** shall be protected with **ETA*** and **ETB***.
- Reset **RE*** shall be protected with **REA*** and **REB***.
- Requests **RQ[1..0]*** shall be protected with **RQA[1..0]*** and **RQB[1..0]***.
- Preemption **PE*** shall be protected with **PEA*** and **PEB***.
- Nuclear Event Detect **NED*** shall be protected with **NEDA*** and **NEDB***.
- Power Normal **PN** shall be protected with **PNA** and **PNB**.
- Power Fail Interrupt **PFI*** shall be protected with **PFIA*** and **PFIB***.
- Warm Start **SR*** shall be protected with **SRA*** and **SRB***.

Profile S modules that choose to implement the Error Correcting configuration and distributed arbitration shall protect the following signals through the use of two extra copies of each signal.

- Arbitrated Message Sync **AP***, **AQ***, and **AR***, shall be protected with **APA***, **APB***, **AQA***, **AQB***, **ARA***, and **ARB***.
- Arbitration Condition **AC[1..0]*** shall be protected with **ACA[1..0]*** and **ACB[1..0]***.

A 2-bit code shall be set in **SP_TMR_HOLD_I** (CSR 456) or **SP_TMR_HOLD_II** (CSR 460) indicating which bit, if any, was in error.

7.1.3.1 TMR module/system considerations

TMR triples the number of signal lines per control signal over a noncorrected implementation. Although capable of detecting and correcting all single bit failures, this method is guaranteed to select the wrong lines on multiple line errors of a given signal without detecting the failure. Thus the module's software needs to take note of a consistently failing line and spare around it if sparing mechanisms (at the bit or bus level) are available, and/or call for replacement of the component causing the error on the bus if they are not.

Implementing an Error Correcting configuration may cost more in unique silicon, I/O, and reduced performance. It is also important that a module that uses the Error Correcting configuration increase its own fault detection and masking capabilities so that the true value of the corrected data handling may be realized throughout the system.

To ensure proper sampling of the signals covered by TMR, the following relation must be satisfied:

$$t_{total} = t_{norm} + t_{comp} + t_{sel} + t_{skew}$$

where

- t_{total} is the total delay that must be accounted for before a signal covered by TMR may be sampled;
- t_{norm} is the maximum delay associated with the signal in a non-TMR implementation;
- t_{comp} is the maximum propagation delay through the comparison logic used in the TMR;
- t_{sel} is the maximum propagation delay through the logic to select one of the three lines;
- t_{skew} is the time difference between the earliest arrival of the fastest TMR line and the latest arrival of the slowest TMR line. Before using any line covered by TMR, this delay must be accounted for.

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7.1.3.2 ECC and TMR registers

The following provides a description of the extensions required for an Error Correcting configuration. These are organized by the signals that are covered.

7.1.3.2.1 Address/Data and bus codes

Two bits (1–0), **ECC_ADDR_ENABLE** from R/W **SP_ENABLE_ECC_TMR** (CSR 660) (see Figure 9-14), control enabling of ECC for these lines as follows:

00 - No ECC - **BC[7..0]*** used for parity as in IEEE Std 896.9-1994. This is the default/reset state.

01 - 32-bit mode: **AD[31..0]*** and **BC[7..0]*** are active, **AD[63..32]*** are forced inactive. Together, **AD[63..0]*** and **BC[7..0]*** form one (72,64) code with a format of FFFFFFFFxxxxxxxx.

11 - 64-bit mode: **AD[63..0]*** and **BC[7..0]*** form one (72,64) code.

Eight bits (7–0) of **BYTE_LANE_IN_ERROR** (CSR 400) are used to store the error syndrome from a 32- or 64-bit bus implementation.

When an error is detected, **BYTE_LANE_IN_ERROR** (CSR 400) shall be frozen and **ECC_TMR_ERROR_DETECTED** shall be set. Writing 1 to clear this bit in **ERROR_HI** (CSR 384) shall unfreeze these syndrome bits.

Bits 6–5, **ECC_72_64_ERROR** of R/C **SP_ECC_HOLD** (CSR 452) (see Figure 9-9), indicate an uncorrectable error on the (72,64) word. Writing 1 to this bit in **SP_ECC_HOLD** (CSR 452) shall clear this bit.

Bits 7–0, **ECC_BC** of R/W **SP_MAINT_MONITOR_ECC** (CSR 664) (see Figure 9-15), are put on **BC[7..0]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. These are initially reset to a released state.

7.1.3.2.2 Command bits and command codes

Bit 2, **ECC_COMMAND_ENABLE** from R/W **SP_ENABLE_ECC_TMR** (CSR 660) (see Figure 9-14), controls enabling of ECC for these lines as follows:

0 - No ECC - **CC[0]*** used for parity as in IEEE Std 896.9-1994. This is the default/reset state.

1 - **CM[7..0]*** and **CC[4..0]*** form (13,8) code word.

Five bits (20–16), **ECC_COMMAND_SYNDROME** of R/C **SP_ECC_HOLD** (CSR 452) (see Figure 9-9), are used to store the error syndrome. When an error is detected, **SP_ECC_HOLD** (CSR 452) shall be frozen and **ECC_TMR_ERROR_DETECTED** shall be set. Writing 1 to clear **ECC_TMR_ERROR_DETECTED** in **ERROR_LOW** (CSR 388) shall unfreeze these syndrome bits. The error syndrome bits shall be cleared by writing a 1 into them in **SP_ECC_HOLD** (CSR 452).

Two bits (25–24), **ECC_COMMAND_ERROR** of R/C **SP_ECC_HOLD** (CSR 452) (see Figure 9-9), indicate the results of the correction. These bits shall be cleared by writing a 1 into them in **SP_ECC_HOLD** (CSR 452).

Bits 18–14, **ECC_CC** of R/W **SP_MAINT_MONITOR_ECC** (CSR 664) (see Figure 9-15), are placed on **CC[4..0]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. These are initially reset to a released state.

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7.1.3.2.3 Status and capability lines

Bit 3, **TMR_ST_CAP_ENABLE** from R/W **SP_ENABLE_ECC_TMR** (CSR 660) (see Figure 9-14), controls enabling of TMR for these lines as follows:

0 - no correction - **ST[7..0]*** and **CA[2..0]*** are used as single lines. **STB[7]*** becomes the **RF*** signal, **STB[6]*** becomes **TED***, and **STB[5]*** becomes **SLD*** as defined in IEEE Std 896.9-1994. This is the default/reset state.
1 - **STA[7..0]*, STB[7..0]*, CAA[2..0]*** and **CAB[2..0]*** provide copies of **ST[7..0]*** and **CA[2..0]*** as described above.

Twenty-two bits (23–2), of R/C **SP_TMR_HOLD_I** (CSR 456) (see Figure 9-10), are used to indicate the status and capability bits in error. A 2-bit code is assigned to each signal line that describes the error.

The codes given result from comparisons made while correction is enabled. These bits are initially reset to an inactive state. Writing 1 into these bits in **SP_TMR_HOLD_I** (CSR 456) shall release these bits.

Bits 7–0, **TMR_ST[7..0]_A** of R/W **SP_MAINT_MONITOR_ST_CAP** (CSR 676) (see Figure 9-18), are placed on **STA[7..0]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted.

Bits 23–16, **TMR_ST[7..0]_B** of R/W **SP_MAINT_MONITOR_ST_CAP** (CSR 676) (see Figure 9-18), are placed on **STB[7..0]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted.

Bits 10–8, **TMR_CA[2..0]_A** of R/W **SP_MAINT_MONITOR_ST_CAP** (CSR 676) (see Figure 9-18), are placed on **CAA[2..0]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted.

Bits 26–24, **TMR_CA[2..0]_B** of R/W **SP_MAINT_MONITOR_ST_CAP** (CSR 676) (see Figure 9-18), are placed on **CAB[2..0]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted.

These are initially reset to an inactive state.

7.1.3.2.4 Synchronization lines

The “A” and “B” copies of these signals (**AIA***, **AKA***, **ASA***, **DIA***, **DKA***, **DSA***, **ETA***, and **AIB***, **AKB***, **ASB***, **DIB***, **DKB***, **DSB***, **ETB***) are used in the TMR voting.

Bit 4, **TMR_SYNCH_ENABLE** from R/W **SP_ENABLE_ECC_TMR** (CSR 660) (see Figure 9-14), controls enabling of TMR for these lines as follows:

0 - no correction - These lines are used as single lines. This is the default/reset state.
1 - The replica copies of the synchronization lines are provided as described above.

Fourteen bits (13–0) of R/C **SP_TMR_HOLD_II** (CSR 460) (see Figure 9-11) are used to indicate the synchronization bits in error. A 2-bit code is assigned to each signal line that describes the error.

The codes given above result from comparisons made while correction is enabled. These bits are initially reset to an inactive state. Writing a 1 into these bits in **SP_TMR_HOLD_II** (CSR 460) will release these bits.

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Bits 10–4, **TMR_AS/AK/AI/DS/DK/DI/ET_A** of R/W **SP_MAINT_MONITOR_SYNCH_A** (CSR 668), are placed on the A copy of the Synchronization lines when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. Bits 10–4, **TMR_AS/AK/AI/DS/DK/DI/ET_B** of R/W **SP_MAINT_MONITOR_SYNCH_B** (CSR 672) (see Figure 9-17), are placed on the B copy of the Synchronization lines when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted.

7.1.3.2.5 Arbitrated message bus and codes

Bit 5, **ECC_ARB_MESSAGE_ENABLE** from R/W **SP_ENABLE_ECC_TMR** (CSR 660) (see Figure 9-14), controls enabling of ECC for these lines as follows:

0 - No ECC - **ABC[0]*** used for parity as in ISO/IEC 10857: 1994. This is the default/reset state.
1 - **AB[7..0]*** and **ABC[4..0]*** form (13,8) code word.

Five bits (4–0), **ECC_ARB_MESSAGE_SYNDROME** of R/C **SP_ECC_HOLD** (CSR 452) (see Figure 9-9), are used to store the error syndrome. These bits shall be cleared by writing a 1 into these bits in **SP_ECC_HOLD** (CSR 452).

Two bits (27–263), **ECC_ARB_MESSAGE_ERROR** of R/C **SP_TMR_HOLD_II** (CSR 460) (see Figure 9-11), indicate the results of the correction. Writing 1 into these bits in **SP_TMR_HOLD_II** (CSR 460) shall clear these bits.

Bits 23–19, **ECC_ABC** of R/W **SP_MAINT_MONITOR_ECC** (CSR 664) (see Figure 9-15), are placed on **ABC[4..0]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. These are initially reset to an inactive state.

7.1.3.2.6 Arbitration handshake signals

Bit 6, **TMR_ARB_SYNCH_ENABLE** from R/W **SP_ENABLE_ECC_TMR** (CSR 660) (see Figure 9-14), controls enabling of TMR for these lines as follows:

0 - no correction - Synchronization lines are used as single lines. This is the default/reset state.
1 - **APA***, **AQA***, **ARA***, and **APB***, **AQB***, **ARB*** provide copies of **AP***, **AQ***, **AR*** as described above.

Six bits (19..14) of R/C **SP_TMR_HOLD_II** (CSR 460) (see Figure 9-11) are used to store the arbitration synchronization bits in error. A 2-bit code is assigned to each signal line that describes the error.

The codes given result from comparisons made while correction is enabled. These bits are initially reset to an inactive state. Writing 1 into these bits in **SP_TMR_HOLD_II** (CSR 460) will release these bits.

Bits 15–13, **TMR_AP/AQ/AR_A** of R/W **SP_MAINT_MONITOR_SYNCH_A** (CSR 668), are placed on the A copy of the Arbitration Synchronization lines when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. Bits 15–13, **TMR_AP/AQ/AR_B** of R/W **SP_MAINT_MONITOR_SYNCH_B** (CSR 672) (see Figure 9-17), are placed on the B copy of the Arbitration Synchronization lines when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. These are initially reset to an inactive state.

7.1.3.2.7 Arbitrated condition lines

Bit 7, **TMR_ARB_COND_ENABLE** from R/W **SP_ENABLE_ECC_TMR** (CSR 660) (see Figure 9-14), controls enabling of TMR for these lines as follows:

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0 - no correction - **AC[1..0]*** are used as single lines. This is the default/reset state.
1 - **ACA[1..0]*** and **ACB[1..0]*** provide copies of **AC[1..0]*** as described above.

Four bits (23–20) of R/C **SP_TMR_HOLD_II** (CSR 460) (see Figure 9-11) are used to indicate the arbitrated condition bits in error. A two bit code is assigned to each signal line that describes the error.

The codes given result from comparisons made while correction is enabled. These bits are initially reset to an inactive state. Writing 1 into these bits in **SP_TMR_HOLD_II** (CSR 460) shall release these bits.

Bits 12–11, **TMR_AC_0/1_A** of R/W **SP_MAINT_MONITOR_SYNCH_A** (CSR 668), are placed on the A copy of the Arbitrated Message Condition lines when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. Bits 12–11, **TMR_AC_0/1_B** of R/W **SP_MAINT_MONITOR_SYNCH_B** (CSR 672) (see Figure 9-17), are placed on the B copy of the Arbitrated Message Condition lines when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. These are initially reset to an inactive state.

7.1.3.2.8 Reset lines

Bit 8, **TMR_RESET_ENABLE** from R/W **SP_ENABLE_ECC_TMR** (CSR 660) (see Figure 9-14) controls enabling of TMR for these lines as follows:

0 - no correction - **RE*** and **RED*** are used as dual lines. This is the default/reset state.
1 - **REA*** and **REB*** provide copies of **RE*** as described above.

Two bits (25–24), **TMR_RESET_ERROR** of R/C **SP_TMR_HOLD_II** (CSR 460) (see Figure 9-11), are used to store the reset bits in error. A 2-bit code is assigned that describes the error.

The codes given result from comparisons made while correction is enabled. These bits are initially reset to an inactive state. Writing 1 into these bits in **SP_TMR_HOLD_II** (CSR 460) shall release these bits.

7.1.3.2.9 Arbitration requests

Bit 9, **TMR_RQ_ENABLE** from R/W **SP_ENABLE_ECC_TMR** (CSR 660) (see Figure 9-14), controls enabling of TMR for these lines as follows:

0 - no correction - **RQ[1..0]*** are used as single lines. This is the default/reset state.
1 - **RQA[1..0]*** and **RQB[1..0]*** provide copies of **RQ[1..0]*** as described above.

For each set of request lines entering the central arbiter, the following CSRs must be supported.

Four bits (31–28) of R/C **SP_TMR_HOLD_II** (CSR 460) (see Figure 9-11) are used to indicate the request bits in error. A 2-bit code is assigned to each signal line that describes the error.

The codes given result from comparisons made while correction is enabled. These bits are initially reset to an inactive state. Writing 1 into these bits in **SP_TMR_HOLD_II** (CSR 460) shall release these bits.

Bits 3–2, **TMR_RQ_0/1_A** of R/W **SP_MAINT_MONITOR_SYNCH_A** (CSR 668), are placed on **RQA[1..0]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. Bits 3–2, **TMR_RQ_0/1_B** of R/W **SP_MAINT_MONITOR_SYNCH_B** (CSR 672) (see Figure 9-17) are placed on **RQB[1..0]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. These are initially reset to an inactive state.

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7.1.3.2.10 Grant lines and grant codes

Bit 10, **ECC_GRANT_ERROR_ENABLE** from R/W **SP_ENABLE_ECC_TMR** (CSR 660) (see Figure 9-14), in all nodes controls enabling of correction for these lines as follows:

0 - no correction - the **GR*** to each node is solely used for providing grants during central arbitration. This is the default/reset state.
1 - A special code, **GC[5..0]*** is generated that specifies the master on the line according to the above description. **GCP*** is even parity over this code.

Seven bits (15–9), **GRANT_CODE_HOLD** of R/C **SP_ECC_HOLD** (CSR 452) (see Figure 9-9), at each receiving node are used to store the **GC[5..0]*** and **GCP*** as a result of a miscompare while correction is enabled. These bits are initially reset to an inactive state. Writing 1 into these bits in **SP_ECC_HOLD** (CSR 452) shall release these bits.

Three bits (23–21), **ECC_GRANT_ERROR_CORRECTION** of R/C **SP_ECC_HOLD** (CSR 452) (see Figure 9-9), at each receiving node indicate the results of the correction.

These bits are initially reset to an inactive state. Writing 1 into these bits in **SP_ECC_HOLD** (CSR 452) shall release these bits.

Bit 12, **ECC_GRANT_EVEN_PARITY_ENABLE** of R/W **SP_ENABLE_ECC_TMR** (CSR 660) (see Figure 9-14), in the Central Arbiter, will force even parity codes to be generated on **GCP*** when active. Bits 13–8, **ECC_GRANT_GC** of R/W **SP_MAINT_MONITOR_ECC** (CSR 664) (see Figure 9-15), in the Central Arbiter, are placed on **GC[5..0]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. These are initially reset to an inactive state.

7.1.3.2.11 Preempt lines

Bit 11, **TMR_PE_ENABLE** from R/W **SP_ENABLE_ECC_TMR** (CSR 660) (see Figure 9-14), controls enabling of TMR for these lines as follows:

0 - no correction - **PE*** is used as a single line. This is the default/reset state.
1 - **PEA*** and **PEB*** provide copies of **PE*** as described above.

Two bits (1–0), **TMR_PE_ERROR** of R/C **SP_TMR_HOLD_I** (CSR 456) (see Figure 9-10), are used to store the arbitrated condition bits in error. A 2-bit code is assigned that describes the error.

The codes given result from comparisons made while correction is enabled. These bits are initially reset to an inactive state. Writing 1 into these bits in **SP_TMR_HOLD_I** (CSR 456) shall release these bits.

Bit 0, **TMR_PE_A** of R/W **SP_MAINT_MONITOR_SYNCH_A** (CSR 668), is placed on **PEA*** when the **MAINT_MONITOR_ SP_MAINT_MONITOR_SYNCH_B** (CSR 672) (see Figure 9-17), is placed on **PEB*** when the **MAINT ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. Bit 0, **TMR_PE_B** of R/W **_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR, is asserted. These are initially reset to an inactive state.

7.1.4 Duplicated signals

Profile S modules not in the Error Correcting configuration shall duplicate the Reset (**RE***), Select (**SL***), and Transaction Error (**TE***) signals with **RED***, **SLD***, and **TED***, respectively, for each implemented Futurebus+ as defined in IEEE Std 896.9-1994. These duplicated signals are optional in Level 0.

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7.1.5 Reflected protection

All Profile S modules shall implement reflected protection using the Status and Capability fields of each Futurebus+ as defined in IEEE Std 896.9-1994. All Profile S modules not in the Error Correcting configuration shall also be required to implement the Reflected Field (**RF***) signal as defined in IEEE Std 896.9-1994. This reflected protection is optional in Level 0.

7.1.6 Protocol monitoring

Profile S modules shall implement parallel protocol handshake protection as defined in IEEE Std 896.9-1994.

Profile S modules that implement distributed arbitration shall implement protocol monitoring on each bus as defined in IEEE Std 896.9-1994 to protect the arbitrated condition and arbitration synchronization signals.

Profile S modules shall implement protocol monitoring on each bus as defined in IEEE Std 896.9-1994 to protect the preemption and end of tenure lines.

All Profile S central arbiter modules that do not implement the Error Correcting configuration shall use protocol monitoring on the grant lines as defined in IEEE Std 896.9-1994.

Protocol monitoring is optional in Level 0.

7.1.7 Timeouts

All Profile S modules shall implement Transaction, Arbitration, Central Arbitration, and Bus Activity timeouts as defined in ISO/IEC 10857: 1994, IEEE Std 896.2-1991, and IEEE Std 896.9-1994. If Split Transactions are implemented, a Profile S module shall implement the Split Transaction timeout as defined in ISO/IEC 10857: 1994 and IEEE Std 896.2-1991. If Distributed Arbitration is implemented, a Profile S module shall implement the Distributed Arbitration Timeout as defined in IEEE Std 896.9-1994. Timeouts are optional in Level 0.

7.2 Error isolation, logging, and diagnostics

Once an error is detected, some action must be taken. At the simple end of the spectrum, bus activity is stopped, the error is logged, and the bus is marked as bad to all the participants. As applications require more information to diagnose the error or to aid in the recovery, various diagnostic activities of increasing complexity may be utilized making use of the alternate access bus. At the far end of this spectrum, enough information is generated with the error to instantly mask the error obviating the need for immediate repair and recovery. As in error detection, the minimum error logging and capability to shut down the bus is required in all Profile S modules.

7.2.1 Error handling

Errors detected by parity, duplicated signals, reflected protection, protocol monitoring, and timeouts shall be handled by Profile S modules as defined in IEEE Std 896.9-1994, Clause 4.

Single errors detected by error correcting codes or triple modular redundancy shall be logged in the appropriate ECC or TMR **SP_xyz_HOLD** CSR location with sufficient information to locate the error. These will cause the **ECC_TMR_ERROR_DETECTED** bit to be set in the **ERROR_LO** CSR and are further defined in Clause 9. As long as the error is masked by the ECC/TMR circuitry and no other error is detected or reported, this will not cause a break in the usage of the Error Correcting configuration. It is strongly rec-

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ommended that software is notified through a low-level interrupt or through polling that error masking has occurred.

7.2.2 Enable/Disable transceivers

Profile S modules shall implement the **MAINT_CONTROL** and **MAINT_MONITOR** CSR bits necessary to enable or disable the transceivers for each Futurebus+ and Serial Bus through at least two separate paths. These are defined in Clause 9.

7.2.3 Force errors

Profile S modules shall implement the **MAINT_CONTROL** CSR and **MAINT_MONITOR** CSR bits necessary to force errors to implemented error detection mechanisms and verify error detection. These are defined further in Clause 9.

7.2.4 Diagnostic data register

Profile S modules shall implement the **MAINT_UTILITY** CSR as defined in IEEE Std 896.9-1994 to provide a diagnostic register to test Futurebus+ transaction timing and error detection. These are included in Clause 9.

7.2.5 Critical register write protection

Profile S modules shall implement the **WRITE_PROTECT** and **WRITE_PROTECTED** CSRs as defined in IEEE Std 896.9-1994. This protects critical Futurebus+ CSRs from spurious writes.

7.3 Error removal and recovery

Once an error is detected, isolated, and logged, it is possible to attempt to remove the error or recover from the error in other ways. With the exception of simple hardware retry, all of these mechanisms are optional.

7.3.1 Hardware retry

Profile S modules shall implement immediate hardware retry as defined in IEEE Std 896.9-1994 in response to all detected bus errors that are not masked through error correction. Hardware retry is optional in Level 0.

7.3.2 Software retry

Profile S modules that implement software retry shall do so as defined in IEEE Std 896.2-1991 and IEEE Std 896.9-1994.

7.3.3 Spare lines

Several spare lines shall be provided in the Error Correcting configuration in support of hard fault recovery.

Once a line is identified that has a hard error on it, the TMR or ECC covering that line is greatly reduced. In the case of TMR, a second error in the three lines would result in an incorrect vote. In the case of ECC, errors can no longer be corrected and only single bit additional errors can be detected. For this reason, it is imperative that a failing line be replaced as soon as possible for the proper continuing operation of software. It was decided that having a complete second Error Correcting Futurebus+ would use too much power and too many pins. Since the TMR and ECC inherently take longer and thus have a lower performance, it was felt that the slight performance penalty to carry spare lines multiplexed into the main Error Correcting Futurebus+ could be absorbed by the longer TMR/ECC bus characteristics. This is not the case with the

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Dual Buses as these are actually two independent high performance Futurebus+ buses as the next subclause will define.

Table 7-4 shows the spare lines grouped with the lines they cover. The number of signals covered by some spares is much smaller than for others because of performance and signal grouping issues. The address, data, and code spares (**ADS[15..0]*** and **BCS[1..0]***) each only cover four signals. The other spares cover between 6 and 15 signals. The address, data, and code lines are in the critical path and use ECC coding for every bus transaction, so any degradation will significantly affect system performance. This degradation comes from the larger, slower multiplexers that are required if more signals are to be spared combined with the larger checking circuits required for the ECC syndromes. The other signals, however, are covered by TMR. The process of TMR voting only involves three signals per vote and this combined with larger multiplexor delays for the larger number of lines to be covered by each spare signal should balance out with those signals covered by ECC in the error correcting bus configuration.

The **ENABLE_SPARE_LINES** in the **SP_ENABLE_SPARES_I** (CSR 680), **SP_ENABLE_SPARES_II** (CSR 684), **SP_ENABLE_SPARES_III** (CSR 688), and **SP_ENABLE_SPARES_IV** (CSR 692) CSRs shall be provided to enable the spare lines. Each spare line has an N-bit code in the CSRs given above that defines the bit that it replaces (see Table 7-5). Any forced error condition produced by the **MAINT_MONITOR** CSRs shall make use of any spare lines configured in place of the original bus lines. The spare lines shall be given for both 32-bit and 64-bit Error Correcting configurations. These are summarized in Table 7-4.

For complete bus pinouts, see Clauses 10,11, and 17.

In Error Correcting configurations, the following spare lines shall be implemented:

Command Spares **CMS[1..0]*** shall be capable of sparing any of the Command (**CM[7..0]***) or Command Code (**CC[4..0]***) signals per Table 7-4.

Status, Capability, and Handshake Spares **TMRS[4..0]*** shall be capable of sparing any of the Status (**ST[7..0]***, **STA[7..0]***, or **STB[7..0]***), Capability (**CA[2..0]***, **CAA[2..0]***, or **CAB[2..0]***), Address Handshakes (**AS***, **ASA***, **ASB***, **AK***, **AKA***, **AKB***, **AI***, **AIA***, or **AIB***), Data Handshakes (**DS***, **DSA***, **DSB***, **DK***, **DKA***, **DKB***, **DI***, **DIA***, or **DIB***), or End of Tenure (**ET***, **ETA***, or **ETB***) signals per Table 7-4.

Reset Spare **RES*** shall be capable of sparing any of the Reset (**RE***, **REA***, **REB***) signals per Table 7-4.

Central Arbitration Spares **GRS*** and **GCS*** shall be capable of sparing any of the Requests (**RQ[1..0]***, **RQA[1..0]***, or **RQB[1..0]***), Grants (**GR***), Grant Codes (**GC[5..0]***), Grant Code Parity (**GCP***), or Preemption (**PE***, **PEA***, or **PEB***) signals per Table 7-4.

Utility Spare **UPSP*** shall be capable of sparing any of the Nuclear Event Detect (**NED***, **NEDA***, or **NEDB***), Power Fail Imminent (**PFI***, **PFIA***, or **PFIB***), or System Reset (**SR***, **SRA***, or **SRB***) signals per Table 7-4. **UWSP** shall be capable of sparing any of the Power Normal (**PN**, **PNA**, or **PNB**) signals per Table 7-4.

Address/Data Spares **ADS[7..0]*** & **BCS[1..0]*** shall be capable of sparing any of the Address/Data (**AD[31..0]***), or Bus Code (**BC[7..0]***) signals per Table 7-4.

In 64-bit Error Correcting configurations, Address/Data Spares **ADS[15..0]*** & **BCS[1..0]*** shall be capable of sparing the respective Address/Data (**AD[63..0]***), or Bus Code (**BC[7..0]***) signals per Table 7-4.

In Error Correcting configurations that implement distributed arbitration, Distributed Arbitration Spares **ARBS*** and **ABS[1..0]*** shall be capable of sparing any of the Arbitrated Message Bus (**AB[7..0]***) Arbi-

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trated Message Bus Codes (**ABC[4..0]***), Arbitration Handshakes (**AR***, **ARA***, **ARB***, **AP*, APA***, **APB***, **AQ***, **AQA***, or **AQB***), or Arbitrated Message Condition (**AC[1..0]***, **ACA[1..0]***, or **ACB[1..0]***) signals per Table 7-4.

Table 7-4—Error Correcting configuration spare pin definition

Signal name	Signal description	Signal coverage by spare
ABS0*	Arbitrated Message Spare 0	AB0*, AB2*, AB4*, AB6*, ABC0*, ABC2*, ABC4*
ABS1*	Arbitrated Message Spare 1	AB1*, AB3*, AB5*, AB7*, ABC1*, ABC3*
CMS0*	Command Spare 0	CM0*, CM2*, CM4*, CM6*, CC0*, CC2*, CC4*
CMS1*	Command Spare 1	CM1*, CM3*, CM5*, CM7*, CC1*, CC3*
TMRS0*	Status, Capability, & Handshake Spare 0	ST0*, ST4*, STB1*, STB5*, AS*, ASA*, ASB*, CA0*, CA1*
TMRS1*	Status, Capability, & Handshake Spare 1	ST1*, ST5*, STA0*, STA4*, STB2*, STB6*, CAA0*, CAA1*, DI*, DIA*, DIB*
TMRS2*	Status, Capability, & Handshake Spare 2	ST2*, ST6*, STA1*, STA5*, STB3*, STB7*, CAB0*, CAB1*, DK*, DKA*, DKB*
TMRS3*	Status, Capability, & Handshake Spare 3	ST3*, ST7*, STA2*, STA6*, AI*, AIA*, AIB*, DS*, DSA*, DSB*
TMRS4*	Status, Capability, & Handshake Spare 4	STA3*, STA7*, STB0*, STB4*, AK*, AKA*, AKB*, ET*, ETA*, ETB*
ARBS*	Arbitration Condition & Handshake Spare	AP*, APA*, APB*, AQ*, AQA*, AQB*, AR*, ARA*, ARB*, AC0*, AC1*, ACA0*, ACA1*, ACB0*, ACB1*
RES*	Reset Spare	RE*, REA*, REB*
GRS*	Arbitration Request and Grant Spare	GR*, RQ0*, RQ1*, RQA0*, RQA1*, RQB0*, RQB1*
GCS*	Grant Code & Preemption Spare	GC0*, GC1*, GC2*, GC3*, GC4*, GC5*, GCP*, PE*, PEA*, PEB*
ADS0*	Address, Data, and Code Spare 0	AD0*, AD2*, AD4*, AD6*
ADS1*	Address, Data, and Code Spare 1	AD1*, AD3*, AD5*, AD7*
ADS2*	Address, Data, and Code Spare 2	AD8*, AD10*, AD12*, AD14*
ADS3*	Address, Data, and Code Spare 3	AD9*, AD11*, AD13*, AD15*
ADS4*	Address, Data, and Code Spare 4	AD16*, AD18*, AD20*, AD22*
ADS5*	Address, Data, and Code Spare 5	AD17*, AD19*, AD21*, AD23*
ADS6*	Address, Data, and Code Spare 6	AD24*, AD26*, AD28*, AD30*
ADS7*	Address, Data, and Code Spare 7	AD25*, AD27*, AD29*, AD31*
ADS8*	Address, Data, and Code Spare 8	AD32*, AD34*, AD36*, AD38*
ADS9*	Address, Data, and Code Spare 9	AD33*, AD35*, AD37*, AD39*
ADS10*	Address, Data, and Code Spare 10	AD40*, AD42*, AD44*, AD46*
ADS11*	Address, Data, and Code Spare 11	AD41*, AD43*, AD45*, AD47*
ADS12*	Address, Data, and Code Spare 12	AD48*, AD50*, AD52*, AD54*
ADS13*	Address, Data, and Code Spare 13	AD49*, AD51*, AD53*, AD55*
ADS14*	Address, Data, and Code Spare 14	AD56*, AD58*, AD60*, AD62*
ADS15*	Address, Data, and Code Spare 15	AD57*, AD59*, AD61*, AD63*
BCS0*	Address, Data, and Code Spare 16	BC0*, BC2*, BC4*, BC6*
BCS1*	Address, Data, and Code Spare 17	BC1*, BC3*, BC5*, BC7*
UPSP*	Utility Signal Push Pull TTL Spare	NED*, NEDA*, NEDB*,PFI*, PFIA*, PFIB*, SR*, SRA*, SRB*
UWSP	Utility Signal Wire OR TTL Spare	PN, PNA, PNB

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7.3.3.1 Spare line enables

The following shall select the signal that a spare line replaces in the Error Correcting configuration (see Table 7-5). A code of all zeroes disables that spare line. All spare lines shall be initially zero upon power up.

Bits 3–0, **SPARE_UTILITY_PP** of R/W **SP_ENABLE_SPARES_I** (CSR 680), selects which signal to spare with **UPSP***.

Bits 5–40, **SPARE_UTILITY_WO** of R/W **SP_ENABLE_SPARES_I** (CSR 680), selects which signal to spare with **UWSP**.

Bits 19–16, **SPARE_BUS_CODE_EVEN** of R/W **SP_ENABLE_SPARES_II** (CSR 684), selects which signal to spare with **BCS0***.

Bits 23–20, **SPARE_BUS_CODE_ODD** of R/W **SP_ENABLE_SPARES_II** (CSR 684), selects which signal to spare with **BCS1***.

Bits 27–24, **SPARE_ARB_MESSAGE_EVEN** of R/W **SP_ENABLE_SPARES_II** (CSR 684), selects which signal to spare with **ABS0***.

Bits 31–28, **SPARE_ARB_MESSAGE_ODD** of R/W **SP_ENABLE_SPARES_II** (CSR 684), selects which signal to spare with **ABS1***.

Bits 8–6, **SPARE_COMMAND_EVEN** of R/W **SP_ENABLE_SPARES_I** (CSR 680), selects which signal to spare with **CMS0***.

Bits 11–9, **SPARE_COMMAND_ODD** of R/W **SP_ENABLE_SPARES_I** (CSR 680), selects which signal to spare with **CMS1***.

Bits 15–12**, SPARE_ST_CAP_HNDSHK_0** of R/W **SP_ENABLE_SPARES_I** (CSR 680), selects which signal to spare with **TMRS0***.

Bits 19–16, **SPARE_ST_CAP_HNDSHK_1** of R/W **SP_ENABLE_SPARES_I** (CSR 680), selects which signal to spare with **TMRS1***.

Bits 23–20, **SPARE_ST_CAP_HNDSHK_2** of R/W **SP_ENABLE_SPARES_I** (CSR 680), selects which signal to spare with **TMRS2***.

Bits 27–24, **SPARE_ST_CAP_HNDSHK_3** of R/W **SP_ENABLE_SPARES_I** (CSR 680), selects which signal to spare with **TMRS3***.

Bits 31–28, **SPARE_ST_CAP_HNDSHK_4** of R/W **SP_ENABLE_SPARES_I** (CSR 680), selects which signal to spare with **TMRS4***.

Bits 3–0, **SPARE_ARB_CONDITION_HNDSHK** of R/W **SP_ENABLE_SPARES_II** (CSR 684), selects which signal to spare with **ARBS***.

Bits 7–4, **SPARE_PREEMPT_GRANT_CODE** of R/W **SP_ENABLE_SPARES_II** (CSR 684), selects which signal to spare with **GCS***.

Bits 11–8, **SPARE_RESET** of R/W **SP_ENABLE_SPARES_II** (CSR 684), selects which signal to spare with **RES**.*

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Bits 15–12, **SPARE_GRANT_ARB_REQ** of R/W **SP_ENABLE_SPARES_II** (CSR 684), selects which signal to spare with **GRS***.

Bits 3–0, **SPARE_ADDR_DATA_0** of R/W **SP_ENABLE_SPARES_III** (CSR 688), selects which signal to spare with **ADS0***.

Bits 7–4, **SPARE_ADDR_DATA_1** of R/W **SP_ENABLE_SPARES_III** (CSR 688), selects which signal to spare with **ADS1***.

Bits 11–8, **SPARE_ADDR_DATA_2** of R/W **SP_ENABLE_SPARES_III** (CSR 688), selects which signal to spare with **ADS2***.

Bits 15–12, **SPARE_ADDR_DATA_3** of R/W **SP_ENABLE_SPARES_III** (CSR 688), selects which signal to spare with **ADS3***.

Bits 19–16, **SPARE_ADDR_DATA_4** of R/W **SP_ENABLE_SPARES_III** (CSR 688), selects which signal to spare with **ADS4***.

Bits 23–20, **SPARE_ADDR_DATA_5** of R/W **SP_ENABLE_SPARES_III** (CSR 688), selects which signal to spare with **ADS5***.

Bits 27–24, **SPARE_ADDR_DATA_6** of R/W **SP_ENABLE_SPARES_III** (CSR 688), selects which signal to spare with **ADS6***.

Bits 31–28, **SPARE_ADDR_DATA_7** of R/W **SP_ENABLE_SPARES_III** (CSR 688), selects which signal to spare with **ADS7***.

Bits 3–0, **SPARE_ADDR_DATA_8** of R/W **SP_ENABLE_SPARES_I** (CSR 692), selects which signal to spare with **ADS8***.

Bits 7–4, **SPARE_ADDR_DATA_9** of R/W **SP_ENABLE_SPARES_I** (CSR 692), selects which signal to spare with **ADS9***.

Bits 11–8, **SPARE_ADDR_DATA_10** of R/W **SP_ENABLE_SPARES_I** (CSR 692), selects which signal to spare with **ADS10***.

Bits 15–12, **SPARE_ADDR_DATA_11** of R/W **SP_ENABLE_SPARES_I** (CSR 692), selects which signal to spare with **ADS11***.

Bits 19–16, **SPARE_ADDR_DATA_12** of R/W **SP_ENABLE_SPARES_I** (CSR 692), selects which signal to spare with **ADS12***.

Bits 23–20, **SPARE_ADDR_DATA_13** of R/W **SP_ENABLE_SPARES_I (**CSR 692), selects which signal to spare with **ADS13***.

Bits 27–24, **SPARE_ADDR_DATA_14** of R/W **SP_ENABLE_SPARES_I** (CSR 692), selects which signal to spare with **ADS14***.

Bits 31–28, **SPARE_ADDR_DATA_15** of R/W **SP_ENABLE_SPARES_I** (CSR 692), selects which signal to spare with **ADS15***.

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Table 7-5—CSR coverage for Error Correcting configuration spares

Signal name	Signal coverage by spare	Covering CSR	Selection bits	ID # (hex)
UPSP*	NED*, NEDA*, NEDB*, PFI*, PFIA*, PFIB*, SR*, SRA*, SRB*	680	3–0	00
UWSP	PN, PNA, PNB	680	5–4	20
BCS0*	BC0*, BC2*, BC4*, BC6*	684	19–16	01
BCS1*	BC1*, BC3*, BC5*, BC7*	684	23–20	02
ABS0*	AB0*, AB2*, AB4*, AB6*, ABC0*, ABC2*, ABC4*	684	27–24	03
ABS1*	AB1*, AB3*, AB5*, AB7*, ABC1*, ABC3*	684	31–28	04
CMS0*	CM0*, CM2*, CM4*, CM6*, CC0*, CC2*, CC4*	680	8–6	05
CMS1*	CM1*, CM3*, CM5*, CM7*, CC1*, CC3*	680	11–9	06
TMRS0*	ST0*, ST4*, STB1*, STB5*, AS*, ASA*, ASB*, CA0*, CA1*	680	15–12	07
TMRS1*	ST1*, ST5*, STA0*, STA4*, STB2*, STB6*, CAA0*, CAA1*, DI*, DIA*, DIB*	680	19–16	08
TMRS2*	ST2*, ST6*, STA1*, STA5*, STB3*, STB7*, CAB0*, CAB1*, DK*, DKA*, DKB*	680	23–20	09
TMRS3*	ST3*, ST7*, STA2*, STA6*, AI*, AIA*, AIB*, DS*, DSA*, DSB*	680	27–24	0A
TMRS4*	STA3*, STA7*, STB0*, STB4*, AK*, AKA*, AKB*, ET*, ETA*, ETB*	680	31–28	0B
ARBS*	AP*, APA*, APB*, AQ*, AQA*, AQB*, AR*, ARA*, ARB*, AC0*, AC1*, ACA0*, ACA1*, ACB0*, ACB1*	684	3–0	0C
RES*	RE*, REA*, REB*	684	11–8	0D
GRS*	GR*, RQ0*, RQ1*, RQA0*, RQA1*, RQB0*, RQB1*	684	15–12	0E
GCS*	GC0*, GC1*, GC2*, GC3*, GC4*, GC5*, GCP*, PE*, PEA*, PEB*	684	7–4	0F
ADS0*	AD0*, AD2*, AD4*, AD6*	688	3–0	10
ADS1*	AD1*, AD3*, AD5*, AD7*	688	7–4	11
ADS2*	AD8*, AD10*, AD12*, AD14*	688	11–8	12
ADS3*	AD9*, AD11*, AD13*, AD15*	688	15–12	13
ADS4*	AD16*, AD18*, AD20*, AD22*	688	19–16	14
ADS5*	AD17*, AD19*, AD21*, AD23*	688	23–20	15
ADS6*	AD24*, AD26*, AD28*, AD30*	688	27–24	16
ADS7*	AD25*, AD27*, AD29*, AD31*	688	31–28	17
ADS8*	AD32*, AD34*, AD36*, AD38*	692	3–0	18
ADS9*	AD33*, AD35*, AD37*, AD39*	692	7–4	19
ADS10*	AD40*, AD42*, AD44*, AD46*	692	11–8	1A
ADS11*	AD41*, AD43*, AD45*, AD47*	692	15–12	1B
ADS12*	AD48*, AD50*, AD52*, AD54*	692	19–16	1C
ADS13*	AD49*, AD51*, AD53*, AD55*	692	23–20	1D
ADS14*	AD56*, AD58*, AD60*, AD62*	692	27–24	1E
ADS15*	AD57*, AD59*, AD61*, AD63*	692	31–28	1F

7.3.4 Dual Buses

Dual Bus systems are provided for applications that will have sufficient duration such that one or more hard bus failures are expected over the life of the application. Each bus shall be a complete Futurebus+ meeting the error detecting bus application and having a complete set of CSRs. Only one bus is required to be active

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at a time, though applications may be created that use the second bus for performance enhancements and then degrade to one bus when a hard failure disables further usage of one of the buses. This specification does not specifically address or exclude an application requiring two active simultaneous buses such as a bridge function, though the Dual Futurebus+ pinouts should be used for such an application.

Profile S modules that choose to implement the Futurebus+ Dual Bus configuration shall support two completely identical (except **TR0***, **TR1***, **RUN*** and **UMP***) Profile S Futurebus+ and Serial Bus connections. Such modules shall implement the **DISABLE_FB_A** and **DISABLE_FB_B** bits in the **ALTERNATE_CONTROL** CSR and the **DISABLE_PAA** and **DISABLE_SAA** bits in the **MAINT_CONTROL** CSR as defined in IEEE Std 896.9-1994. These are included in Clause 9.

7.4 Pinout summary

Table 7-6 provides a summary of the logical signals for each bus configuration in IEEE Std 896.10-1997.

Table 7-6—Pinout summary

Signals	Single error detecting	Dual error detecting	Error correcting
Address/Data (32 bit)	AD[31..0]*	1-AD[31..0]* 2-AD[31..0]*	AD[31..0]*
Bus Detection (32 bit)	BP[3..0]*	1-BP[3..0]* 2-BP[3..0]*	BC[7..0]*
Bus Spares (32 bit)			ADS[7..0]* BCS[1..0]*
Address/Data (64 bit)	AD[63..0]*	1-AD[63..0]* 2-AD[63..0]*	AD[63..0]*
Bus Detection (64 bit)	BP[7..0]*	1-BP[7..0]* 2-BP[7..0]*	BC[7..0]*
Bus Spares (64 bit)			ADS[15..0]* BCS[1..0]*
Address/Data (128 bit)	AD[127..0]*		
Bus Detection (128 bit)	BP[15..0]*		
Command	CM[7..0]*	1-CM[7..0]* 2-CM[7..0]*	CM[7..0]*
Command Detection	CP*	1-CP* 2-CP*	CC[4..0]*
Command Spares			CMS[1..0]*
Status	ST[7..0]*	1-ST[7..0]* 2-ST[7..0]*	ST[7..0]*
Capability	CA[2..0]*	1-CA[2..0]* 2-CA[2..0]*	CA[2..0]*
Status and Cap Detection	RF*, TED*, SLD*	1-RF*, 1-TED*, 1-SLD*, 2-RF*, 2-TED*, 2-SLD*	STA[7..0]*, STB[7..0]* CAA[2..0]*, CAB[2..0]*
Address Handshake	AS*, AK*, AI*	1-AS*, 1-AK*, 1-AI*, 2-AS*, 2-AK*, 2-AI*	AS*, ASA*, ASB*, AK*, AKA*, AKB*, AI*, AIA*, AIB*
Data Handshakes	DS*, DK*, DI*	1-DS*, 1-DK*, 1-DI*, 2-DS*, 2-DK*, 2-DI*	DS*, DSA*, DSB*, DK*, DKA*, DKB*, DI*, DIA*, DIB*
End of Tenure	ET*	1-ET* 2-ET*	ET*, ETA*, ETB*

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Table 7-6—Pinout summary *(continued)*

Signals	Single error detecting	Dual error detecting	Error correcting
Status, Capability, and Handshake Spares			TMRS[4..0]*
Reset	RE*, RED*	1-RE*, 1-RED* 2-RE*, 2-RED*	RE*, REA*, REB*
Reset Spare			RES*
CA Requests	RQ[0..1]*	1-RQ[0..1]*, 2-RQ[0..1]*	RQ[0..1]*, RQA[0..1]* RQB[0..1]*
CA Grants	GR*	1-GR* 2-GR*	GR*, GC[5..0]*, GCP*
Preemption	PE*	1-PE* 2-PE*	PE*, PEA*, PEB*
Central Arbitration Spares			GRS*, GCS*
Geographic Address	GA[4..0]*	1-GA[4..0]* 2-GA[4..0]*	GA[4..0]*
GA Parity	GAP*	1-GAP* 2-GAP*	GAP*
Utility Test Signals	UMP*, TR0*, TR1*, RUN*	UMP*, TR0*, TR1*, RUN*	UMP*, TR0*, TR1*, RUN*
Utility, Power	NED*, PFI*, PN, SR*	1-NED*, 1-PFI,* 1-PN, 1-SR*, 2-NED*, 2-PFI*, 2-PN, 2-SR*	NED*, NEDA*, NEDB*, PFI*, PFIA*, PFIB*, PN, PNA, PNB, SR*, SRA*, SRB*
Utility Spares			UPSP*, UWSP
Arbitrated Message Bus[a]	AB[7..0]*	1-AB[7..0]* 2-AB[7..0]*	AB[7..0]*
Arbitrated Message Bus Detection[a]	ABP*	1-ABP* 2-ABP*	ABC[4..0]*
Arbitrated Message Synchronization[a]	AP*, AQ*, AR*	1-AP*, 1-AQ*, 1-AR* 2-AP*, 2-AQ*, 2-AR*	AP*, APA*, APB*, AQ*, AQA*, AQB*, AR*, ARA*, ARB*
Arbitrated Message Condition[a]	AC[1..0]*	1-AC[1..0]*, 2-AC[1..0]*	AC[1..0]*, ACA[1..0]*, ACB[1..0]*
Distributed Arbitration Spares[a]			ABS[1..0]* ARBS*
Total Signals (32/64/128 bit configuration)	100/136/208	196/268/Not permitted	191/223/Not permitted

[a]These signals are optional.

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8. Serial Bus

The Serial Bus shall serve as the ISO/IEC 13213: 1994 compatible alternate access bus required by IEEE Std 896.9-1994. It may also be used as a user test interface in conjunction with the utility signals.

In addition to the Futurebus+ interface, Profile S modules shall contain a backplane Serial Bus interface that is compliant with the IEEE Std 1394-1995 high speed Serial Bus and the following specifications. The primary purpose of the Profile S Serial Bus is for module maintenance. Module maintenance includes control of module power, determining module identification and capabilities, running module diagnostics, isolating a module from a Futurebus+ interface, and handling front panel indicators and switches.

The Serial Bus supports these maintenance actions by providing direct access to Serial Bus CSRs and alternate, or redundant, indirect access to Futurebus+ CSRs. Alternate access to the CSRs of Futurebus+ node(s) becomes important when the Futurebus+ interface is not functioning due to, for example, failure of the Futurebus+ interface. All of the Serial Bus node CSRs specified in this clause and the Futurebus+ node CSRs specified in 9.3.6.3 shall be accessible via the Serial Bus Interface. Access to Futurebus+ node CSRs via the Serial Bus shall be accomplished with the Futurebus+ Alternate Access Unit (FBAAU) in 9.3.6.3.

Other uses of the Serial Bus are permitted provided they do not interfere with this primary purpose of the Serial Bus.

8.1 Serial Bus physical layer

This subclause describes the physical layer requirements for the Profile S Serial Bus interface. A summary of these physical layer requirements is listed in Table 8-1. The Profile S Serial Bus interface shall conform to the backplane (not the cable) physical environment specified in IEEE Std 1394-1995.

Table 8-1—Serial Bus physical layer referenced specifications

Function	Standard	Parameter	Comments
Electrical	IEEE Std 896.10-1997	Wire-or transceivers	Same electrical environment as specified for the Futurebus+ interface.
Bit cell period	IEEE Std 1394-1995	1/49.152 MHz (±100 ppm)	
Signal mapping	IEEE Std 896.10-1997	Two pins in Connector field G	**SBUS_DATA** to pin **SB0*** **SBUS_STRB** to pin **SB1***
Power	IEEE Std 896.10-1997	+5 V, +3.3 V, and +2.1 V supplies	Powered on and off with the other module logic.
Arbitration Fair Urgent Priority Arbitration Number	IEEE Std 1394-1995 IEEE Std 896.10-1997	 Required Optional 6 bits = Futurebus+ **GA[4..0]*** and a 0 bit.	 One node per Serial Bus per module.

The backplane version of Serial Bus is specified using two technologies: BTL and TTL. Since the Profile S electrical characteristics are very similar to BTL for wire-or signals, serial bus will operate correctly over wire-or transceivers built to meet the IEEE Std 896.10-1997 electrical specifications. Serial Bus signals (**SB0*** and **SB1***) shall use the same electrical environment as the Futurebus+ wire-or signals as specified in Clause 12.

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The bit cell frequency shall be 49.152 MHz ± 100 ppm.

The signal **SBUS_DATA** defined in IEEE Std 1394-1995 shall be referred to as **SB0*** in this specification. The connector pin assignment for **SB0*** is specified in Clauses 10,11, and 17. The signal **SBUS_STRB** defined in IEEE Std 1394-1995 shall be referred to as **SB1*** in this specification. The connector pin assignment for **SB1*** is also specified in Clauses 10, 11, and 17. Signals **SB0*** and **SB1*** shall be bused across all slots in a Profile S backplane.

A module's Serial Bus node logic and associated power control logic shall be powered from the +5 V, +3.3 V, and/or 2.1 V Futurebus+ supply rails. This logic shall be powered on and off with the module's other functional logic [i.e., the Futurebus+ interface(s) and module application logic]. The Serial Bus node logic and associated logic shall conform to the power characteristics specified in Clause 13.

A module's Serial Bus node shall implement the Fair backplane arbitration scheme specified in IEEE Std 1394-1995. A module may optionally implement the Urgent Priority backplane arbitration scheme also specified in IEEE Std 1394-1995. The high-order five bits of the 6-bit Arbitration Number shall be equal to the state of the module's Futurebus+ geographical address signals, **GA[4..0]***. The remaining low-order bit of the Arbitration number shall be 0.

8.2 Serial Bus link layer

This subclause describes the link layer requirements for the Profile S Serial Bus interface. A summary of these link layer requirements is listed in Table 8-2.

Table 8-2—Serial Bus Link Layer Referenced Specifications

Function	Standard	Parameter	Comments
Unified Transactions	IEEE Std 1394-1995	Optional	Write transactions may be unified or split.
Split Transactions	IEEE Std 1394-1995	Required	
Isochronous Data Transfer	IEEE Std 1394-1995	Optional	

A module's Serial Bus node shall implement Split Transactions. Read and lock transactions may be split. Write transactions into a bus bridge from the Serial Bus to another bus should be split. Write transactions to other Serial Bus nodes may be either split or unified. Thus, a Serial Bus node shall support Unified Transactions as master and may optionally support Unified Transactions as a slave.

A module's Serial Bus node may optionally implement the Isochronous Data Transfer mode. Since Isochronous Data Transfer occurs at the highest bus priority and may increase the latency of maintenance operations, the use of Isochronous Data Transfer should be carefully evaluated before being used on a Profile S Serial Bus.

8.3 Serial Bus transaction layer

This subclause describes the transaction layer requirements for Profile S's Serial Bus interface. A summary of these transaction layer requirements is listed in Table 8-3.

A module's Serial Bus node shall support transactions with the following transaction codes: quadlet write request, quadlet read request, and quadlet read response. The support of the write response transaction code

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Table 8-3—Serial Bus transaction layer referenced specifications

Function	Standard	Parameter	Comments
Transaction Codes	IEEE Std 1394-1995		
quadlet write request		Required	Aligned. Unaligned is optional.
block write request		Optional	
write response		Optional	Required for bridges.
quadlet read request		Required	Aligned. Unaligned is optional.
block read request		Optional	
quadlet read response		Required	Aligned. Unaligned is optional.
block read response		Optional	
cycle start		Optional	
lock request		Optional	If implemented aligned is required.
isochronous packet		Optional	Unaligned is optional.
lock response		Optional	
Lock Subcommands	IEEE Std 1394-1995		
mask_swap		Required	
compare_swap		Required	
fetch_add		Optional	
little_add		Optional	
bounded_add		Optional	
wrap_add		Optional	
Transaction Retry	IEEE Std 1394-1995	Required	

is required for a bus bridge from the Serial Bus to another bus, but is optional for other Serial Bus interfaces. All other transaction codes specified in IEEE Std 1394-1995 may be optionally supported.

A module's Serial Bus node shall support at least aligned data transactions. The support of unaligned data transactions is allowed but optional.

A module's Serial Bus node shall support mask_swap and swap_compare subcommands if lock transactions are implemented. All other lock subcommands specified in IEEE Std 1394-1995 may be optionally supported.

A module's Serial Bus node shall support transaction retry.

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9. Bus/Node management and CSRs

This clause defines the access and definition of the complete set of CSRs that may be part of any Profile S module.

9.1 Addressing

Profile S modules with (only) 32-bit data capability shall implement 32-bit addressing. Profile S modules with 64-bit or 128-bit data capability may implement either 32-bit or 64-bit addressing. Modules that implement 32-bit addressing shall never assert **AW*** (Address Width). Modules that implement 64-bit addressing shall release **AW*** when addressing the lower 3.75 GB of memory space.

When a 32-bit equivalent of a 64-bit address exists, a module shall use the 32-bit address. This restriction allows interoperability of 32-bit and 64-bit modules. Subclause 3.1.1.3 of IEEE Std 896.2-1991 (Hybrid Addressing) includes a table defining mapping between 32-bit and 64-bit address spaces.

9.2 Byte-Lane wiring and byte ordering

All Profile S modules shall follow the byte-lane mapping as described in Clause 3 of IEEE Std 896.2-1991 for the Core CSRs.

9.3 CSRs

Figure 9-1 shows two typical Space Profile modules, each with a Dual Futurebus+ interface and a dual Serial Bus interface. Notice that a set of CSRs supports each type of interface. There shall be a set of CSRs to support the bus on a Single Futurebus+ configuration. There shall be two sets of CSRs to support each bus on a Dual Futurebus+ configuration. There shall be a single set of CSRs to support the bus in an Error Correcting configuration. For this latter configuration, although only one set of CSRs is required, the implementation of error correction techniques to provide error correction over the CSRs is module dependent. CSRs represent and interact with module functions as well as the actual Futurebus+ or Serial Bus interfaces. See ISO/IEC 13213: 1994 for a full discussion of CSRs.

The CSR address space for each interface shall be allocated as shown in Table 9-1. The tables that follow 9.4 summarize each of these CSR areas with appropriate defining standard. The following subclauses define in order all CSRs redefined or newly defined in this standard.

Table 9-1—CSR address space

Area name	Register offset address range
CSR core registers	0–508
Bus-Dependent CSRs	512–1020
ROM registers	1024– 2044
Unit-Specific area	2048– 4092

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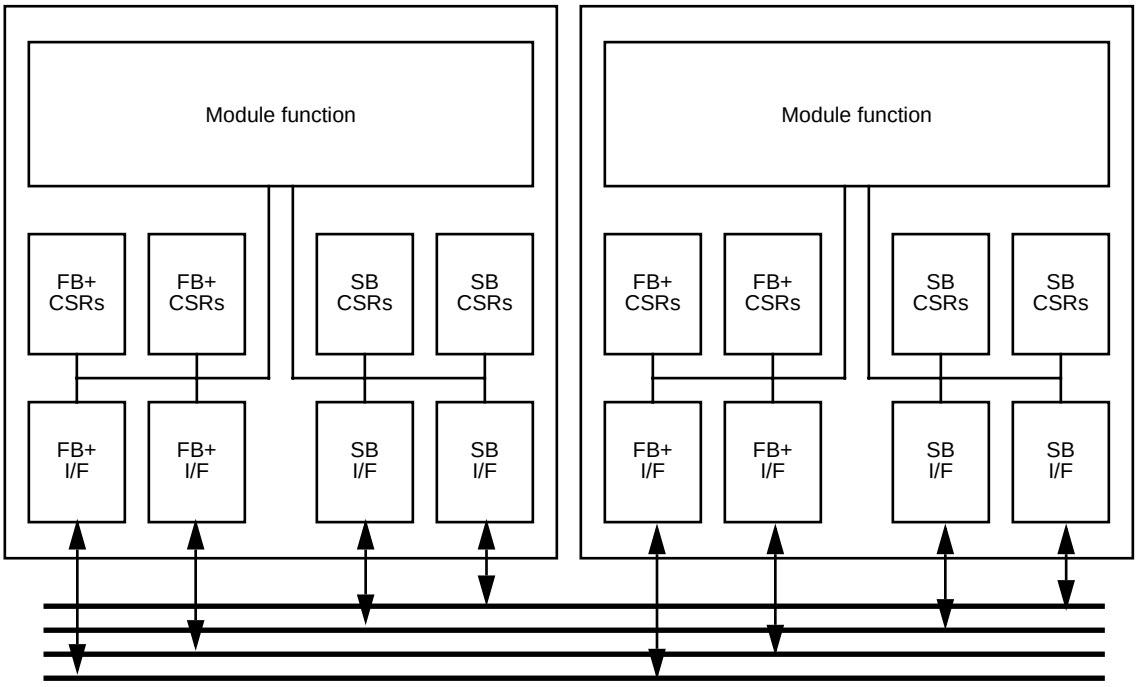

Figure 9-1—CSR locations on space profile modules

9.4 Futurebus+ CSRs

A complete list of the minimum required register set, with field and bit assignments for each Futurebus+ interface, is shown in Tables 9-2 through 9-6. Registers and bits not listed are considered optional. If a module implements optional functionality it shall do so according to requirements specified in IEEE Std 896.2-1991, Clause 3.

A mandate of **Required** means that the register, field, or bit shall be readable, whatever its value. Some bits, like capability bits, are additionally required to be set to 1, meaning that capability is required. All non-implemented bits, fields, and registers shall return zero when read.

The CSR bit fields that have an R/C (read/clear) access type allow reads and write-one-to-clear accesses. Write-one-to-clear access uses the written value to determine how to modify the existing value. In a normal read/write access the written value is stored in the CSR. With a write-one-to-clear CSR, the bits in the CSR are cleared if the written value has a logic one in the same bit position. For example, if a write-one-to-clear CSR has the value 0xFFFF0000 currently in it and 0x0F0F0F0F is written to it, the resulting value will be 0xF0F00000. The logic zeros in the result are caused by two cases. First, the original value had a zero in that bit position. Second, the new value that was written into the CSR had a one in that bit position. The only bit positions with logical ones that are left in the new CSR value are the same bit positions that had logic ones in that position and that had a logic zero in that bit position in the value that was written.

Formally, this may be written as new_value = old_value AND NOT(written_mask)

Although beyond the scope of this document, it is expected that some sort of checking is performed on any CSRs that maintain a value for long periods of time. This could be as simple as a parity bit across each field that changes in unison or duplicated bits that hold information that is dynamic in nature and independent from other CSRs. This could be as complicated as some form of error correcting making use of error correct-

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ing codes and triplicated bits. This might even be handled for some fields by background software routines that would compare or refresh the values on a regular basis. The important thing to remember is that if the CSRs change due to an fault (especially those controlling bus functions such as sparing) and the resulting erroneous behavior is not detected, the system is no longer capable of providing the service it was designed to accomplish.

Table 9-2—Profile S core CSRs

Register name	Address	Mandate	Standard
STATE_CLEAR bit ATN bit OFF	0	Required Not supported Not supported	ISO/IEC 13213: 1994
STATE_SET bit ATN bit OFF	4	Required Not supported Not supported	ISO/IEC 13213: 1994
NODE_IDS	8	Required	ISO/IEC 13213: 1994
RESET_START	12	Required	ISO/IEC 13213: 1994
INDIRECT_ADDRESS	16	Optional	ISO/IEC 13213: 1994
INDIRECT_DATA	20	Optional	ISO/IEC 13213: 1994
SPLIT_TIMEOUT	24,28	Optional[a]	ISO/IEC 13213: 1994
ARGUMENT	32,36	Required	ISO/IEC 13213: 1994
TEST_START	40	Required	ISO/IEC 13213: 1994
TEST_STATUS	44	Required	ISO/IEC 13213: 1994
UNIT_BASE	48,52	Optional	ISO/IEC 13213: 1994
UNIT_EXTENT	56,60	Optional	ISO/IEC 13213: 1994
MEMORY_BASE	64,68	Optional	ISO/IEC 13213: 1994
MEMORY_EXTENT	72,76	Optional	ISO/IEC 13213: 1994
INTERRUPT_TARGET	80	Optional	ISO/IEC 13213: 1994
INTERRUPT_MASK	84	Optional	ISO/IEC 13213: 1994
CLOCK_VALUE	88,92	Optional	ISO/IEC 13213: 1994
CLOCK_TICK_PERIOD	96,100	Optional	ISO/IEC 13213: 1994
CLOCK_STROBE_ARRIVED	104,108	Optional	ISO/IEC 13213: 1994
CLOCK_INFO00	112	Optional	ISO/IEC 13213: 1994
CLOCK_INFO01	116	Optional	ISO/IEC 13213: 1994
CLOCK_INFO02	120	Optional	ISO/IEC 13213: 1994
CLOCK_INFO03	124	Optional	ISO/IEC 13213: 1994
MESSAGE_REQUEST_TARGET	128–188	Optional	ISO/IEC 13213: 1994
MESSAGE_RESPONSE_TARGET	192–252	Optional	ISO/IEC 13213: 1994
Reserved per ISO/IEC 13213: 1994	256–380	Required	ISO/IEC 13213: 1994
ERROR_HI	384	Required	IEEE Std 896.9-1994 (L0-896.2)
ERROR_LO	388	Required	IEEE Std 896.9-1994, IEEE Std 896.10-1997 (L0-896.2)
FAILING_ADDRESS	392, 396	Required	IEEE Std 896.2-1991
BYTE_LANE_IN ERROR	400	Required	IEEE Std 896.2-1991, IEEE Std 896.10-1997 (not in L0)
DATA_HOLD	404–432	Required	IEEE Std 896.2-1991
TAG_HOLD	436	Optional	ISO/IEC 13213: 1994
TIME_STAMP	440, 444	Optional	ISO/IEC 13213: 1994
FTE_HOLD	448	Required (L0-opt)	IEEE Std 896.9-1994
SP_ECC_HOLD	452	Optional[b]	IEEE Std 896.10-1997

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Table 9-2—Profile S core CSRs *(continued)*

Register name	Address	Mandate	Standard
SP_TMR_HOLD_I	456	Optional[b]	IEEE Std 896.10-1997
SP_TMR_HOLD_II	460	Optional[b]	IEEE Std 896.10-1997
SP_CLOCK_CONTROL	464	Optional[b]	IEEE Std 896.10-1997
Reserved	468–476	Required	IEEE Std 896.10-1997
Vendor-Defined	480–508	Optional	ISO/IEC 13213: 1994

[a]Required if Split Transaction capable.
[b]Required if fault tolerance configuration is error correcting.

Table 9-3—Futurebus+-specific CSRs

Register name	Address	Mandate	Standard
FB_LOGICAL_COMMON_CONTROL	512	Required	IEEE Std 896.2-1991
FB_LOGICAL_MODULE_CONTROL	516	Required	IEEE Std 896.2-1991
FB_BUS_PROPAGATION_DELAY	520	Required	IEEE Std 896.2-1991
FB_COMPETITION_SETTLING_TIME	524	Optional[a]	IEEE Std 896.2-1991
FB_TRANSACTION_TIMEOUT	528	Required	IEEE Std 896.2-1991
FB_MESSAGE_PASSING_SELECT_MASK	532,536	Optional[b]	IEEE Std 896.2-1991
FB_BUSY_RETRY_COUNTER	540	Required	IEEE Std 896.2-1991
FB_BUSY_RETRY_DELAY	544	Required	IEEE Std 896.2-1991
FB_ERROR_RETRY_COUNTER	548	Required (L0-opt)	IEEE Std 896.2-1991
FB_ERROR_RETRY_DELAY	552	Required (L0-opt)	IEEE Std 896.2-1991
FB_MAINT_CONTROL	556	Required (L0-opt)	IEEE Std 896.9-1994
FB_WRITE_PROTECT	560	Required	IEEE Std 896.9-1994
FB_REQ_TENURE_TIMEOUT	564	Required (L0-opt)	IEEE Std 896.9-1994
FB_ARB_MSG_TIMEOUT	568	Required(L0-opt)[a]	IEEE Std 896.9-1994
Reserved	572	Required	IEEE Std 896.10-1997
FB_MAINT_UTILITY	576–604	Required	IEEE Std 896.9-1994
FB_MAINT_MONITOR	608–656	Required (L0-opt)	IEEE Std 896.9-1994
SP_ENABLE_ECC_TMR	660	Optional[c]	IEEE Std 896.10-1997
SP_MAINT_MONITOR_ECC	664	Optional[c]	IEEE Std 896.10-1997
SP_MAINT_MONITOR_SYNCH_A	668	Optional[c]	IEEE Std 896.10-1997
SP_MAINT_MONITOR_SYNCH_B	672	Optional[c]	IEEE Std 896.10-1997
SP_MAINT_MONITOR_ST_CAP	676	Optional[c]	IEEE Std 896.10-1997
SP_ENABLE_SPARES_I	680	Optional[c]	IEEE Std 896.10-1997
SP_ENABLE_SPARES_II	684	Optional[c]	IEEE Std 896.10-1997
SP_ENABLE_SPARES_III	688	Optional[c]	IEEE Std 896.10-1997
SP_ENABLE_SPARES_IV	692	Optional[c]	IEEE Std 896.10-1997
Reserved	696–764	Required	IEEE Std 896.10-1997
Vendor-Dependent applications	768–1020	Optional	IEEE Std 896.9-1994

[a]Required if distributed arbitration capable.
[b]Required if message capable.
[c]Required if fault tolerance configuration is error correcting.

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Table 9-4—ROM CSRs

Bit/Field name	Address	Mandate	Standard
ROM_INFO_BLOCK	1024	Required	IEEE Std 896.2-1991 (3.2.4)
Bus Identifier = 0x30383936	1028	Required	IEEE Std 896.2-1991
PROFILE_ID_HI[a]	1032	Required	IEEE Std 896.2-1991
PROFILE_ID_LO[a]	1036	Required	IEEE Std 896.10-1997
MODULE_LOGICAL_CAPABILITY	1040	Required	IEEE Std 896.2-1991
NODE_CAPABILITIES_EXT	1044	Required	IEEE Std 896.9-1994, IEEE Std 896.10-1997
COMPETITION_INTERNAL_DELAY	1048	Optional[b]	IEEE Std 896.2-1991
PACKET_SPEED	1052	Optional[c]	IEEE Std 896.2-1991
MESSAGE_FRAME_SIZE	1056	Optional[d]	IEEE Std 896.2-1991
BUSY_RETRY_COUNTER_CAPABILITY	1060	Required	IEEE Std 896.2-1991
BUSY_RETRY_DELAY_CAPABILITY	1064	Required	IEEE Std 896.2-1991
ERROR_RETRY_COUNTER_CAPABILITY	1068	Required (L0-opt)	IEEE Std 896.2-1991
ERROR_RETRY_DELAY_CAPABILITY	1072	Required (L0-opt)	IEEE Std 896.2-1991
Reserved (3 quadlets)	1076–1084	Required	IEEE Std 896.2-1991
ROOT_DIRECTORY	1088+	Required	IEEE Std 896.10-1997

[a]X’53’ must be in one of the eight bytes of PROFILE_ID.
[b]Required if distributed arbitration capable.
[c]Required if packet mode implemented.
[d]Required if message capable.

Table 9-5—Required root directory ROM entries

Register name	Key type	Mandate	Standard
MODULE_VENDOR_ID	0x08	Required	IEEE Std 896.2-1991
MODULE_SPEC_ID	0x05	Required	IEEE Std 896.2-1991
MODULE_HW_VERSION	0x04	Required	IEEE Std 896.2-1991
NODE_CAPABILITIES	0x0C	Required	IEEE Std 896.2-1991
NODE_UNIQUE_ID	0x8D	Required	ISO/IEC 13213: 1994
MODULE_SW_VERSION	0x06	1 of these 3 required	ISO/IEC 13213: 1994
NODE_SW_VERSION	0x0B	1 of these 3 required	ISO/IEC 13213: 1994
UNITS_SW_VERSION	0x13	1 of these 3 required	ISO/IEC 13213: 1994
SP_PROCESSOR_CLOCK	0x30	Required	IEEE Std 896.10-1997

Table 9-6—Unit area CSRs

Function	Address	Mandate	Standard
Serial Bus Isolate Control Unit	Vendor	Required	IEEE Std 896.10-1997
Alternate Access Unit to Serial Bus CSRs	Vendor	Required	IEEE Std 896.10-1997
Telemetry Parametric Unit	Vendor	Optional	IEEE Std 896.10-1997
Telemetry Configuration Unit	Vendor	Optional	IEEE Std 896.10-1997

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The following subclauses describe Profile S changes and enhancements to the CSRs beyond what is referenced as called out in the above tables. Some rationale is also given for the CSRs chosen from other supporting standards. The definition of new CSRs specific to Profile S is provided. All CSRs required by IEEE Std 896.9-1994 are also required by Profile S modules. Fields marked with a dagger (†) are changed in this standard from IEEE Std 896.2-1991 or IEEE Std 896.9-1994.

9.4.1 Profile S core CSR extensions

9.4.1.1 STATE_CLEAR and STATE_SET CSRs

In the **STATE_CLEAR** and **STATE_SET** CSRs, the **ATN** and **OFF** bits are both used for live insertion. Live insertion is an unsupported feature in Space Profile modules.

9.4.1.2 ERROR_LO CSR

This standard adds one field to the **ERROR_LO** CSR, **ECC_TMR_ERROR_DETECTED**. When set, this bit indicates that an ECC or TMR error was detected and that the **MAINT_MONITOR** CSRs were written and should be locked.

If this bit is set, the **ELOG** bit in **STATE_SET** and the **ERROR_SUMMARY** bit in **ERROR_HI** shall be set. The bits that shall cause **ECC_TMR_ERROR_DETECTED** to be set are given in Figure 9-2. Clearing **ECC_TMR_ERROR_DETECTED** and the bit that caused it to be set followed by **ERROR_SUMMARY** shall unlock the **MAINT_MONITOR** CSRs such that the next error will be captured.

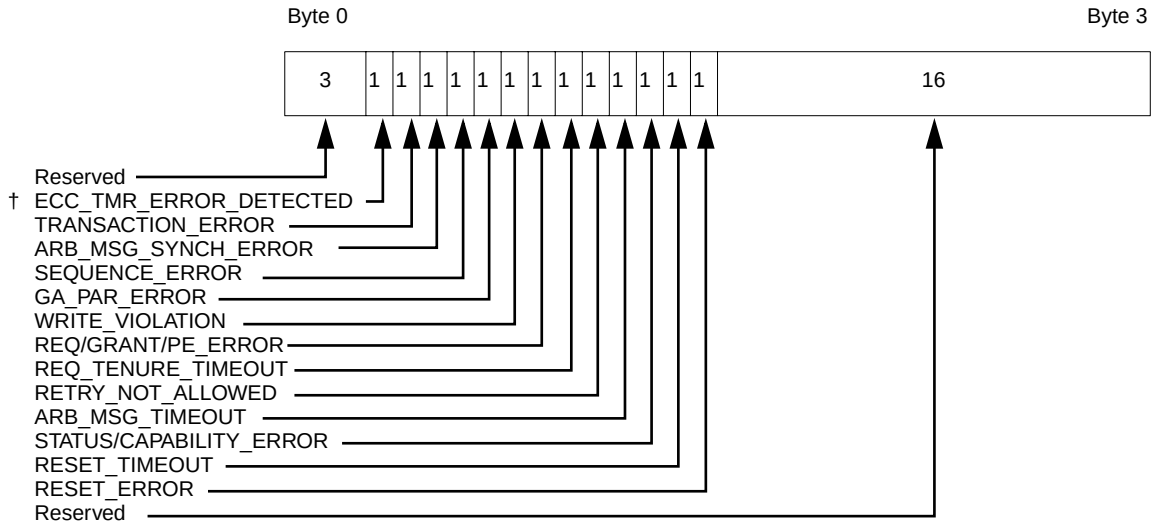

Figure 9-2—ERROR LO (CSR 388) (most significant half)

The bits in the least significant half of **ERROR_LO** are specified in IEEE Std 896.2-1991. Only the most significant half of **ERROR_LO** and the bits that are added are given in Figure 9-2. The remainder of **ERROR_LO** is unchanged. The changed bit is defined in Table 9-7.

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Table 9-7—ERROR LO (CSR 388) (most significant half)

Bit field	Req./ Opt.	Access type	Power up	System reset	Bus initialize
ECC_TMR_ERROR_DETECTED	Req	R/C	0	0	no change
	When set, this bit indicates that an ECC or TMR error has occurred and that the **MAINT_MONITOR** CSRs were written and should be locked. The bits that cause **ECC_TMR_ERROR_DETECTED** to be set are **ECC_72_64_ERROR** **ECC_COMMAND_ERROR** **ECC_ARB_MESSAGE_ERROR** **ECC_GRANT_ERROR_CORRECTION** **EC_SYNDROMES_I** **EC_SYNDROMES_II** **TMR_RQ_0/1_ERROR** **ECC_COMMAND_SYNDROME** For bit fields given above, any bit set in the field will set **ECC_TMR_ERROR_DETECTED**.				

9.4.1.3 BYTE_LANE_IN_ERROR CSR

The **BYTE_LANE_IN_ERROR** CSR (see Figure 9-3 and Table 9-8) is modified in Profile S from the IEEE Std 896.2-1991 definition. Normally, this CSR indicates where parity errors were detected. Profile S modifies bit 0..7 to hold the error syndrome for 32-bit and 64-bit implementations.

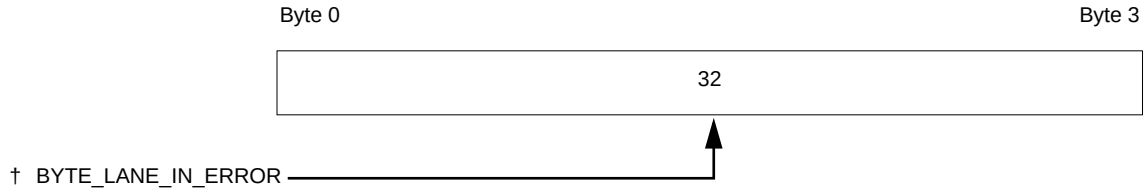

Figure 9-3—BYTE_LANE_IN_ERROR (CSR 400)

Table 9-8—BYTE_LANE_IN_ERROR (CSR 400)

Bit field	Req./ Opt.	Access type	Power up	System reset	Bus initialize
BYTE_LANE_IN_ERROR	Req.	R/C	0x00000000	0x00000000	no change
	This register is normally used to store the identification of the byte lanes on which bad parity was detected. An error in byte lane **AD[7..0]** is stored as a one in the LSB: an error in byte lane **AD[15..8]** is stored as a one in LSB+1, errors in subsequent bytes follow the same sequence. This standard redefines bits 7..0 in an Error Correcting configuration. In such a configuration, these bits are used to store the error syndrome for a 32-bit or 64-bit implementation. These bits are frozen when the **ERROR_SUMMARY** bit in **ERROR_HI** is set.				

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9.4.1.4 SP_ECC_HOLD and SP_TMR_HOLD CSRs

The CSRs in Figures 9-4 through 9-6 and Tables 9-9 through 9-11 are used to hold the error detection/correction results for the bus.

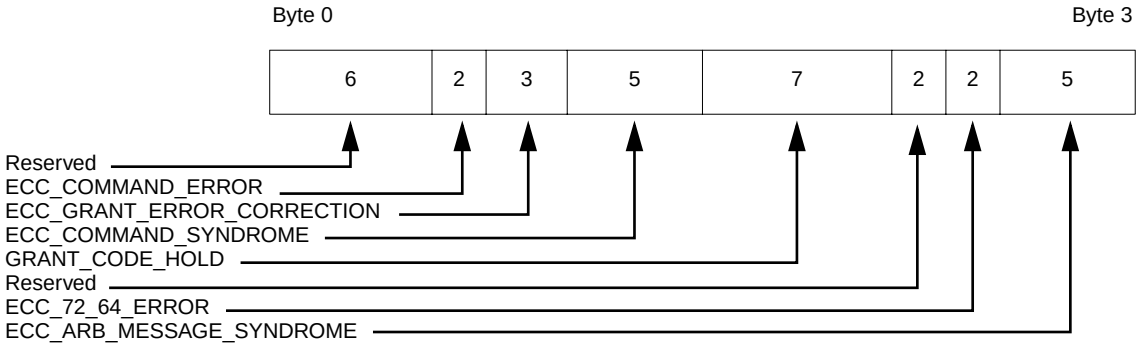

Figure 9-4—SP_ECC_HOLD (CSR 452)

Table 9-9—SP_ECC_HOLD (CSR 452)

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
ECC_ARB_MESSAGE_SYNDROME	Req.	R/C	00000	00000	no change
	These bits store the error syndrome of the Arbitrated Message Bus.				
ECC_72_64_ERROR	Req.	R/C	00	00	no change
	These bits indicate correction results for **AD[63..0]*** and **BC[7..0]***. 00 - No error detected 01 - Correctable error detected and corrected 10 - Uncorrectable error				
GRANT_CODE_HOLD	Req.	R/C	0000000	0000000	no change
	These bits are used to store **GC[5..0]*** and **GCP*** as a result of a miscompare. These bits are updated whenever **GC[5..0]*** or **GCP*** change, they are frozen only after an error occurs.				
ECC_COMMAND_SYNDROME	Req.	R/C	00000	00000	no change
	These bits give the error syndrome for the **CM[7..0]***, **CC[4..0]*** (13,8) code.				
ECC_GRANT_ERROR_CORRECTION	Req.	R/C	000	000	no change
	These bits indicate the correction results for **GR***, **GC[5..0]***, and **GCP***. 0000 - No error detected 0001 - **GCP*** wrong 0010 - **GC[5..0]*** does not match receiving ID 0100 - **GC[5..0]*** matches ID without grant				
ECC_COMMAND_ERROR	Req.	R/C	00	00	no change
	These bits indicate the correction results for **CM[7..0]*** and **CC[4..0]***. 00 - No error detected 01 - Correctable error detected and corrected 10 - Uncorrectable error				

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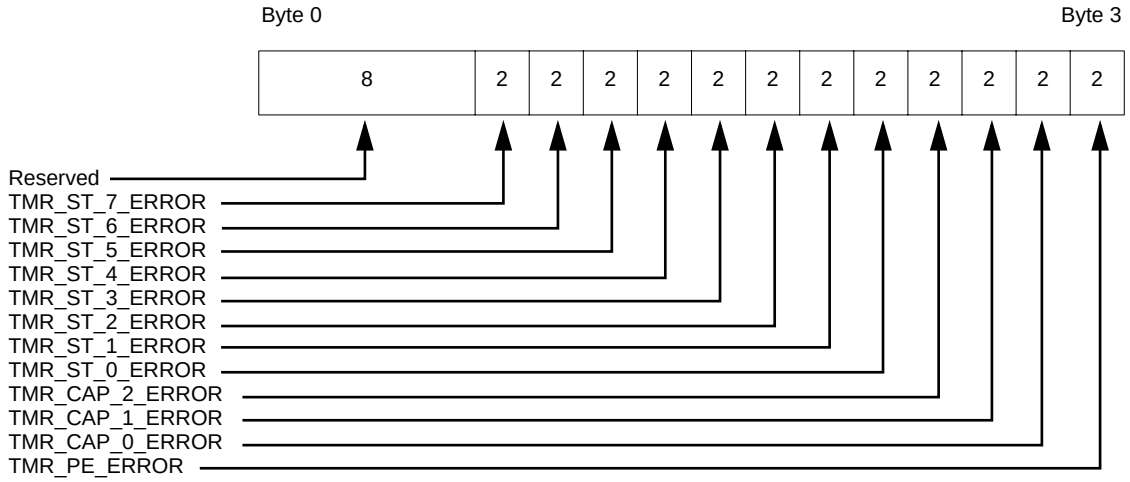

Figure 9-5—ERROR LO (CSR 388) (most significant half)

Table 9-10—SP_TMR_HOLD_I (CSR 456)

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
TMR_PE_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate the result of TMR voting on the Preemption lines. 00 - no error detected 01 - **PE*** did not match 10 - **PEA*** did not match 11 - **PEB*** did not match				
TMR_CAP_0_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate that the **CA[0]***, **CAA[0]*** and **CAB[0]*** bits are in error resulting from comparisons made while correction is enabled. 00 - No error detected 01 - **CA[0]***did not match 10 - **CAA[0]***did not match 11 - **CAB[0]***did not match				
TMR_CAP_1_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate that the **CA[1]***, **CAA[1]*** and **CAB[1]*** bits are in error resulting from comparisons made while correction is enabled. 00 - No error detected 01 - **CA[1]*** did not match 10 - **CAA[1]*** did not match 11 - **CAB[1]*** did not match				
TMR_CAP_2_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate that the **CA[2]***, **CAA[2]*** and **CAB[2]*** bits are in error resulting from comparisons made while correction is enabled. 00 - No error detected 01 - **CA[2]*** did not match 10 - **CAA[2]*** did not match 11 - **CAB[2]*** did not match				

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Table 9-10—SP_TMR_HOLD_I (CSR 456) *(continued)*

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
TMR_ST_0_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate that the **ST[0]***, **STA[0]*** and **STB[0]*** bits are in error resulting from comparisons made while correction is enabled. 00 - No error detected 01 - **ST[0]*** did not match 10 - **STA[0]*** did not match 11 - **STB[0]*** did not match				
TMR_ST_1_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate that the **ST[1]***, **STA[1]*** and **STB[1]*** bits are in error resulting from comparisons made while correction is enabled. 00 - No error detected 01 - **ST[1]*** copy did not match 10 - **STA[1]*** did not match 11 - **STB[1]*** did not match				
TMR_ST_2_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate that the **ST[2]***, **STA[2]*** and **STB[2]*** bits are in error resulting from comparisons made while correction is enabled. 00 - No error detected 01 - **ST[2]*** did not match 10 - **STA[2]*** did not match 11 - **STB[2]*** did not match				
TMR_ST_3_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate that the **ST[3]***, **STA[3]*** and **STB[3]*** bits are in error resulting from comparisons made while correction is enabled. 00 - No error detected 01 - **ST[3]*** did not match 10 - **STA[3]*** did not match 11 - **STB[3]*** did not match				
TMR_ST_4_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate that the **ST[4]***, **STA[4]*** and **STB[4]*** bits are in error resulting from comparisons made while correction is enabled. 00 - No error detected 01 - **ST[4]*** did not match 10 - **STA[4]*** did not match 11 - **STB[4]*** did not match				
TMR_ST_5_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate that the **ST[5]***, **STA[5]*** and **STB[5]*** bits are in error resulting from comparisons made while correction is enabled. 00 - No error detected 01 - **ST[5]*** did not match 10 - **STA[5]*** did not match 11 - **STB[5]*** did not match				

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Table 9-10—SP_TMR_HOLD_I (CSR 456) *(continued)*

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
TMR_ST_6_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate that the **ST[6]***, **STA[6]*** and **STB[6]*** bits are in error resulting from comparisons made while correction is enabled. 00 - No error detected 01 - **ST[6]*** did not match 10 - **STA[6]*** did not match 11 - **STB[6]*** did not match				
TMR_ST_7_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate that the **ST[7]***, **STA[7]*** and **STB[7]*** bits are in error resulting from comparisons made while correction is enabled. 00 - No error detected 01 - **ST[7]*** did not match 10 - **STA[7]*** did not match 11 - **STB[7]*** did not match				

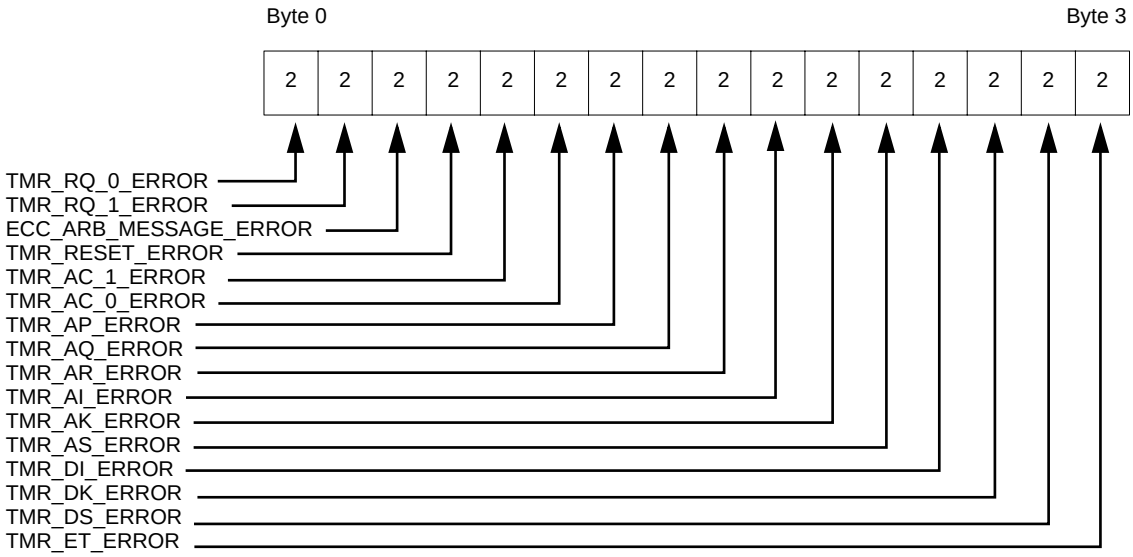

Figure 9-6—SP_TMR_HOLD_II (CSR 460)

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Table 9-11—SP_TMR_HOLD_II (CSR 460)

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
TMR_ET_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate the results of the TMR voting on the End of Tenure lines. 00 - no error detected, all bits match 01 - **ET*** did not match 10 - **ETA*** did not match 11 - **ETB*** did not match				
TMR_DS_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate the results of the TMR voting on the Data Handshake lines. 00 - no error detected, all bits match 01 - **DS*** did not match 10 - **DSA*** did not match 11 - **DSB*** did not match				
TMR_DK_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate the results of the TMR voting on the Data Handshake lines. 00 - no error detected, all bits match 01 - **DK*** did not match 10 - **DKA*** did not match 11 - **DKB*** did not match				
TMR_DI_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate the results of the TMR voting on the Data Handshake lines. 00 - no error detected, all bits match 01 - **DI*** did not match 10 - **DIA*** did not match 11 - **DIB*** did not match				
TMR_AS_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate the results of the TMR voting on the Address Handshake lines. 00 - no error detected, all bits match 01 - **AS*** did not match 10 - **ASA*** did not match 11 - **ASB*** did not match				
TMR_AK_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate the results of the TMR voting on the Address Handshake lines. 00 - no error detected, all bits match 01 - **AK*** did not match 10 - **AKA*** did not match 11 - **AKB*** did not match				
TMR_AI_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate the results of the TMR voting on the Address Handshake lines. 00 - no error detected, all bits match 01 - **AI*** did not match 10 - **AIA*** did not match 11 - **AIB*** did not match				

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Table 9-11—SP_TMR_HOLD_II (CSR 460) *(continued)*

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
TMR_AR_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate the TMR voting on the Arbitration Message Synchronization lines. 00 - no error detected 01 - **AR*** did not match 10 - **ARA*** did not match 11 - **ARB*** did not match				
TMR_AQ_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate the TMR voting on the Arbitration Message Synchronization lines. 00 - no error detected 01 - **AQ*** did not match 10 - **AQA*** did not match 11 - **AQB*** did not match				
TMR_AP_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate the TMR voting on the Arbitration Message Synchronization lines. 00 - no error detected 01 - **AP*** did not match 10 - **APA*** did not match 11 - **APB*** did not match				
TMR_AC_0_ERROR	Req.	R/C	00		00
	These bits are used to indicate that the **AC[0]***, **ACA[0]*** and **ACB[0]*** bits are in error resulting from comparisons made while correction is enabled. 00 - No error detected 01 - **AC[0]*** did not match 10 - **ACA[0]*** did not match 11 - **ACB[0]*** did not match				
TMR_AC_1_ERROR	Req.	R/C	00		00
	These bits are used to indicate that the **AC[1]***, **ACA[1]*** and **ACB[1]*** bits are in error resulting from comparisons made while correction is enabled. 00 - No error detected 01 - **AC[1]*** did not match 10 - **ACA[1]*** did not match 11 - **ACB[1]*** did not match				
TMR_RESET_ERROR	Req.	R/C	00		00
	These bits are used to indicate the TMR voting on the Reset lines. 00 - no error detected 01 - **RE*** did not match 10 - **REA*** did not match 11 - **REB*** did not match				
ECC_ARB_MESSAGE_ERROR	Req.	R/C	00		00
	These bits indicate the correction results for **AB[7..0]*** and **ABC[4..0]***. 00 - No error detected 01 - Correctable error detected and corrected 10 - Uncorrectable error				

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Table 9-11—SP_TMR_HOLD_II (CSR 460) *(continued)*

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
TMR_RQ_0_ERROR	Req.	R/C		00	00
	These bits are used to indicate that the **RQ[0]***, **RQA[0]*** and **RQB[0]*** bits are in error resulting from comparisons made while correction is enabled. 00 - No error detected 01 - **RQ[0]*** did not match 10 - **RQA[0]*** did not match 11 - **RQB[0]*** did not match				
TMR_RQ_1_ERROR	Req.	R/C	00	00	no change
	These bits are used to indicate that the **RQ[1]***, **RQA[1]*** and **RQB[1]*** bits are in error resulting from comparisons made while correction is enabled. 00 - No error detected 01 - **RQ[1]*** did not match 10 - **RQA[1]*** did not match 11 - **RQB[1]*** did not match				

9.4.1.5 SP_CLOCK_CONTROL CSR

The **SP_CLOCK_CONTROL** CSR (see Figure 9-7 and Table 9-12) is used to hold the clock frequency divisor for a processor module or any other Profile S module that might benefit from clock control. This CSR allows the user to control the operating speed of modules and thereby control power consumption. Exact operation is implementation dependent.

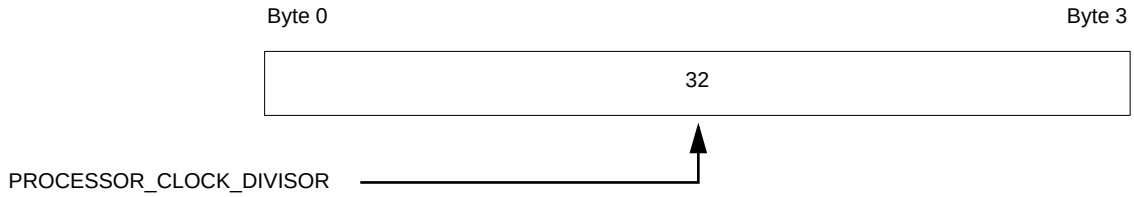

Figure 9-7—SP_CLOCK_CONTROL (CSR 464)

Table 9-12—SP_CLOCK_CONTROL (CSR 464)

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
PROCESSOR_CLOCK_DIVISOR	Opt.	R/W	0x0000	0x0000	no change
	These bits contain the desired processor clock divisor minus one. A value of all zeros will give the maximum frequency.				

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9.4.2 Profile S Futurebus+ specific CSR extensions

9.4.2.1 MAINT_CONTROL

The **ECC_ENABLE** bit (see Figure 9-8 and Table 9-13) is defined in the **MAINT_CONTROL** CSR to enable the ECC and TMR functionality described in this standard. The **ECC_CAPABLE** bit in the **NODE_CAPABILITIES_EXT** CSR must also be set in order for the ECC and TMR functionality to be enabled. If ECC is not enabled, **TMRS0**, **TMRS1**, and **TMRS2** shall drive **RF***, **SLD***, and **TED***, respectively.

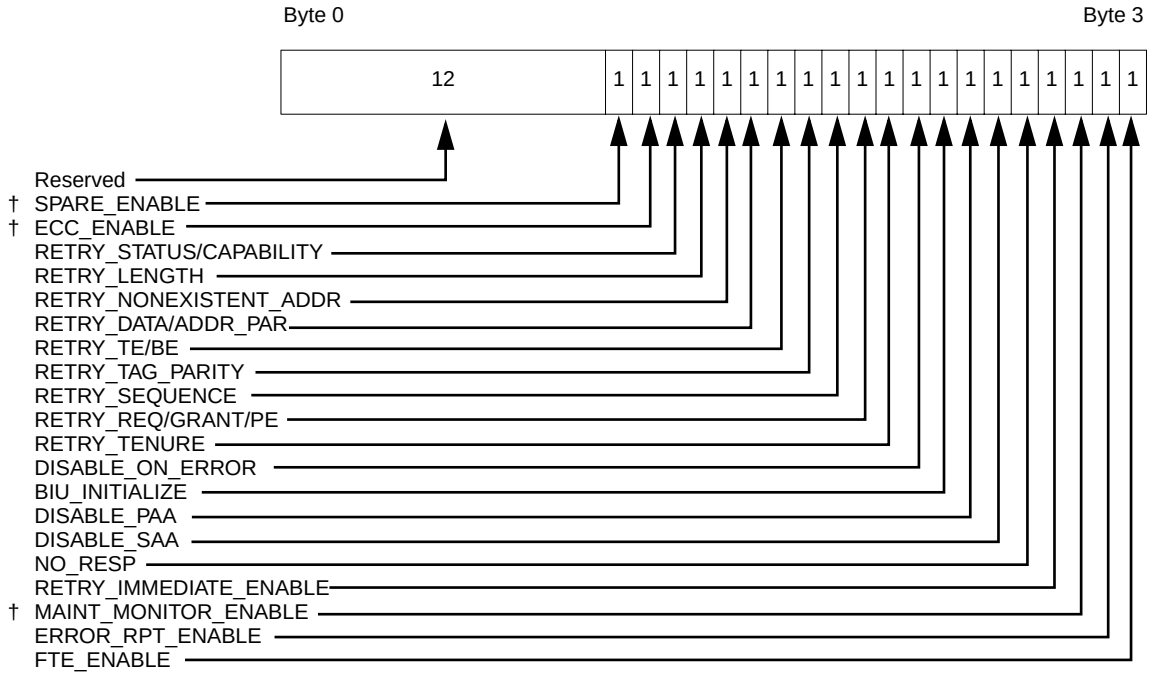

Figure 9-8—MAINT_CONTROL (CSR 556)

Table 9-13—MAINT_CONTROL (CSR 556)

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
ECC_ENABLE	Req.	R/W	0	0	no change
	When this bit is set to one, all Profile S ECC and TMR functionality described in this standard is enabled. Otherwise the ECC and TMR functionality is disabled.				
SPARE_ENABLE	Req.	R/W	0	0	no change
	When this bit is set to one, all Profile S sparing functionality described in this standard is enabled. Otherwise the sparing is disabled.				
MAINT_MONITOR_ENABLE	Req.	R/W	0	0	no change
	If set, this bit enables the contents of the **MAINT_MONITOR** CSRs to their respective signals in the arbitration and parallel bus.				

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The **SPARE_ENABLE** bit (see Figure 9-8 and Table 9-13) is defined in the **MAINT_CONTROL** CSR to enable the sparing functionality described in this standard. The **ECC_CAPABLE** bit in the **NODE_ CAPABILITIES_EXT** CSR must also be set in order for the sparing functionality to be enabled.

The **MAINT_MONITOR_ENABLE** bit (see Figure 9-8 and Table 9-13) is defined in the **MAINT_CONTROL** CSR to coordinate action with the **MAINT_MONITOR, SP_MAINT_MONITOR_ECC, SP_MAINT_MONITOR_SYNCH_A, SP_MAINT_MONITOR_SYNCH_B,** and **SP_MAINT_ MONITOR_ST_CAP** CSRs to allow the assertion and release of various signals for testing the fault detection logic of modules with the **FTE_CAP** and **ECC_CAPABLE** bits asserted in the **NODE_CAPABILITIES_EXT** CSR.

9.4.2.2 SP_ENABLE_ECC_TMR CSR

The **SP_ENABLE_ECC_TMR** CSR (see Figure 9-9 and Table 9-14) is used to enable/disable the ECC and TMR functionality for specific sets of signals on the bus.

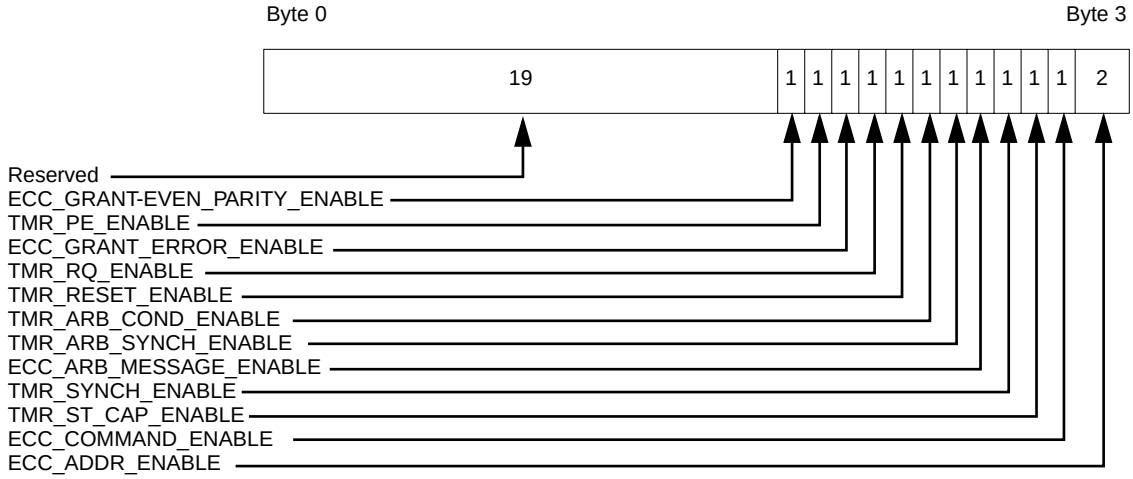

Figure 9-9—SP_ENABLE_ECC_TMR (CSR 660)

Table 9-14—SP_ENABLE_ECC_TMR (CSR 660)

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
ECC_ADDR_ENABLE	Req.	R/W	00	00	no change
	These two bits control enabling of ECC for **AD[63..0]*** and **BC[7..0]***. 00 - no ECC, **BC[7..0]*** used for parity as in IEEE Std 896.9-1994 01 - 32-bit mode 11 - 64-bit mode				
ECC_COMMAND_ENABLE	Req.	R/W	0	0	no change
	This bit controls enabling ECC for **CM[7..0]*** and **CC[4..0]***. 0 - no ECC, **CC[0]*** used for parity as in IEEE Std 896.9-1994 1 - **CM[7..0]*** and **CC[4..0]*** form a (13,8) code word				

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Table 9-14—SP_ENABLE_ECC_TMR (CSR 660) *(continued)*

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
TMR_ST_CAP_ENABLE	Req.	R/W	0	0	no change
	This bit controls enabling TMR for the Status lines (**ST[7..0]***, **STA[7..0]***, and **STB[7..0]***) and the Capability lines (**CA[2..0]***, **CAA[2..0]***, and **CAB[2..0]***). 0 - no correction, **ST[7..0]*** and **CA[2..0]*** are used as single lines 1 - TMR enabled, “A” and “B” copies are used				
TMR_SYNCH_ENABLE	Req.	R/W	0	0	no change
	This bit controls enabling of TMR for the Synchronization lines (**AI*, AK*, AS*, DI*, DK*, DS*,** and **ET***). 0 - no correction, the Synchronization lines are used as single lines 1 - TMR enabled, “A” and “B” copies are used				
ECC_ARB_MESSAGE_ ENABLE	Req.	R/W	0	0	no change
	This bit controls enabling of ECC for **AB[7..0]*** and **ABC[4..0]***. 0 - no ECC, **ABC[0]*** used for parity as in ISO/IEC 10857: 1994 1 - **AB[7..0]*** and **ABC[4..0]*** form a (13,8) code word				
TMR_ARB_SYNCH_ ENABLE	Req.	R/W	0	0	no change
	This bit controls enabling of TMR for the Arbitrated Message Synchronization lines. 0 - no correction, Synchronization lines are used as single lines 1 - TMR enabled, “A” and “B” copies are used				
TMR_ARB_COND_ENABLE	Req.	R/W	0	0	no change
	This bit controls enabling of TMR for the Arbitrated Message Condition lines. 0 - no correction, **AC[1..0]*** are used as single lines 1 - TMR enabled, “A” and “B” copies are used				
TMR_RESET_ENABLE	Req.	R/W	0	0	no change
	This bit controls enabling of TMR for the Reset lines. 0 - no correction, **RE*** and **RED*** are used as dual lines 1 - TMR enabled, “A” and “B” copies are used				
TMR_RQ_ENABLE	Req.	R/W	0	0	no change
	This bit controls enabling of TMR for the CA Requests lines. 0 - no correction, **RQ[1..0]*** are used as single lines 1 - TMR enabled, “A” and “B” copies are used				
ECC_GRANT_ERROR_ENABLE	Req.	R/W	0	0	no change
	This bit controls enabling of correction for the CA Grant lines. 0 - no correction, the **GR*** to each node is solely used for providing grants during central arbitration 1 - **GC[5..0]*** is generated that specifies the master on the line.				
TMR_PE_ENABLE	Req.	R/W	0	0	no change
	This bit controls the enabling of TMR for the Preemption lines. 0 - no correction, **PE*** is used as a single line 1 - TMR enabled, “A” and “B” copies are used				

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Table 9-14—SP_ENABLE_ECC_TMR (CSR 660) *(continued)*

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
ECC_GRANT_EVEN_PARITY_ ENABLE	Req.	R/W	0	0	no change
	This bit forces even parity to be generated on **GCP*** when active. 0 - **GCP*** is odd parity for **GC[5..0]***, this is the default value 1 - **GCP*** is even parity for **GC[5..0]***				

9.4.2.3 SP_MAINT_MONITOR registers

The **SP_MAINT_MONITOR** CSRs (see Figures 9-10 through 9-13 and Tables 9-15 through 9-18) are used to hold the values that are driven onto the additional error correcting signals when the **MAINT_MONITOR_ENABLE** bit is set. Base signal CSRs are defined in IEEE Std 896.9-1994 (see Table 9-3). These CSRs allow any values to be driven onto the bus. This allows a way for the system developer and end user to test the error detecting and possibly error correcting functions of the bus.

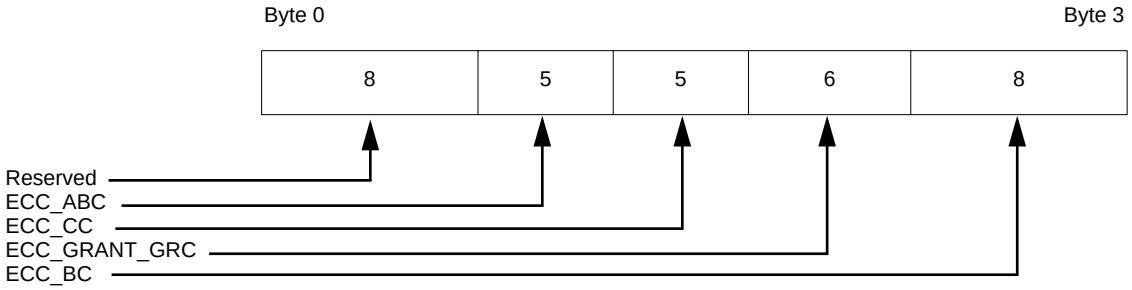

Figure 9-10—SP_MAINT_MONITOR_ECC (CSR 664)

Table 9-15—SP_MAINT_MONITOR_ECC (CSR 664)

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
ECC_BC	Req.	R/W	00000000	00000000	no change
	These bits are placed on **BC[7..0]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. These are initially reset to an inactive state.				
ECC_GRANT_GC	Req.	R/W	000000	000000	no change
	These bits are placed on **GC[5..0]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. These are initially reset to an inactive state.				
ECC_CC	Req.	R/W	00000	00000	no change
	These bits are placed on **CC[4..0]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. These are initially reset to an inactive state.				
ECC_ABC	Req.	R/W	00000	00000	no change
	These bits are placed on **ABC[4..0]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. These are initially reset to an inactive state.				

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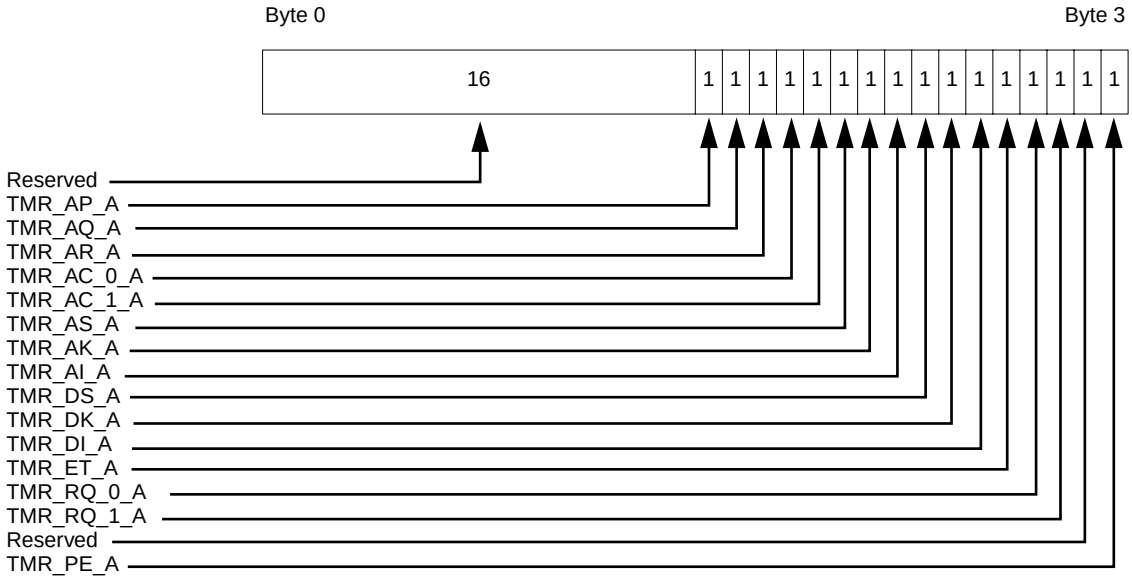

Figure 9-11—SP_MAINT_MONITOR_SYNCH_A (CSR 668)

Table 9-16—SP_MAINT_MONITOR_SYNCH_A (CSR 668)

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
TMR_PE_A	Req.	R/W	0	0	no change
	This bit is placed on **PEA*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_RQ_1_A	Req.	R/W	0	0	no change
	This bit is placed on **RQA[1]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_RQ_0_A	Req.	R/W	0	0	no change
	This bit is placed on **RQA[0]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_ET_A	Req.	R/W	0	0	no change
	This bit is placed on **ETA*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_DI_A	Req.	R/W	0	0	no change
	This bit is placed on **DIA*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_DK_A	Req.	R/W	0	0	no change
	This bit is placed on **DKA*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				

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Table 9-16—SP_MAINT_MONITOR_SYNCH_A (CSR 668) *(continued)*

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
TMR_DS_A	Req.	R/W	0	0	no change
	This bit is placed on **DSA*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_AI_A	Req.	R/W	0	0	no change
	This bit is placed on **AIA*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_AK_A	Req.	R/W	0	0	no change
	This bit is placed on **AKA*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_AS_A	Req.	R/W	0	0	no change
	This bit is placed on **ASA*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_AC_1_A	Req.	R/W	0	0	no change
	This bit is placed on **ACA[1]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_AC_0_A	Req.	R/W	0	0	no change
	This bit is placed on **ACA[0]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_AR_A	Req.	R/W	0	0	no change
	This bit is placed on **ARA*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_AQ_A	Req.	R/W	0	0	no change
	This bit is placed on **AQA*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_AP_A	Req.	R/W	0	0	no change
	This bit is placed on **APA*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				

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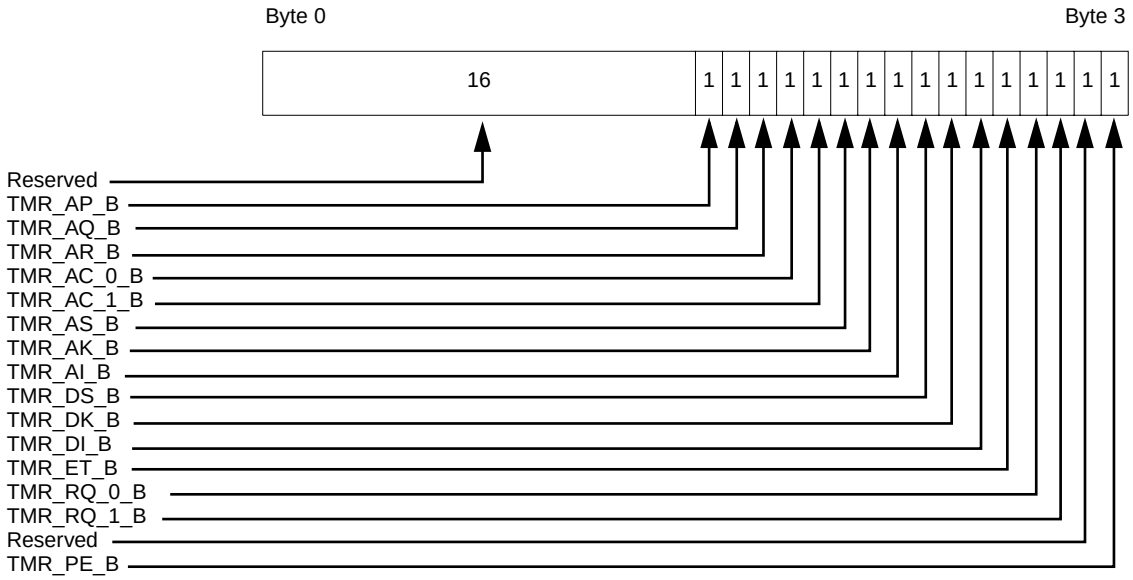

Figure 9-12—SP_MAINT_MONITOR_SYNCH_B (CSR 672)

Table 9-17—SP_MAINT_MONITOR_SYNCH_B (CSR 672)

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
TMR_PE_B	Req.	R/W	0	0	no change
	This bit is placed on **PEB*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_RQ_1_B	Req.	R/W	0	0	no change
	This bit is placed on **RQB[1]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_RQ_0_B	Req.	R/W	0	0	no change
	This bit is placed on **RQB[0]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_ET_B	Req.	R/W	0	0	no change
	This bit is placed on **ETB*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_DI_B	Req.	R/W	0	0	no change
	This bit is placed on **DIB*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				

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Table 9-17—SP_MAINT_MONITOR_SYNCH_B (CSR 672) *(continued)*

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
TMR_DK_B	Req.	R/W	0	0	no change
	This bit is placed on **DKB*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_DS_B	Req.	R/W	0	0	no change
	This bit is placed on **DSB*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_AI_B	Req.	R/W	0	0	no change
	This bit is placed on **AIB*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_AK_B	Req.	R/W	0	0	no change
	This bit is placed on **AKB*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_AS_B	Req.	R/W	0	0	no change
	This bit is placed on **ASB*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_AC_1_B	Req.	R/W	0	0	no change
	This bit is placed on **ACB[1]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_AC_0_B	Req.	R/W	0	0	no change
	This bit is placed on **ACB[0]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_AR_B	Req.	R/W	0	0	no change
	This bit is placed on **ARB*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_AQ_B	Req.	R/W	0	0	no change
	This bit is placed on **AQB*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				
TMR_AP_B	Req.	R/W	0	0	no change
	This bit is placed on **APB*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. This bit is initially reset to an inactive state.				

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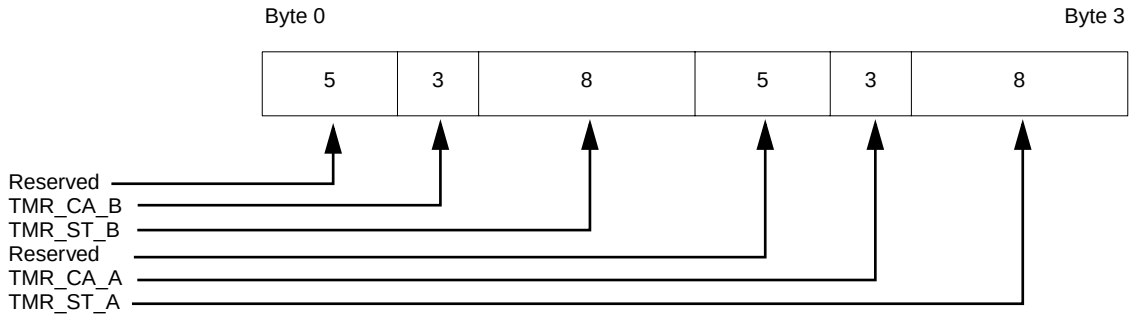

Figure 9-13—SP_MAINT_MONITOR_ST_CAP (CSR 676)

Table 9-18—SP_MAINT_MONITOR_ST_CAP (CSR 676)

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
TMR_ST[7..0]_A	Req.	R/W	00000000	00000000	no change
	These bits are placed on **STA[7..0]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. These bits are initially reset to an inactive state.				
TMR_CA[2..0]_A	Req.	R/W	000	000	no change
	These bits are placed on **CAA[2..0]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. These bits are initially reset to an inactive state.				
TMR_ST[7..0]_B	Req.	R/W	00000000	00000000	no change
	These bits are placed on **STB[7..0]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. These bits are initially reset to an inactive state.				
TMR_CA[2..0]_B	Req.	R/W	000	000	no change
	These bits are placed on **CAB[2..0]*** when the **MAINT_MONITOR_ENABLE** bit in the **MAINT_CONTROL** CSR is asserted. These bits are initially reset to an inactive state.				

9.4.2.4 Sparing CSRs

The sparing CSRs (see Figures 9-14 through 9-17 and Tables 9-19 through 9-22) control which signal line is spared by the spare lines. Sparing is enabled/disabled by setting/clearing the SPARE_ENABLE bit in the **MAINT_CONTROL** CSR (see Figure 9-8).

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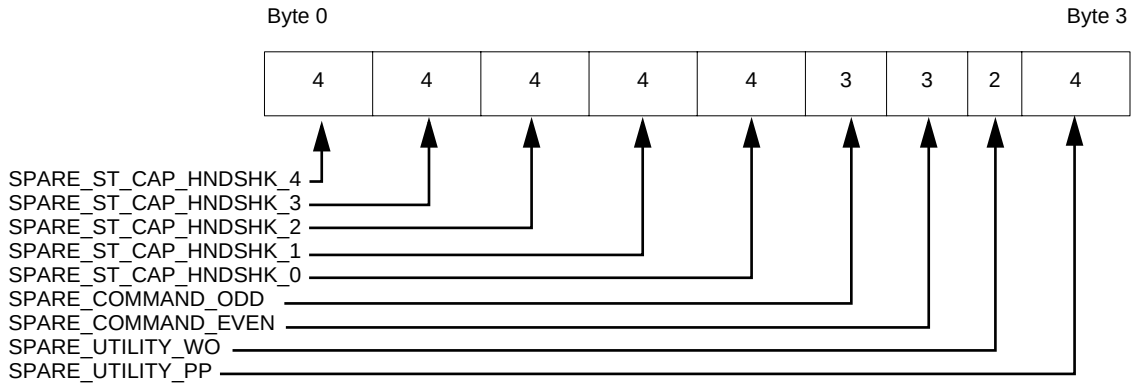

Figure 9-14—SP_ENABLE_SPARES_I (CSR 680)

Table 9-19—SP_ENABLE_SPARES_I (CSR 680)

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
SPARE_UTILITY_PP	Req.	R/W	0000	0000	no change
These bits select which signal to spare with **UPSP***. 0000 - **UPSP*** disabled, no sparing 0001 - **NED*** spared with UTSP 0010 - **NEDA*** spared with UTSP 0011 - **NEDB*** spared with UTSP 0100 - **PFI*** spared with UTSP 0101 - **PFIA*** spared with UTSP 0110 - **PFIB*** spared with UTSP 0111 - **SR*** spared with UTSP 1000 - **SRA*** spared with UTSP 1001 - **SRB*** spared with UTSP 1010–1111 - reserved					
SPARE_UTILITY_WO	Req.	R/W	0000	0000	no change
These bits select which signal to spare with **UWSP**. 00 - **UWSP** disabled, no sparing 01 - **PN** spared with UWSP 10 - **PNA** spared with UWSP 11 - **PNB** spared with UWSP					
SPARE_COMMAND_EVEN	Req.	R/W	0000	0000	no change
These bits select which signal to spare with **CMS0**. 000 - **CMS0** disabled, no sparing 001 - **CM0*** spared with CMS0 010 - **CM2*** spared with CMS0 011 - **CM4*** spared with CMS0 100 - **CM6*** spared with CMS0 101 - **CC0*** spared with CMS0 110 - **CC2*** spared with CMS0 111 - **CC4*** spared with CMS0					

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Table 9-19—SP_ENABLE_SPARES_I (CSR 680) *(continued)*

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
SPARE_COMMAND_ODD	Req.	R/W	0000	0000	no change
	These bits select which signal to spare with **CMS1**. 000 - **CMS1** disabled, no sparing 001 - **CM1*** spared with CMS1 010 - **CM3*** spared with CMS1 011 - **CM5*** spared with CMS1 100 - **CM7*** spared with CMS1 101 - **CC1*** spared with CMS1 110 - **CC3*** spared with CMS1				
SPARE_ST_CAP_HNDSHK_0	Req.	R/W	0000	0000	no change
	These bits select which signal to spare with **TMRS0**. 0000 - **TMRS0** disabled, no sparing 0001 - **ST0*** spared with TMRS0 0010 - **ST4*** spared with TMRS0 0011 - **STB1*** spared with TMRS0 0100 - **STB5*** spared with TMRS0 0101 - **AS*** spared with TMRS0 0110 - **ASA*** spared with TMRS0 0111 - **ASB*** spared with TMRS0 1000 - **CA0*** spared with TMRS0 1001 - **CA1*** spared with TMRS0 1010–1111 - reserved				
SPARE_ST_CAP_HNDSHK_1	Req.	R/W	0000	0000	no change
	These bits select which signal to spare with **TMRS1**. 0000 - **TMRS1** disabled, no sparing 0001 - **ST1*** spared with TMRS1 0010 - **ST5*** spared with TMRS1 0011 - S**TA0*** spared with TMRS1 0100 - **STA4*** spared with TMRS1 0101 - **STB2*** spared with TMRS1 0110 - **STB6*** spared with TMRS1 0111 - **CAA0*** spared with TMRS1 1000 - **CAA1*** spared with TMRS1 1001 - **DI*** spared with TMRS1 1010 - **DIA*** spared with TMRS1 1011 - **DIB*** spared with TMRS1 1100–1111 - reserved				
SPARE_ST_CAP_HNDSHK_2	Req.	R/W	0000	0000	no change
	These bits select which signal to spare with **TMRS2**. 0000 - TMRS2 disabled, no sparing 0001 - **ST2*** spared with TMRS2 0010 - **ST6*** spared with TMRS2 0011 - **STA1*** spared with TMRS2 0100 - **STA5*** spared with TMRS2 0101 - **STB3*** spared with TMRS2 0110 - **STB7*** spared with TMRS2 0111 - **CAB0*** spared with TMRS2 1000 - **CAB1*** spared with TMRS2 1001 - **DK*** spared with TMRS2 1010 - **DKA*** spared with TMRS2 1011 - **DKB*** spared with TMRS2 1100–1111 - reserved				

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Table 9-19—SP_ENABLE_SPARES_I (CSR 680) *(continued)*

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
SPARE_ST_CAP_HNDSHK_3	Req.	R/W	0000	0000	no change
These bits select which signal to spare with **TMRS3**. 0000 - **TMRS3** disabled, no sparing 0001 - **ST3*** spared with TMRS3 0010 - **ST7*** spared with TMRS3 0011 - **STA2*** spared with TMRS3 0100 - **STA6*** spared with TMRS3 0101 - **AI*** spared with TMRS3 0110 - **AIA*** spared with TMRS3 0111 - **AIB*** spared with TMRS3 1000 - **DS*** spared with TMRS3 1001 - **DSA*** spared with TMRS3 1010 - **DSB*** spared with TMRS3 1011–1111 - reserved					
SPARE_ST_CAP_HNDSHK_4	Req.	R/W	0000	0000	no change
These bits select which signal to spare with **TMRS4**. 0000 - **TMRS4** disabled, no sparing 0001 - **STA3*** spared with TMRS4 0010 - **STA7*** spared with TMRS4 0011 - **STB0*** spared with TMRS4 0100 - S**TB4*** spared with TMRS4 0101 - **AK*** spared with TMRS4 0110 - **AKA*** spared with TMRS4 0111 - **AKB*** spared with TMRS4 1000 - **ET*** spared with TMRS4 1001 - **ETA*** spared with TMRS4 1010 - **ETB*** spared with TMRS4 1011–1111 - reserved					

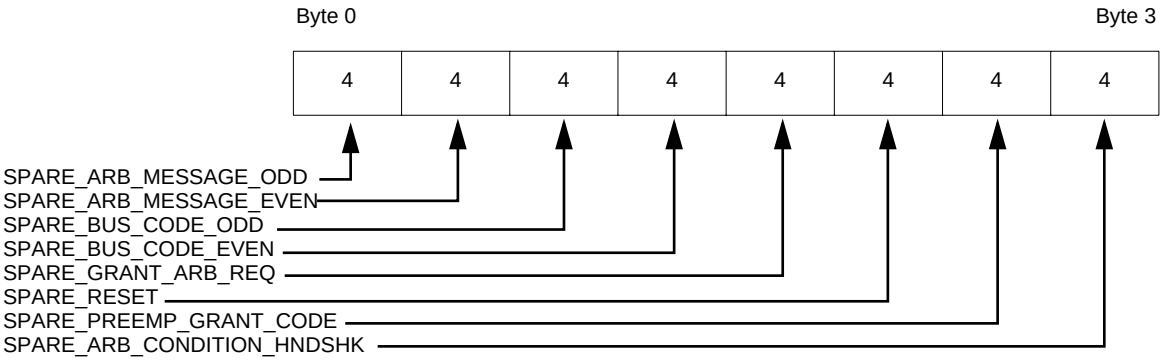

Figure 9-15—SP_ENABLE_SPARES_II (CSR 684)

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Table 9-20—SP_ENABLE_SPARES_II (CSR 684)

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
SPARE_ARB_CONDITION_HNDSHK	Req.	R/W	0000	0000	no change
These bits select which signal to spare with **ARBS**. 0000 - **ARBS** disabled, no sparing 0001 - **AP*** spared with ARBS 0010 - **APA*** spared with ARBS 0011 - **APB*** spared with ARBS 0100 - **AQ*** spared with ARBS 0101 - **AQA*** spared with ARBS 0110 - **AQB*** spared with ARBS 0111 - **AR*** spared with ARBS 1000 - **ARA*** spared with ARBS 1001 - **ARB*** spared with ARBS 1010 - **AC0*** spared with ARBS 1011 - **AC1*** spared with ARBS 1100 - **ACA0*** spared with ARBS 1101 - **ACA1*** spared with ARBS 1110 - **ACB0*** spared with ARBS 1111 - **ACB1*** spared with ARBS					
SPARE_PREEMPT_GRANT_CODE	Req.	R/W	0000	0000	no change
These bits select which signal to spare with **GCS**. 0000 - **GCS** disabled, no sparing 0001 - **PE*** spared with GCS 0010 - **PEA*** spared with GCS 0011 - **PEB*** spared with GCS 0100 - reserved 0101 - reserved 0110 - reserved 0111 - reserved 1000 - **GC0*** spared with GCS 1001 - **GC1*** spared with GCS 1010 - **GC2*** spared with GCS 1011 - **GC3*** spared with GCS 1100 - **GC4*** spared with GCS 1101 - **GC5*** spared with GCS 1110 - **GCP*** spared with GCS 1111 - reserved					
SPARE_RESET	Req.	R/W	0000	0000	no change
These bits select which signal to spare with **RES**. 0000 - **RES** disabled, no sparing 0001 - **RE*** spared with RES 0010 - **REA*** spared with RES 0011 - **REB*** spared with RES 0100 - 1111 - reserved					

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Table 9-20—SP_ENABLE_SPARES_II (CSR 684) *(continued)*

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
SPARE_GRANT_ARB_REQ	Req.	R/W	0000	0000	no change
These bit select which signal to spare with **GRS**. 0000 - **GRS** disabled, no sparing 0001 - **GR*** spared with GRS 0010 - **RQ0*** spared with GRS 0011 - **RQ1*** spared with GRS 0100 - **RQA0*** spared with GRS 0101 - **RQA1*** spared with GRS 0110 - **RQB0*** spared with GRS 0111 - **RQB1*** spared with GRS 1000–1111 - reserved					
SPARE_BUS_CODE_EVEN	Req.	R/W	0000	0000	no change
These bits select which signal to spare with **BCS0**. 0000 - **BCS0** disabled, no sparing 0001 - **BC0*** spared with BCS0 0010 - **BC2*** spared with BCS0 0011 - **BC4*** spared with BCS0 0100 - **BC6*** spared with BCS0 0101–1111 - reserved					
SPARE_BUS_CODE_ODD	Req.	R/W	0000	0000	no change
These bits select which signal to spare with **BCS1**. 0000 - **BCS1** disabled, no sparing 0001 - **BC1*** spared with BCS1 0010 - **BC3*** spared with BCS1 0011 - **BC5*** spared with BCS1 0100 - **BC7*** spared with BCS1 0101–1111 - reserved					
SPARE_ARB_MESSAGE_EVEN	Req.	R/W	0000	0000	
These bits select which signal to spare with **ABS0**. 0000 - **ABS0** disabled, no sparing 0001 - **AB0*** spared with ABS0 0010 - **AB2*** spared with ABS0 0011 - **AB4*** spared with ABS0 0100 - **AB6*** spared with ABS0 0101 - **ABC0*** spared with ABS0 0110 - **ABC2*** spared with ABS0 0111 - **ABC4*** spared with ABS0 1000–1111 - reserved					
SPARE_ARB_MESSAGE_ODD	Req.	R/W	0000	0000	
These bits select which signal to spare with **ABS1**. 0000 - **ABS1** disabled, no sparing 0001 - **AB1*** spared with ABS1 0010 - **AB3*** spared with ABS1 0011 - **AB5*** spared with ABS1 0100 - **AB7*** spared with ABS1 0101 - **ABC1*** spared with ABS1 0110 - **ABC3*** spared with ABS1 0111–1111 - reserved					

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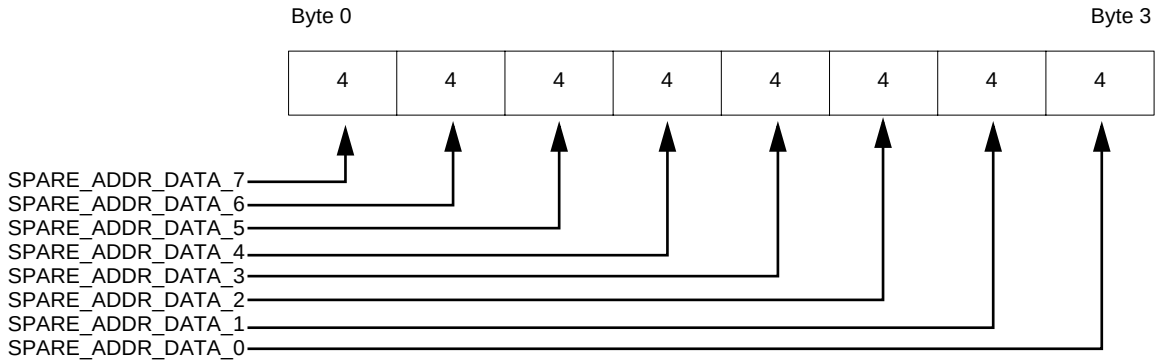

Figure 9-16—SP_ENABLE_SPARES_III (CSR 688)

Table 9-21—SP_ENABLE_SPARES_III (CSR 688)

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
SPARE_ADDR_DATA_0	Req.	R/W	0000	0000	no change
These bits select which signal to spare with **ADS0**. 0000 - **ADS0** disabled, no sparing 0001 - **AD0*** spared with ADS0 0010 - **AD2*** spared with ADS0 0011 - **AD4*** spared with ADS0 0100 - **AD6*** spared with ADS0 0101–1111 - reserved					
SPARE_ADDR_DATA_1	Req.	R/W	0000	0000	no change
These bits select which signal to spare with **ADS1**. 0000 - **ADS1** disabled, no sparing 0001 - **AD1*** spared with ADS1 0010 - **AD3*** spared with ADS1 0011 - **AD5*** spared with ADS1 0100 - **AD7*** spared with ADS1 0101–1111 - reserved					
SPARE_ADDR_DATA_2	Req.	R/W	0000	0000	no change
These bits select which signal to spare with **ADS2**. 0000 - **ADS2** disabled, no sparing 0001 - **AD8*** spared with ADS2 0010 - **AD10*** spared with ADS2 0011 - **AD12*** spared with ADS2 0100 - **AD14*** spared with ADS2 0101–1111 - reserved					

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Table 9-21—SP_ENABLE_SPARES_III (CSR 688) *(continued)*

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
SPARE_ADDR_DATA_3	Req.	R/W	0000	0000	no change
	These bits select which signal to spare with **ADS3**. 0000 - **ADS3** disabled, no sparing 0001 - **AD9*** spared with ADS3 0010 - **AD11*** spared with ADS3 0011 - **AD13*** spared with ADS3 0100 - **AD15*** spared with ADS3 0101–1111 - reserved				
SPARE_ADDR_DATA_4	Req.	R/W	0000	0000	no change
	These bits select which signal to spare with **ADS4**. 0000 - **ADS4** disabled, no sparing 0001 - **AD16*** spared with ADS4 0010 - **AD18*** spared with ADS4 0011 - **AD20*** spared with ADS4 0100 - **AD22*** spared with ADS4 0101–1111 - reserved				
SPARE_ADDR_DATA_5	Req.	R/W	0000	0000	no change
	These bits select which signal to spare with **ADS5**. 0000 - **ADS5** disabled, no sparing 0001 - **AD17*** spared with ADS5 0010 - **AD19*** spared with ADS5 0011 - **AD21*** spared with ADS5 0100 - **AD23*** spared with ADS5 0101–1111 - reserved				
SPARE_ADDR_DATA_6	Req.	R/W	0000	0000	no change
	These bits select which signal to spare with **ADS6**. 0000 - **ADS6** disabled, no sparing 0001 - **AD24*** spared with ADS6 0010 - **AD26*** spared with ADS6 0011 - **AD28*** spared with ADS6 0100 - **AD30*** spared with ADS6 0101–1111 - reserved				
SPARE_ADDR_DATA_7	Req.	R/W	0000	0000	no change
	These bits select which signal to spare with **ADS7**. 0000 - **ADS7** disabled, no sparing 0001 - **AD25*** spared with ADS7 0010 - **AD27*** spared with ADS7 0011 - **AD29*** spared with ADS7 0100 - **AD31*** spared with ADS7 0101–1111 - reserved				

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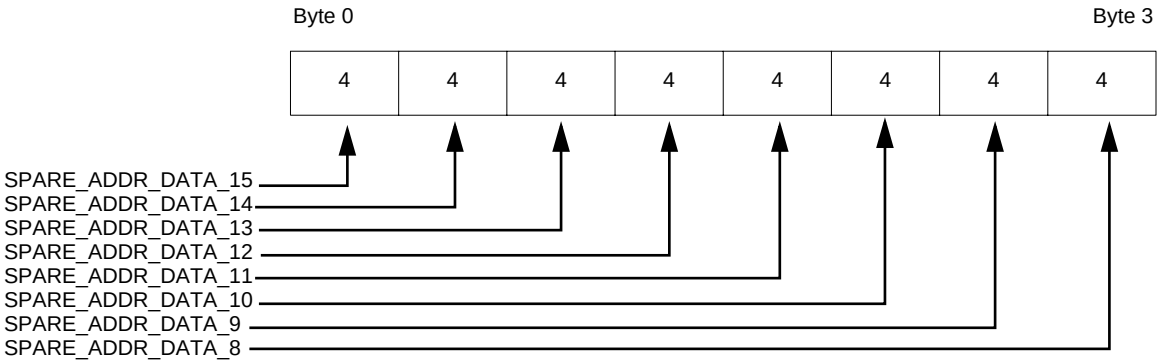

Figure 9-17—SP_ENABLE_SPARES_IV (CSR 692)

Table 9-22—SP_ENABLE_SPARES_IV (CSR 692)

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
SPARE_ADDR_DATA_8	Req.	R/W	0000	0000	no change
These bits select which signal to spare with **ADS8**. 0000 - **ADS8** disabled, no sparing 0001 - **AD32*** spared with ADS8 0010 - **AD34*** spared with ADS8 0011 - **AD36*** spared with ADS8 0100 - **AD38*** spared with ADS8 0101–1111 - reserved					
SPARE_ADDR_DATA_9	Req.	R/W	0000	0000	no change
These bits select which signal to spare with **ADS9**. 0000 - **ADS9** disabled, no sparing 0001 - **AD33*** spared with ADS9 0010 - **AD35*** spared with ADS9 0011 - **AD37*** spared with ADS9 0100 - **AD39*** spared with ADS9 0101–1111 - reserved					
SPARE_ADDR_DATA_10	Req.	R/W	0000	0000	no change
These bits select which signal to spare with **ADS10**. 000 - **ADS10** disabled, no sparing 0001 - **AD40*** spared with ADS10 0010 - **AD42*** spared with ADS10 0011 - **AD44*** spared with ADS10 0100 - **AD46*** spared with ADS10 0101–1111 - reserved					

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Table 9-22—SP_ENABLE_SPARES_IV (CSR 692) *(continued)*

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
SPARE_ADDR_DATA_11	Req.	R/W	0000	0000	no change
These bits select which signal to spare with **ADS11**. 0000 - **ADS11** disabled, no sparing 0001 - **AD41*** spared with ADS11 0010 - **AD43*** spared with ADS11 0011 - **AD45*** spared with ADS11 0100 - **AD47*** spared with ADS11 0101–1111 - reserved					
SPARE_ADDR_DATA_12	Req.	R/W	0000	0000	no change
These bits select which signal to spare with **ADS12**. 0000 - **ADS12** disabled, no sparing 0001 - **AD48*** spared with ADS12 0010 - **AD50*** spared with ADS12 0011 - **AD52*** spared with ADS12 0100 - **AD54*** spared with ADS12 0101–1111 - reserved					
SPARE_ADDR_DATA_13	Req.	R/W	0000	0000	no change
These bits select which signal to spare with **ADS13**. 0000 - **ADS13** disabled, no sparing 0001 - **AD49*** spared with ADS13 0010 - **AD51*** spared with ADS13 0011 - **AD53*** spared with ADS13 0100 - **AD55*** spared with ADS13 0101–1111 - reserved					
SPARE_ADDR_DATA_14	Req.	R/W	0000	0000	no change
These bits select which signal to spare with **ADS14**. 0000 - **ADS14** disabled, no sparing 0001 - **AD56*** spared with ADS14 0010 - **AD58*** spared with ADS14 0011 - **AD60*** spared with ADS14 0100 - **AD62*** spared with ADS14 0101–1111 - reserved					
SPARE_ADDR_DATA_15	Req.	R/W	0000	0000	no change
These bits select which signal to spare with **ADS15**. 0000 - **ADS15** disabled, no sparing 0001 - **AD57*** spared with ADS15 0010 - **AD59*** spared with ADS15 0011 - **AD61*** spared with ADS15 0100 - **AD63*** spared with ADS15 0101–1111 - reserved					

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9.4.3 Profile S ROM CSR extensions

9.4.3.1 PROFILE ID CSR

The **PROFILE ID** CSR (see Figure 9-18 and Table 9-23) indicates which profiles are supported by the module. The PROFILE ID CSR has eight one-byte positions for a module to identify which Profile it is compliant with. Profile S modules shall use the code 0x53 (ASCII “S”) in exactly one of these eight fields. All unused fields shall be set to 0.

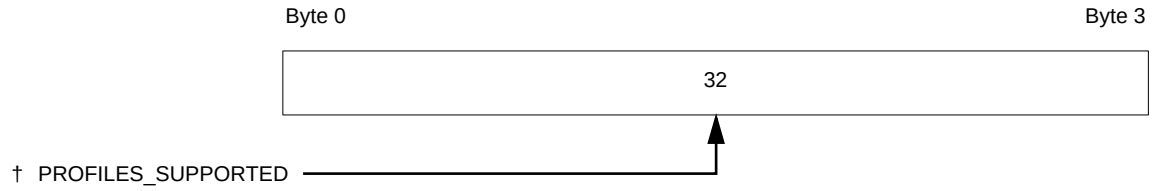

Figure 9-18—PROFILE ID (CSR 1032 or 1036)

Table 9-23—PROFILE ID (CSR 1032 or 1036)

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
PROFILES_SUPPORTED	Req.	R/O	0x53 in one position	0x53 in one position	no change
	These bits are the ASCII representation of “S”. Other byte positions may contain designators for other supported profiles or 0 if not used.				

9.4.3.2 NODE_CAPABILITIES_EXT CSR

The **ECC_CAPABLE** bit (see Figure 9-19 and Table 9-24) is defined in the **NODE_CAPABILITIES_EXT** CSR to indicate that the module supports the Profile S ECC and TMR functionality described in this standard. In IEEE Std 896.2-1991 this bit is reserved. If **ECC_CAPABLE** is one, all facilities defined in this document are supported. There shall be no options. However, as will be noted in the **MAINT_CONTROL** CSR, certain of the facilities can be disabled.

The remainder of the **NODE_CAPABILITIES_EXT** CSR is unchanged.

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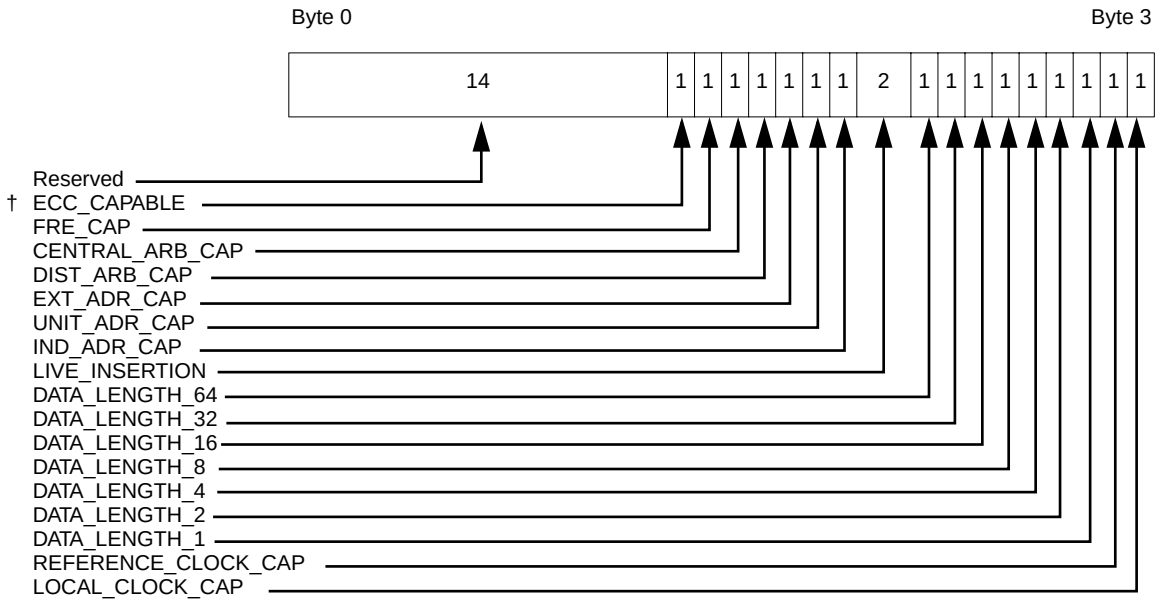

Figure 9-19—NODE_CAPABILITIES_EXT (CSR 1044)

Table 9-24—NODE_CAPABILITIES_EXT (CSR 1044)

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
ECC_CAPABLE	Req.	R/O			
	If one, this bit indicates that the node supports the Profile S ECC and TMR functionality described in this standard.				

9.4.3.3 Clock control

In order to support variable operating frequencies on board space modules, one CSR and one ROM entry have been provided to contain clock parameter information. The **SP_PROCESSOR_CLOCK** (Key=0x30) contains the maximum clock frequency supported by a processor module and is required to be present in the ROM Root Directory. The **SP_CLOCK_CONTROL** (CSR 464) is used to control the clock and is optional (see 9.4.1.5). The exact utilization is implementor dependent.

The **SP_PROCESSOR_CLOCK** ROM Entry (see Figure 9-20 and Table 9-25) is used to hold the maximum clock frequency supported by the processor module. This CSR allows the user to control power (see 9.4.1.5).

9.5 Unit space CSRs

The upper 2048 bytes of the CSR address space is specified as the initial units space. If the total memory requirements for all units residing on a node are less than 2048 bytes, they may be mapped into this area. If more memory is required for the unit architecture, it may be mapped into any available node address space through the **UNITS BASE/BOUND** CSRs (set at system configuration). The unit size information is contained in the **UNITS_EXTENT_ROM** CSR.

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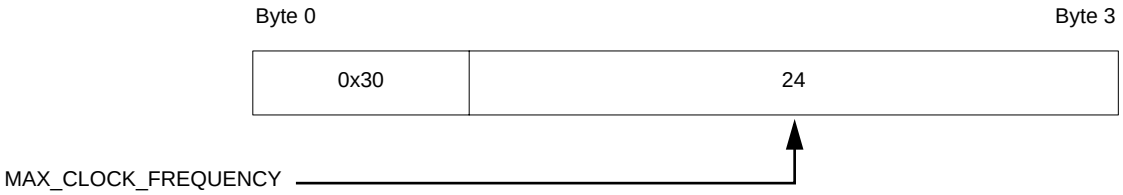

Figure 9-20—SP_PROCESSOR_CLOCK ROM Entry (Key=0x30)

Table 9-25—SP_PROCESSOR_CLOCK ROM Entry (Key=0x30)

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
MAX_CLOCK_FREQUENCY	Req.	R/O			no change
	These bits contain the nominal maximum clock frequency supported by a Profile S module in kilohertz.				

9.5.1 Standard units

All standard units, if implemented, shall be in accordance with ISO/IEC 13213: 1994.

9.5.2 Telemetry units

Modules shall implement at least one telemetry unit. Telemetry units provide a uniform means of accessing node specific parametric information. This information is generally of a health and welfare or configuration nature. Items such as relay position, temperature, current, voltage, and dosimetry are examples of such information. This data may be stored in nonvolatile memory if data retention is required through periods when power is reduced or withheld. Telemetry units shall be read/write accessible through on-module diagnostics, the Serial Bus, and the primary or backup system backplane. Telemetry units are made up of a collection of Parametric Units and/or Configuration Units.

9.5.2.1 Parametric units

All nodes shall have a resident area for health and welfare information. At a minimum, module information will be contained in this space. For cases where a node is performing a control function, information for the controlled system should be available in the node's parametric unit space. Each entry in the parametric unit space will consist of four words structured as shown in Table 9-26. These are further defined in Figures 9-21 through 9-24 and Tables 9-27 through 9-30.

Table 9-26—Parametric data entry

31 24	23 16	15 8	7 0
SYSTEM SPECIFIC		TELEMETRY TYPE	
SENSOR DATA			
ACTION REQUIRED			
ACTION REQUIRED THRESHOLD			

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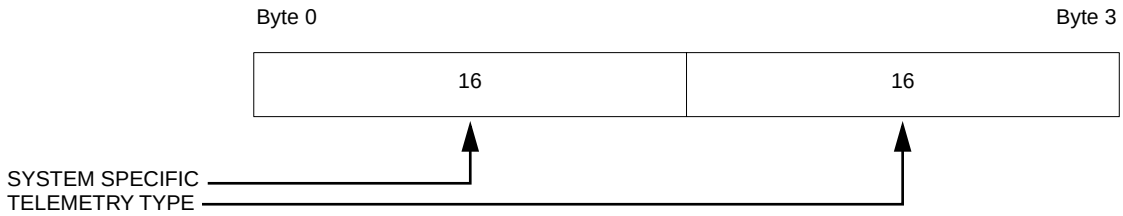

Figure 9-21—Telemetry entry word 1

Table 9-27—Telemetry entry word 1

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
SYSTEM_SPECIFIC	Opt.	R/O			no change
	These bits contain specific information about the telemetry word and are defined by the using system.				
TELEMETRY_TYPE	Req.	R/O			no change
	These bits contain the type of telemetry data that this entry represents and are defined by the using system.				

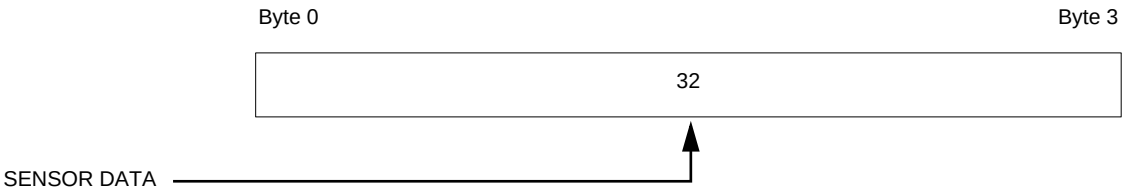

Figure 9-22—Telemetry entry word 2

Table 9-28—Telemetry entry word 2

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
SENSOR_DATA	Opt.	R/O			no change
	These bits contain any sensed data for this telemetry entry and are defined by the using system.				

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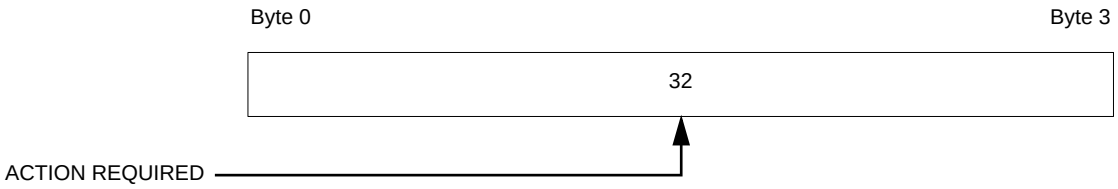

Figure 9-23—Telemetry entry word 3

Table 9-29—Telemetry entry word 3

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
ACTION_REQUIRED	Opt.	R/O			no change
These bits contain an action code value.					

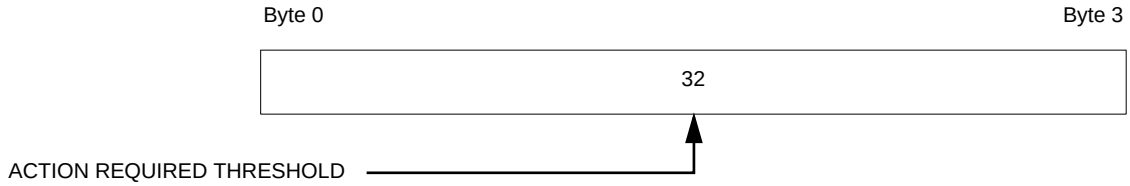

Figure 9-24—Telemetry entry word 4

Table 9-30—Telemetry entry word 4

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
ACTION_REQUIRED THRESHOLD	Opt.	R/O			no change
These bits contain an action code threshold value and are defined by the using system.					

9.5.2.2 Configuration units

Configuration units are intended to provide actual and commanded status and physical configuration information on host nodes and controlled systems or subsystems. Items such as relay or valve position indication, primary or redundant system active, last built-in test results, etc., are possible. Each entry in the configuration units space will adhere to the one-word format shown in Table 9-31. These are further explained in Figure 9-25 and Table 9-32.

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Table 9-31—Configuration data entry word

31	24	23	16	15	8	7	0
DEVICE IDENTIFIER				ORDERED		ACTUAL	

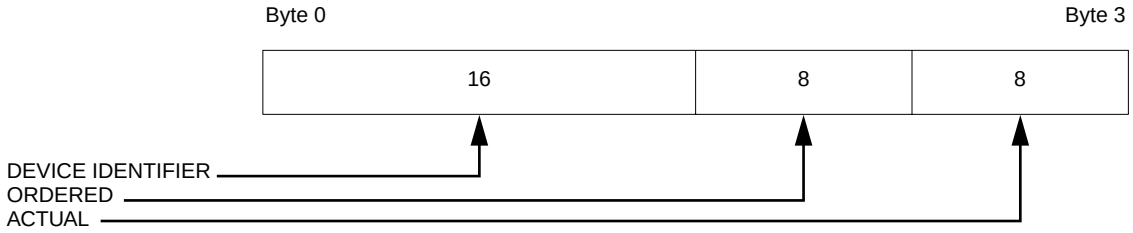

Figure 9-25—Configuration data entry

Table 9-32—Configuration data entry

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
DEVICE IDENTIFIER	Req.	R/O			no change
	These bits identify the specific device to which the data pertains.				
ORDERED	Req.	R/O			no change
	These bits contain the command that was ordered.				
ACTUAL	Req.	R/O			no change
	These bits contain the actual command that was executed.				

9.5.3 Alternate access units

It shall be possible to access CSRs from either Futurebus+ or Serial Bus interface. This is accomplished using an Alternate Access Unit (AAU) as described in IEEE Std 896.9-1994 and ISO/IEC 13213: 1994. Two AAUs shall be implemented in any Profile S module: A Futurebus+ Alternate Access Unit and a Serial Bus Alternate Access Unit.

An Alternate Access Unit is a type of unit architecture that defines access between multiple ISO/IEC 13213: 1994 compliant buses when they share a common module. An AAU is simply a port into a portion of the local resources of the node sharing the module. An AAU should not be confused with a bridge that has more capability and complexity. The AAU framework is general enough to allow for any number of ISO/IEC 13213: 1994 compliant buses to access one another's CSRs and/or units. The purpose of this framework is to provide a general access method that will be used to specify individual AAUs. A full AAU architecture must be specified for each type of AAU just as is the case for any other standard unit architecture. All items shall be in accordance with ISO/IEC 13213: 1994 standard units.

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There are two classes of AAUs—Node and Unit. Node AAUs specify alternate access to the CSR space of the nodes that share the module. Unit AAUs specify alternate access to a unit that is shared between nodes on a module.

A Node AAU may be used when access to a node's CSRs is required from another bus. An example of this is the use of the Serial Bus as a diagnostic path in a Futurebus+ system. The diagnostic path would require access to the CSRs of the Futurebus+ node to activate module tests and to acquire test results. A Unit AAU may be used when units need to be shared between buses.

This AAU framework specification makes restrictions on AAU units to simplify and standardize their implementation (see Figure 9-26):

a) The location of the AAU shall be described in the node's ROM space as per ISO/IEC 13213: 1994 ROM Format specification. This is required of all standard units.
b) A node class AAU shall be limited to the first 2 kB of CSR space. Units in the initial unit space may be accessed by using a separate Unit class AAU.
c) A separate unit specification is required for each type of AAU unit. This is required of all standard units.
d) The location of the AAU shall be limited to the indirect space. To access the alternate node's CSR space, or units, the indirect address and indirect data register pair must be used. However, the local access (between nodes on the same module) is implementation specific and beyond the scope of this standard.
e) The AAU access shall be limited to module resources only, and shall not cause or generate bus transactions.

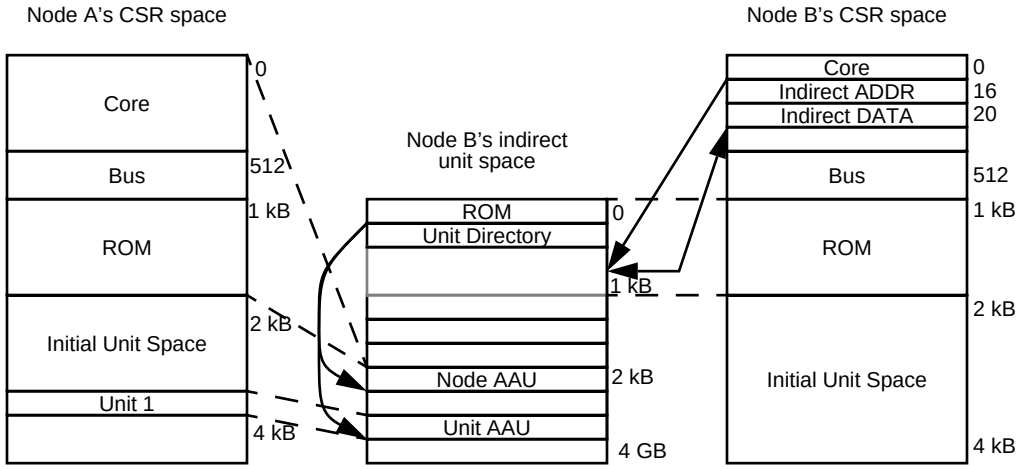

Figure 9-26—AAU mapping

9.5.4 Futurebus+ alternate access unit

A Futurebus+ Alternate Access Unit shall be provided that permits access of Futurebus+ CSRs on a Profile S module through the Serial Bus interface. This is described in IEEE Std 896.9-1994 and ISO/IEC 13213: 1994.

Profile S modules shall implement a node AAU that allows the Serial Bus node access to the Futurebus+ node's CSRs: the Futurebus+ Alternate Access Unit (FBAAU). The FBAAU is a unit architecture that resides in the indirect-address space of the Serial Bus node. The FBAAU is typically used to access Futurebus+ CSRs from the Serial Bus for maintenance purposes.

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Any node on the Serial Bus (or node that has access via a bridge) may access the FBAAU through the indirect address and data registers of the Serial Bus node that shares the module. Futurebus+ access shall include all Futurebus+ CSR registers that consist of the first 2 kB of the Futurebus+'s initial node address space. Reading and writing these registers via the indirect register pair as an alternate path shall have the same effect as reads and writes from the Futurebus+ node itself. The FBAAU is defined as a unit in the ROM specification of the Serial Bus node. A unit directory shall be implemented in ROM for the FBAAU. The exact offset from the start of the indirect space is determined by the module's vendor, and programmed into the ROM root directory.

The FBAUU ROM unit directory shall be programmed as specified in Table 9-33. Other entries may optionally be present pursuant to ISO/IEC 13213: 1994.

Table 9-33—Required FBAAU ROM unit directory entries

Key	Entry	Comments
0x12	UNIT_SPEC_ID	This entry shall be supplied by the vendor as acquired through the IEEE (see ISO/IEC 13213: 1994 and Clause 3 of IEEE Std 896.2-1991).
0x13	UNIT_SW_VERSION	This entry shall be supplied by the vendor.
0x15	UNIT_LOCATION	This entry is the offset to the UNIT_LOCATE leaf. The exact offset is determined by the vendor pursuant to ISO/IEC 13213: 1994.

The FBAAU UNIT_LOCATE leaf shall be programmed as specified in Table 9-34.

Table 9-34—FBAAU Unit_Locate leaf values

Field	Value	Comments
LENGTH	4	
CRC-16		The CRC shall be provided by the vendor and shall be calculated as per ISO/IEC 13213: 1994.
base64_hi/base64_lo		The vendor shall provide the address offset from the start of indirect memory, where the AAU shall reside.
bound64_hi/bound64_lo		The vendor shall provide the bound address offset from the start of indirect memory, where the AAU shall reside (bound64 is one larger than the last unit added).
TAG	10 (binary)	

9.5.5 Serial bus alternate access unit

A Serial Bus Alternate Access Unit shall be provided that permits access of Serial Bus CSRs on a Profile S module through the Futurebus+ interface. This is described in IEEE Std 896.9-1994 and ISO/IEC 13213: 1994.

Profile S modules shall implement a node AAU that allows the Futurebus+ node access to the Serial Bus node's CSRs: the Serial Bus Alternate Access Unit (SBAAU). The SBAAU is a unit architecture that resides

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in the indirect-address space of the Futurebus+ node. The SBAAU is typically used to access Serial Bus CSRs from the Futurebus+ for maintenance purposes.

Any node on the Futurebus+ (or node that has access via a bridge) may access the SBAAU through the indirect address and data registers of the Futurebus+ node that shares the module. Serial Bus access shall include all Serial Bus CSR registers that consist of the first 2 kB of the Serial Bus's initial node address space. Reading and writing these registers via the indirect register pair as an alternate path shall have the same effect as reads and writes from the Serial Bus node itself. The SBAAU is defined as a unit in the ROM specification of the Futurebus+ node. A unit directory shall be implemented in ROM for the SBAAU. The exact offset from the start of the indirect space is determined by the module's vendor, and programmed into the ROM root directory.

The SBAUU ROM unit directory shall be programmed as specified in Table 9-35. Other entries may optionally be present pursuant to ISO/IEC 13213: 1994.

Table 9-35—Required SBAAU ROM unit directory entries

Key	Entry	Comments
0x12	UNIT_SPEC_ID	This entry shall be supplied by the vendor as acquired through the IEEE (see ISO/IEC 13213: 1994 and Clause 3 of IEEE Std 896.2-1991).
0x13	UNIT_SW_VERSION	This entry shall be supplied by the vendor.
0x15	UNIT_LOCATION	This entry is the offset to the UNIT_LOCATE leaf. The exact offset is determined by the vendor pursuant to ISO/IEC 13213: 1994.

The SBAAU UNIT_LOCATE leaf shall be programmed as specified in Table 9-36.

Table 9-36—SBAAU Unit_Locate Leaf values

Field	Value	Comments
LENGTH	4	
CRC-16		The CRC shall be provided by the vendor and shall be calculated according to ISO/IEC 13213: 1994.
base64_hi/base64_lo		The vendor shall provide the address offset from the start of indirect memory, where the AAU shall reside.
bound64_hi/bound64_lo		The vendor shall provide the bound address offset from the start of indirect memory, where the AAU shall reside (bound64 is one larger than the last unit added).
TAG	10 (binary)	

9.5.6 Futurebus+ isolate control unit

The Futurebus+ Isolate Control Unit (FBICU) shall be implemented to enable and disable the Futurebus+ transceivers. This unit shall contain a single CSR. The CSR shown in Figure 9-27 and described in Table 9-37 shall provide control of the enabling and disabling of the Futurebus+ transceivers. It is recommended that this CSR be located within the Serial Bus node's initial units space.

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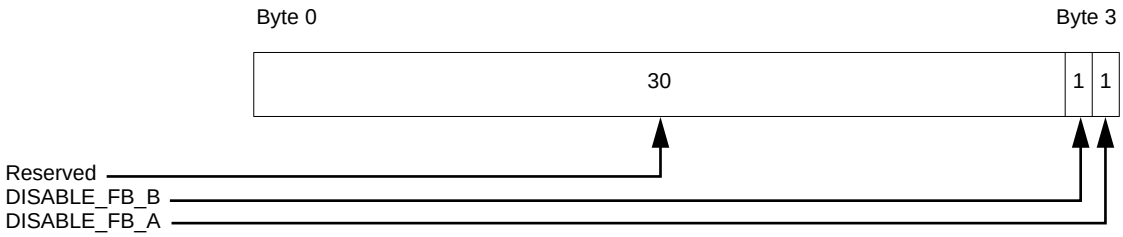

Figure 9-27—Isolate control unit CSR

Table 9-37—Futurebus+ isolate control unit CSR

Bit field	Req./Opt.	Access type	Power up	System reset	Bus initialize
DISABLE_FB_A	Req.	R/W	0	0	no change
	When this bit is set to one, the primary Futurebus+ node transceivers shall be isolated from the Futurebus+ backplane such that the node is not allowed to assert any Futurebus+ signals. Note, that the module should still perform a system reset received via **RE*/RED*** if possible. The System software is expected to set the **DISABLE_FB_A** bit to isolate a faulty Futurebus+ node from the backplane.				
DISABLE_FB_B	Reserved if only one Futurebus+ node is present. Required if two Futurebus+ nodes are present.	R/W	0	0	no change
	When this bit is set to one, the secondary Futurebus+ node transceivers shall be isolated from the Futurebus+ backplane such that the node is not allowed to assert any Futurebus+ signals. Note, that the module should still perform a system reset received via **RE*/RED*** if possible. The System software is expected to set the **DISABLE_FB_B** bit to isolate the faulty Futurebus+ node from the backplane. NOTE—This bit is only implemented on modules that have two Futurebus+ nodes.				

9.6 Serial Bus management

This subclause describes the bus management requirements for Profile S's Serial Bus interface. A summary of these bus management requirements is listed in Table 9-38.

The selection of a Serial Bus master to perform the start-up configuration/initialization process and the system maintenance process is implementation dependent. At any given time only one Serial Bus master should have configuration and maintenance responsibility. Furthermore, that manager should not be contained on the same module as the Futurebus+ Monarch or a second Serial Bus Manager. In many system implementations, the selection of a configuration manager should be deterministic. Therefore, the automatic configuration manager selection scheme specified in IEEE Std 1394-1995 is optional. If an automatic selection scheme is implemented in an interface, it shall be possible to disable the scheme.

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Table 9-38—Serial Bus management referenced standards

Function	Standard	Parameter	Comments
Configuration Manager	IEEE Std 1394-1995	Optional	
Core CSRs	IEEE Std 1394-1995, ISO/IEC 13213: 1994	As required	
Serial Bus Dependent CSRs	IEEE Std 1394-1995	As required	
ROM CSRs	IEEE Std 1394-1995, ISO/IEC 13213: 1994	Required	At least the “General ROM Format”
Futurebus+ Isolate Control Unit	IEEE Std 896.10-1997	Required	
Alternate Access Unit to Futurebus+ CSRs	IEEE Std 896.10-1997	Required	

9.6.1 Module design

The Serial Bus is an important maintenance access interface to Profile S modules. A Profile S Serial Bus implementation should be robust and minimize the chance of a module failure preventing Serial Bus access. Serial Bus and associated logic should not share logic devices with other module circuitry. For example, the Serial Bus signals, **SB0*** and **SB1***, should be in a transceiver device separate from any Futurebus+ signals. The AAUs (SBAAU and FBAAU) should rely on a minimum set of logic to avoid the likelihood of a module failure preventing access to Futurebus+ CSRs. For example, the AAUs should not rely on a processor in the module’s main functional logic to assist in accesses.

The primary purpose of Profile S’s Serial Bus is for module maintenance, alternate access, and test, and it is not recommended that the specified Serial Bus be used otherwise. Additional application specific interfaces such as a cable Serial Bus interface are allowed but are beyond the scope of this standard.

9.6.2 Other extensions

The specified Serial Bus interface along with its CSRs and access to Futurebus+ CSRs provides a base level of capabilities. If a vendor wishes to implement additional capabilities, the vendor is free to do so. These additional capabilities shall not interfere with the base level of capabilities. Extensions such as JTAG interface, software debug, history logs, error reporting, and fault tolerant recovery are possible, but are not specified by this standard.

Extending a Serial Bus out of a single backplane environment with bus bridging is allowed but is beyond the scope of this standard.

Profile S backplanes shall be wired with two Serial Bus pins per Futurebus+ bus. Error Correcting configuration backplanes shall be wired with two Serial Buses of two pins each. Profile S modules shall implement a Serial Bus for each implemented Futurebus+. Error Correcting configuration modules shall implement two Serial Buses of two pins each.

9.7 Private space

The private space is allocated for vendor-dependent node-local uses per ISO/IEC 13213: 1994. Private space addresses shall use Exxxxxxx (32-bit extended) and FFFFFFFF Exxxxxxx (64-bit extended).

Some nodes may need to allocate private space for internal uses in a way that makes the private space on the bus inaccessible to these nodes. Such nodes, which are said to implement the private space, shall not gener-

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ate bus transactions with addresses in the private space. Instead, transactions with private space addresses shall be routed to node-local resources (such as boot ROM or peripherals).

Nodes that do not implement the private space may access these addresses on the bus. However, software is expected to constrain the assignment of extended spaces within the private space, since these bus addresses cannot be accessed by those nodes that implement the private space option.

9.8 Interrupts

If Profile S modules generate interrupts, IEEE Std 896.2-1991 requires that they shall support the interrupt mechanism defined in IEEE Std 896.2-1991. Nodes generate interrupts by writing a 32-bit (4 byte) datum to an assigned 32-bit CSR address; the CSR address and interrupt datum (a vector, for example) are assigned at system configuration time. Writes to the interrupt address may return busy status if there is a short-term condition (such as a queue of interrupts that is temporarily full) that prevents the responding node from logging the interrupt.

9.9 Diagnostics and test

All Profile S modules shall implement built-in self-test. Test coverage should be stated in product literature; coverage of at least 90% of detectable faults is recommended. The interface to built-in tests shall be through the diagnostic registers defined earlier in this subclause.

9.10 Monarch selection

Although all modules need not be monarch capable, all modules shall support a standard monarch selection method so that they may be used in systems that implement this process. The monarch is responsible for low-level bus parameters as required to facilitate system boot. Once system software is operating, that software may choose to select a new monarch. However, system software operation is beyond the scope of this standard.

The Profile F monarch selection process shall be used.

9.10.1 Monarch selection process

In order to simplify the “cold-start” of a system, it may be necessary to select a single processor (monarch) to run a configuration initialization process.

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10. Detailed specification, physical layer—SEM-E Stretch

10.1 Mechanical

The physical characteristics for the SEM-E Stretch module shall be in accordance with IEEE Std 1101.7-1995. Whenever the highest module bus I/O requirements are present, the 396-pin connector version shall be used. Otherwise, the 372-pin connector version should be used due to its superior mounting, EMI, and keying capabilities. (See Clause 17 for all the details of this connector.) Critical requirements between the module and the subrack shall also be as outlined in IEEE Std 1101.7-1995.

10.1.1 Unoccupied slots

The system integrator is responsible for ensuring that a configuration having unoccupied slots meets the internal environmental standards specified in IEEE Std 1156.4-1997. Additionally, it is the integrator's responsibility to ensure that all applicable EMI standards are met for the applications in which the systems are intended to operate.

10.1.2 Backplane capacity

The backplane and subrack assembly shall support no more than 31 slots.

The space working group has used 14 slots as a "typical" system size and has used this number for electrical studies. Because mechanical analysis is completely system-dependent, no mechanical or thermal analyses performed by the working group should be substituted for this analysis. This analysis should be supported by product literature.

10.1.3 Injector/Elector mechanism

If insertion/extraction levers are used, they shall be retained so that they do not rattle during shock and random vibration.

10.2 Input/Output

If there are non-Futurebus+ signals passing into or out of a SEM-E Stretch module, those signals should connect through the backplane user I/O area. Connection to dual or redundant or secondary buses on the backplane is permitted for SEM-E Stretch modules.

10.3 Profile connector, power, and signal pin assignments

10.3.1 Connector naming conventions and connector assignment

Figure 10-1 shows the connector naming convention for SEM-E Stretch modules. The entire connector consists of 50 rows (1–50) and 8 columns (a–h) of pins and is built from 10 segments, each 5 rows by 8 columns. For pinout reference, the connector is partitioned into six sections: C, D, E, F, G, and H. Sections C and D consist of 5 rows by 4 columns (20 pin locations) each. Sections E and F consist of 11 rows by 4 columns (44 pin locations) each. Sections G and H consist of 34 rows by 4 columns (136 pin locations) each. These connector sections are defined for both the SEM-E Stretch Dual Futurebus+ and the SEM-E Stretch Error Correcting configuration. The SEM-E Stretch Single 32-bit and SEM-E Stretch Single 64-bit Futurebus+ profiles are modifications of these two base definitions. For all implementations, sections C and D may optionally contain fiber connections. Connector section E contains two optional dual-redundant MIL-STD-1553 serial buses and user-defined I/O. Connector section F contains user-defined I/O only. Connector section G contains the data, control, utility, and arbitration lines needed to implement a Single 32-bit Future-

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bus+. This section is also used for the Futurebus+ 1 Bus in the Dual Bus Futurebus+ configuration. In the Error Correcting configuration, connector section G contains the data lines and the base copy of the control, utility, and arbitration lines. Connector section G contains 28 V power connections in all configurations. Connector section H contains the data, control, utility, and arbitration lines needed for the Futurebus+ 2 bus in the Dual Bus configuration. In the single bus configurations, connector section H contains the required data lines for the 64-bit bus and user-defined I/O lines. In the Error Correcting configuration, connector section H contains the A and B copies of the control, utility, and arbitration lines, and the spare lines. In all configurations, connector section H contains 28 V power connections. Power (+5 V and +3.3 V) and ground are distributed across all connector sections.

Pins are referenced by row number and column letter as shown. Pin locations 1a and 1c do not exist and are replaced by the first or alpha key. Pin locations 50b and 50d also do not exist and are replaced by the second or beta key. The total number of pins in the connector is 396. Sides “A” and “B” of the connector are referenced as shown in Figure 10-1. Pins in each row (a–h) are alternately staggered vertically as shown in Figure 10-1.

All connector views in this section show the backplane connector pinout as seen from the front of the rack. Note that other documents may refer to a through h as rows and 1 through 50 as columns. The convention described above was chosen in order to simplify the connector figures in this document and is consistent with the Futurebus+ Military Profile, ISO/IEC 14536: 1995.

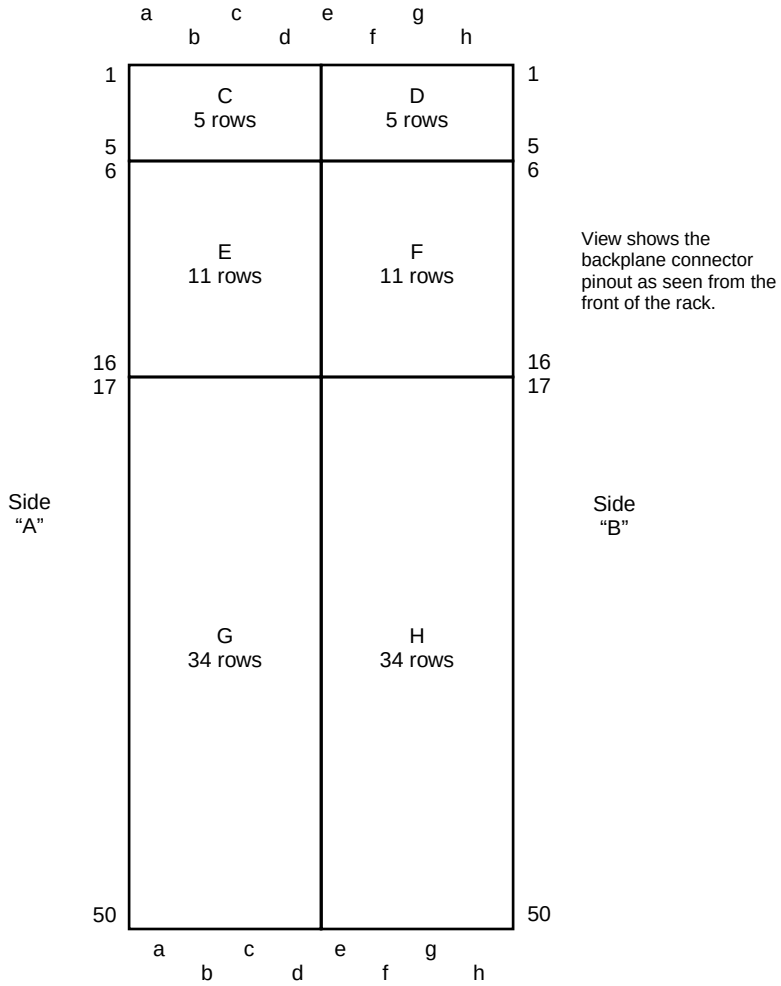

Figure 10-1—Module SEM-E Stretch connector naming conventions

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10.3.2 Signal pin assignments

Initial attempts were made to develop a space profile pin definition that matched the military profile. This proved impossible for the following reasons. First, the military profile requires many more power and ground connections due to the high power dissipation of the modules. Second, the military profile does not support the Error Correcting configuration or have adequate spare lines.

Work was done with the pinouts to allow easy card layout for all possible transceiver implementations (using 8-bit and 9-bit transceivers and separate protocol chips). The pinouts allow for a discrete interface where individual transceivers and separate protocol chips are used, a completely integrated interface where transceivers and protocol chips are combined in the same package, and a range of partially integrated implementations between these two extremes. Due to the limited space on SEM-E Stretch cards, a partially or completely integrated interface is recommended.

Whenever possible, signals overlap between the SEM-E Stretch Dual Futurebus+, the SEM-E Stretch Error Correcting configuration, the SEM-E Stretch Single 32-bit Futurebus+, and the SEM-E Stretch Single 64-bit Futurebus+. Figures 10-2 through 10-5 show how the signals are distributed on the connector for the SEM-E Stretch module configurations.

User-Defined I/O signals are shown in Figures 10-2 through 10-5. These allow maximum flexibility for non-bused signals and are defined in connector sections E–H. When the optional central arbiter or MIL-STD-1553 bus is implemented, some, most or all of the user-defined I/O pinouts are utilized to provide the additional signal paths required. See 10.3.3 for the definition of the Central Arbitration usage of user-defined I/O for that module.

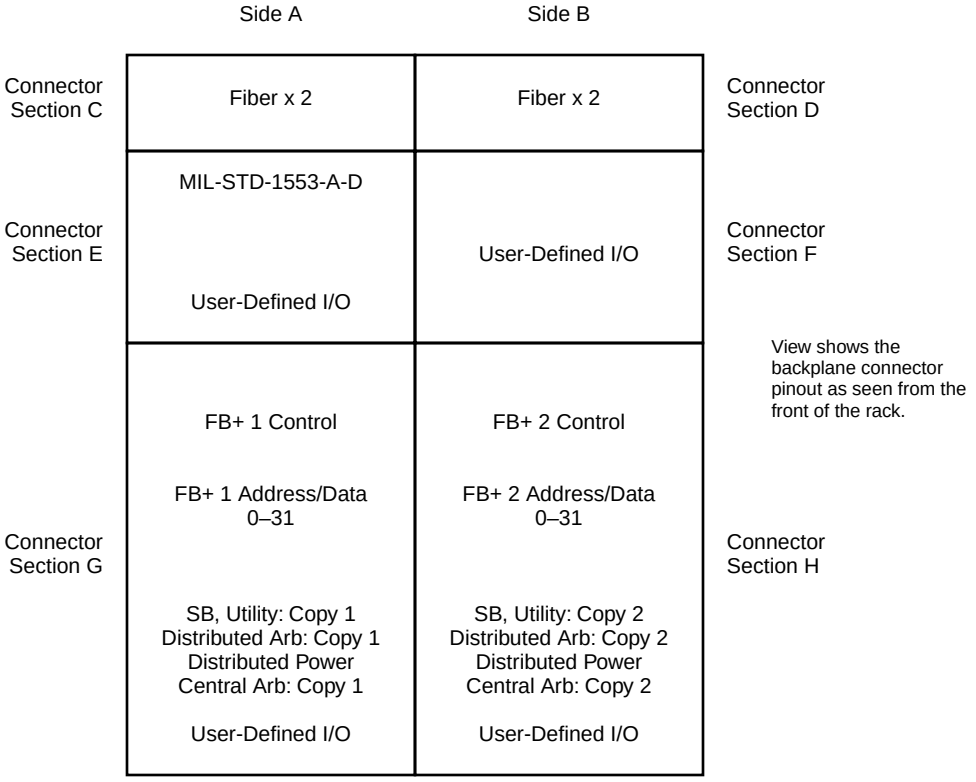

Figure 10-2—Module SEM-E Stretch connector usage (Dual Futurebus+)

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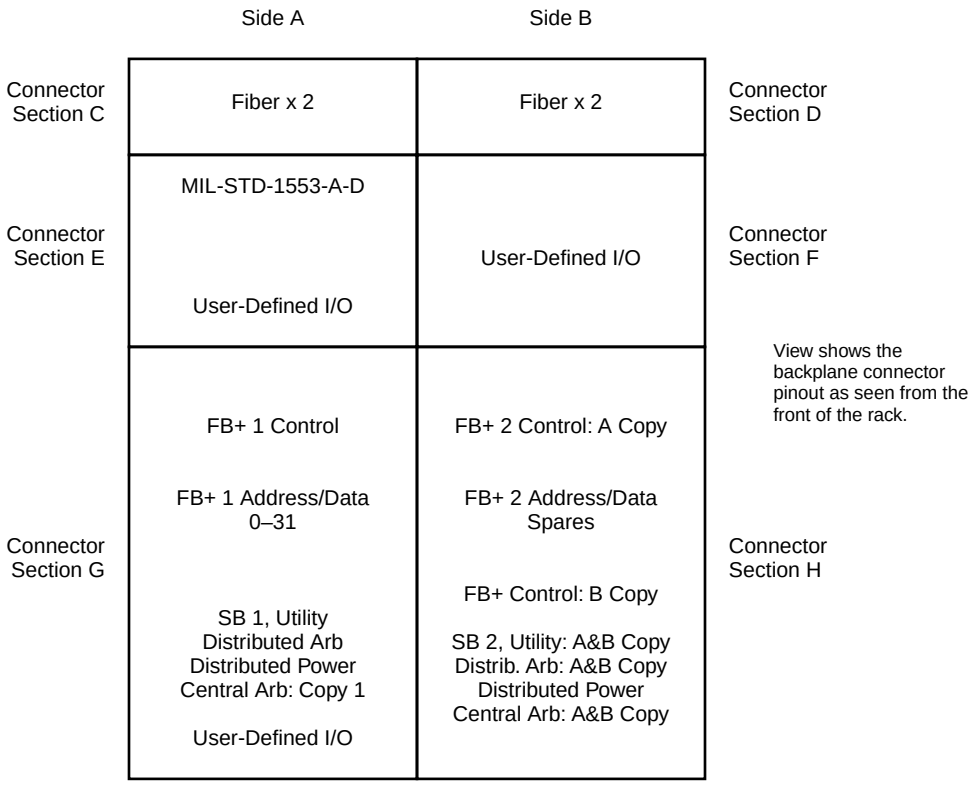

Figure 10-3—Module SEM-E Stretch connector usage (Error Correcting configuration)

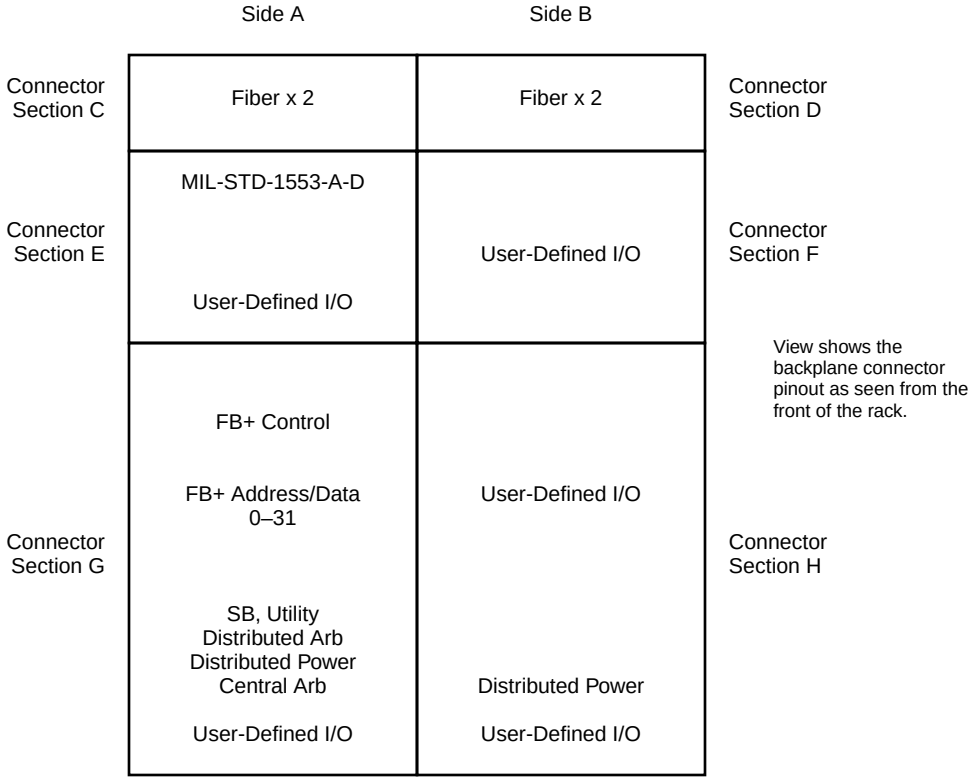

Figure 10-4—Module SEM-E Stretch connector usage (Single 32-bit Futurebus+)

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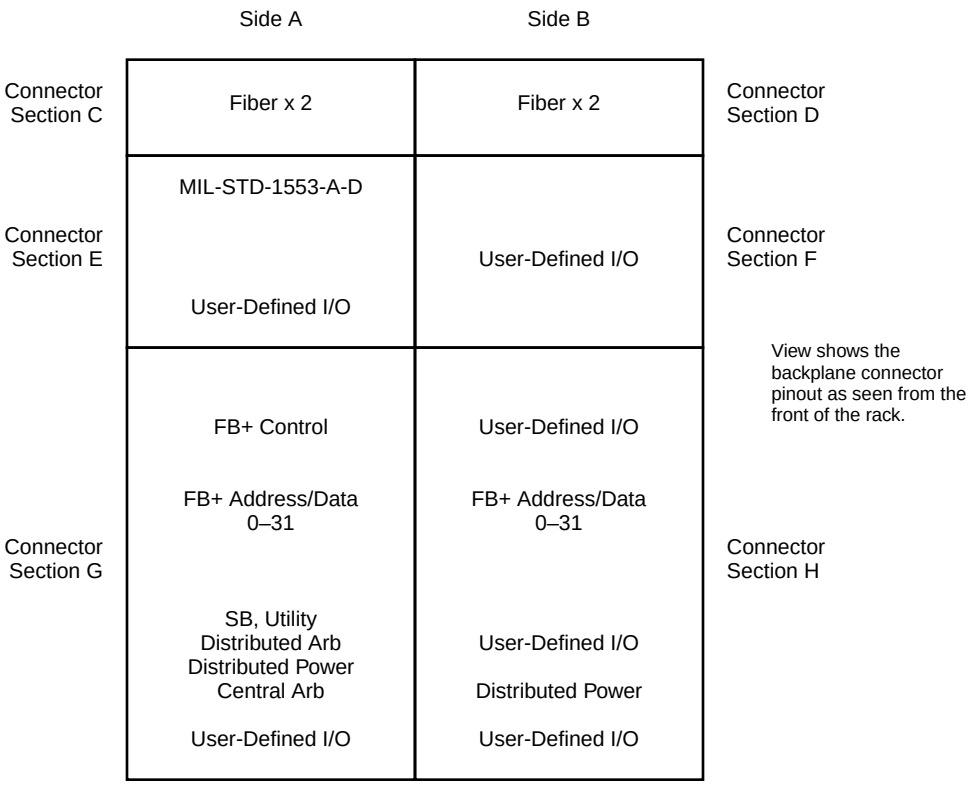

Figure 10-5—Module SEM-E Stretch connector usage (Single 32-bit Futurebus+)

10.3.2.1 Connector sections C and D

If fiber is implemented, connector sections C and D shall be used for the four fiber connections. These pins replace one segment of the connector. The connector only supports a fiber segment at one end of the connector. This resulted in the choice of sections C and D. This implies two fiber connections for each side of the card. If the fiber connections are not implemented, the original connector section may be used for user-defined I/O.

Figures 10-6 and 10-7 show the pinouts for sections C and D for all connector definitions. If used for fiber, section C shall contain a keying pin occupying two pin locations and two fiber connections. Section D shall also contain two fiber connections. If the fiber connections are not implemented, section C shall contain 15 user-defined connections, two keying location pins, one +5 V connection, one +3.3 V connection, and one ground connection. Similarly, section D shall contain 17 user-defined connections, one +5 V connection, one +3.3 V connection, and one ground connection.

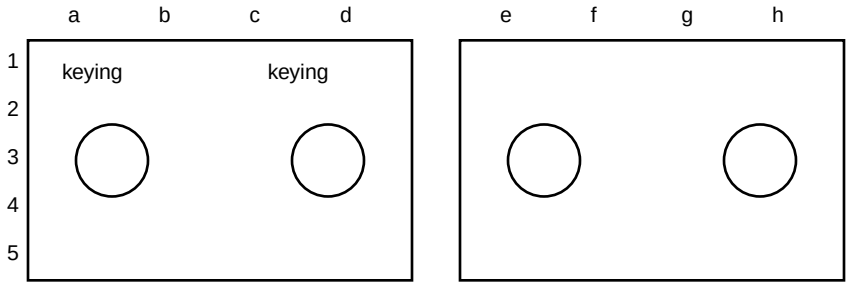

Figure 10-6—SEM-E Stretch sections C and D with fiber connections

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	a	b	c	d	e	f	g	h
1	KEY	User I/O*	KEY	GND	User I/O*	User I/O*	User I/O*	GND
2	User I/O*	User I/O*	User I/O*	User I/O*	User I/O*	User I/O*	User I/O*	User I/O*
3	User I/O*	User I/O*	3.3 V	User I/O*	User I/O*	User I/O*	3.3 V	User I/O*
4	User I/O*	User I/O*	User I/O*	User I/O*	User I/O*	User I/O*	User I/O*	User I/O*
5	User I/O*	5 V	User I/O*	User I/O*	User I/O*	5 V	User I/O*	User I/O*

Figure 10-7—Pinout for SEM-E Stretch connector sections C and D without fiber

10.3.2.2 Connector section E

Due to the proliferation of the MIL-STD-1553B interface in the space community, connector section E contains one optional dual-redundant MIL-STD-1553B serial buses as shown in Figure 10-8. The remainder of section E is used for user-defined I/O as shown in Figure 10-9. If the MIL-STD-1553B interface is not used, Figure 10-10 shows user-defined I/O covering the entire connector section E. To use a specific bus with external transformers, the Bus X+ and Bus X– signals should be used. Either a direct-coupled or transformer-coupled implementation may be used. To use a specific bus on the other side of a transformer, the Bus X dc+ and Bus X dc– should be used. Only one of these are required to be used for a given bus X.)

	a	b	c	d
6				
7	GND			
8		Bus A–	Bus B–	GND
9		Bus A dc+		
10		Bus A+	2.1 V	Bus B+
11		Bus A dc–	Bus B dc+	Bus B dc–
12		5 V		
13				
14	GND			
15				GND
16				

Figure 10-8—Pinout for SEM-E Stretch connector section E (with MIL-STD-1553B)

	a	b	c	d
6	User I/O*	User I/O*	User I/O*	User I/O*
7		User I/O*	User I/O*	User I/O*
8	User I/O*			
9	User I/O*		User I/O*	User I/O*
10	User I/O*			
11	User I/O*			
12	User I/O*		User I/O*	User I/O*
13	User I/O*	User I/O*	User I/O*	User I/O*
14		User I/O*	User I/O*	User I/O*
15	User I/O*	User I/O*	User I/O*	
16	User I/O*	User I/O*	User I/O*	User I/O*

Figure 10-9—User-Definable I/O for SEM-E Stretch connector section E (with MIL-STD-1553B)

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	a	b	c	d
6	User I/O*	User I/O*	User I/O*	User I/O*
7		User I/O*	User I/O*	User I/O*
8	User I/O*	User I/O*	User I/O*	
9	User I/O*	User I/O*	User I/O*	User I/O*
10	User I/O*	User I/O*		User I/O*
11	User I/O*	User I/O*	User I/O*	User I/O*
12	User I/O*		User I/O*	User I/O*
13	User I/O*	User I/O*	User I/O*	User I/O*
14		User I/O*	User I/O*	User I/O*
15	User I/O*	User I/O*	User I/O*	
16	User I/O*	User I/O*	User I/O*	User I/O*

Figure 10-10—User-Definable I/O for SEM-E Stretch connector section E (without MIL-STD-1553B)

10.3.2.3 Connector section F

Connector section F contains user-defined I/O as shown in Figure 10-11.

	e	f	g	h
6	User I/O*	User I/O*	User I/O*	User I/O*
7		User I/O*	User I/O*	User I/O*
8	User I/O*	User I/O*	User I/O*	
9	User I/O*	User I/O*	User I/O*	User I/O*
10	User I/O*	User I/O*		User I/O*
11	User I/O*	User I/O*	User I/O*	User I/O*
12	User I/O*		User I/O*	User I/O*
13	User I/O*	User I/O*	User I/O*	User I/O*
14		User I/O*	User I/O*	User I/O*
15	User I/O*	User I/O*	User I/O*	
16	User I/O*	User I/O*	User I/O*	User I/O*

Figure 10-11—User-Definable I/O for SEM-E Stretch connector section F

10.3.2.4 Connector section G

Connector section G shall contain the Futurebus+ data, control, utility, and arbitration signals. In the SEM-E Stretch Dual Futurebus+ configuration, connector section G shall be used for Futurebus+ 1, power, ground, and two key pins. In the SEM-E Stretch Error Correcting configuration implementation, connector section G shall be used for a single 32-bit Futurebus+, power, ground, and two key pins. The Single 32-bit Futurebus+, is a subset of either the Dual Futurebus+ or the Error Correcting configuration implementations. This is possible because the same pin locations are used for common pins in both the Dual Futurebus+ and the Error Correcting configuration pin assignments.

Connector section G shall also be used for central arbitration signals, distributed arbitration signals, power, and ground. Modules shall support central arbitration, but distributed arbitration is optional. If distributed arbitration is not implemented, the pins may be used for user-defined I/O. All SEM-E Stretch configurations provide at least one set of all central and distributed arbitration signals for each bus implemented.

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Figures 10-12 through 10-14 show the implementations for the SEM-E Stretch configurations in section G. Figures 10-15 through 10-17 show the user-definable I/O signal locations for each SEM-E Stretch configuration in section G. Note that all signals in section G (except **PN** and the sparing pins) are active low.

The I/Os shown with an asterisk in Figures 10-15 through 10-17 are very few in number and isolated from the larger groups on other sections of the connector.

	a	**b**	**c**	**d**
17	1-RF*	1-SLD*	3.3 V	1-TED*
18	1-AI*	1-AK*	1-AS*	1-ET*
19	1-DI*	5 V	1-DK*	1-DS*
20	1-CA0*	1-CA1*	1-CA2*	1-CP*
21	GND	1-CM0*	1-CM1*	1-CM2*
22	1-CM3*	1-CM4*	1-CM5*	GND
23	1-CM6*	1-CM7*	1-ST0*	1-ST1*
24	1-ST2*	1-ST3*	3.3 V	1-ST4*
25	1-ST5*	1-ST6*	1-ST7*	
26	1-AD2*	5 V	1-AD1*	1-AD0*
27	1-AD5*	1-AD4*	1-AD3*	1-BP0*
28	GND	1-AD7*	1-AD6*	1-AD8*
29	1-AD11*	1-AD10*	1-AD9*	GND
30	1-AD14*	1-AD13*	1-AD12*	1-AD15*
31	1-AD17*	1-AD16*	3.3 V	1-BP1*
32	1-AD21*	1-AD20*	1-AD19*	1-AD18*
33	1-AD23*	5 V	1-AD22*	1-BP2*
34	1-AD27*	1-AD26*	1-AD25*	1-AD24*
35	GND	1-AD30*	1-AD29*	1-AD28*
36	1-RE*	1-BP3*	1-AD31*	GND
37	1-SB0*	1-TR0*	1-TR1*	1-SB1*
38	1-NED*	1-PFI*	3.3 V	1-UMP*
39	1-RUN*	1-PN	1-SR*	
40	1-RED*	5 V		1-AR*
41	1-AQ*	1-AP*	1-AC0*	1-AC1*
42	GND	1-ABP*	1-AB0*	1-AB1*
43	1-AB2*	1-AB3*	1-AB4*	GND
44	1-AB5*	1-RTN-B	1-AB6*	1-28 V-B
45	1-28 V-A	1-AB7*	1-RTN-A	1-RQ0*
46	1-RQ1*	1-GR*	3.3 V	1-PE*
47				
48		2.1 V		
49	GAP*	GA0*	GA1*	GA2*
50	GA3*	KEY	GA4*	KEY

Figure 10-12—Pinout for SEM-E Stretch Dual Futurebus+ connector section G

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	a	b	c	d
17	TMRS0*	TMRS1*	3.3 V	TMRS2*
18	AI*	AK*	AS*	ET*
19	DI*	5 V	DK*	DS*
20	CA0*	CA1*	CA2*	
21	GND	CM0*	CM1*	CM2*
22	CM3*	CM4*	CM5*	GND
23	CM6*	CM7*	ST0*	ST1*
24	ST2*	ST3*	3.3 V	ST4*
25	ST5*	ST6*	ST7*	
26	AD2*	5 V	AD1*	AD0*
27	AD5*	AD4*	AD3*	BC0*
28	GND	AD7*	AD6*	AD8*
29	AD11*	AD10*	AD9*	GND
30	AD14*	AD13*	AD12*	AD15*
31	AD17*	AD16*	3.3 V	BC1*
32	AD21*	AD20*	AD19*	AD18*
33	AD23*	5 V	AD22*	BC2*
34	AD27*	AD26*	AD25*	AD24*
35	GND	AD30*	AD29*	AD28*
36	RE*	BC3*	AD31*	GND
37	1-SB0*	TR0*	TR1*	1-SB1*
38	NED*	PFI*	3.3 V	UMP*
39	RUN*	PN	SR*	
40		5 V		AR*
41	AQ*	AP*	AC0*	AC1*
42	GND	ABC0*	AB0*	AB1*
43	AB2*	AB3*	AB4*	GND
44	AB5*	RTN-B	AB6*	28 V-B
45	28 V-A	AB7*	RTN-A	RQ0*
46	RQ1*	GR*	3.3 V	PE*
47				
48		2.1 V		
49	GAP*	GA0*	GA1*	GA2*
50	GA3*	KEY	GA4*	KEY

Figure 10-13—Pinout for SEM-E Stretch Error Correcting configuration connector section G

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	a	b	c	d
17	RF*	SLD*	3.3 V	TED*
18	AI*	AK*	AS*	ET*
19	DI*	5 V	DK*	DS*
20	CA0*	CA1*	CA2*	CP*
21	GND	CM0*	CM1*	CM2*
22	CM3*	CM4*	CM5*	GND
23	CM6*	CM7*	ST0*	ST1*
24	ST2*	ST3*	3.3 V	ST4*
25	ST5*	ST6*	ST7*	
26	AD2*	5 V	AD1*	AD0*
27	AD5*	AD4*	AD3*	BP0*
28	GND	AD7*	AD6*	AD8*
29	AD11*	AD10*	AD9*	GND
30	AD14*	AD13*	AD12*	AD15*
31	AD17*	AD16*	3.3 V	BP1*
32	AD21*	AD20*	AD19*	AD18*
33	AD23*	5 V	AD22*	BP2*
34	AD27*	AD26*	AD25*	AD24*
35	GND	AD30*	AD29*	AD28*
36	RE*	BP3*	AD31*	GND
37	SB0*	TR0*	TR1*	SB1*
38	NED*	PFI*	3.3 V	UMP*
39	RUN*	PN	SR*	
40	RED*	5 V		AR*
41	AQ*	AP*	AC0*	AC1*
42	GND	ABP*	AB0*	AB1*
43	AB2*	AB3*	AB4*	GND
44	AB5*	RTN-B	AB6*	28 V-B
45	28 V-A	AB7*	RTN-A	RQ0*
46	RQ1*	GR*	3.3 V	PE*
47				
48		2.1 V		
49	GAP*	GA0*	GA1*	GA2*
50	GA3*	KEY	GA4*	KEY

Figure 10-14—Pinout for SEM-E Stretch Single 32-bit and Single 64-bit Futurebus+ connector section G

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	a	b	c	d
17				
18				
19				
20				
21				
22				
23				
24				
25				Reserved
26				
27				
28				
29				
30				
31				
32				
33				
34				
35				
36				
37				
38				
39				Reserved
40			Reserved	
41				
42				
43				
44				
45				
46				
47	User I/O*	User I/O*	User I/O*	User I/O*
48	User I/O*		User I/O*	User I/O*
49				
50				

Figure 10-15—User-Definable I/O for SEM-E Stretch Dual Futurebus+ connector section G

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	a	b	c	d
17				
18				
19				
20				Reserved
21				
22				
23				
24				
25				Reserved
26				
27				
28				
29				
30				
31				
32				
33				
34				
35				
36				
37				
38				
39				Reserved
40	Reserved		Reserved	
41				
42				
43				
44				
45				
46				
47	User I/O*	User I/O*	User I/O*	User I/O*
48	User I/O*		User I/O*	User I/O*
49				
50				

Figure 10-16—User Definable I/O for SEM-E Stretch Error Correcting configuration connector section G

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	a	b	c	d
17				
18				
19				
20				
21				
22				
23				
24				
25				Reserved
26				
27				
28				
29				
30				
31				
32				
33				
34				
35				
36				
37				
38				
39				Reserved
40			Reserved	
41				
42				
43				
44				
45				
46				
47	User I/O*	User I/O*	User I/O*	User I/O*
48	User I/O*		User I/O*	User I/O*
49				
50				

Figure 10-17—User-Definable I/O for SEM-E Stretch single 32-bit and single 64-bit Futurebus+ connector section G

10.3.2.5 Connector section H

Connector section H shall contain data, control, utility, and arbitration lines for the Dual Bus, Error Correcting, and Single 64-bit Futurebus+ configurations. In the Dual Bus configuration, section H shall contain the entire Futurebus+ 2. In the Error Correcting configuration, section H shall contain the A and B copies of the control, utility, and arbitration lines and the spare lines. In the Single 64-bit configuration, section H shall contain the address and data lines corresponding to **AD[63..32]***. No signals shall be reserved in the Single 32-bit configuration.

For the Dual Futurebus+ and the Error Correcting configuration, several of the system control lines are duplicated to provide fault tolerance. Details of this feature are given in Table 10-1. The remaining area may

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be used for any local interconnects or user-defined I/O. As a minimum, connector section H shall contain the power pattern specified in Figure 10-20. If not used, these pins shall be reserved. The user may also define additional power and ground pins, if a unique keying is assigned to that configuration. Figures 10-18 through 10-21 show the pinouts for the SEM-E Stretch configurations in section H. Figures 10-22 through 10-25 show the user-definable I/O signal locations for each SEM-E Stretch configuration in section H. Note that all signals in section H (except **PN** and the sparing pins) are active low.

The 64-bit Futurebus+ is a modification of the Dual Futurebus+ where the second Futurebus+ pin definition is renamed to define address/data bits 32 through 63 and parity bits 4 through 7. The second set of control signals should be deleted. Note that a Dual Bus backplane may have Dual Bus modules and Single 32-bit modules both present concurrently. Single 64-bit modules may be plugged into a Dual Bus backplane if all other modules on the backplane are also Single 64-bit modules. Also note that an Error Correcting configuration backplane may have Error Correcting configuration modules and Single 32-bit modules both present concurrently, but the ECC and TMR on all Error Correcting configuration modules must be disabled. Single 64-bit backplanes may have Single 64-bit modules and Single 32-bit modules both present concurrently.

Table 10-1—Occurrence of space profile system control lines

Signal	32/64 Single Futurebus+	Dual Futurebus+	Error Correcting configuration
Utility Spares **UPSP*, UWSP**	0	0	2
Nuclear Event Detect **NED***	1	2	3
Power Failure Imminent **PFI***	1	2	3
Power Normal **PN**	1	2	3
Reset **RE***	1	2	3
Duplicate Reset **RED***	1	2	0
Reset Spare **RES***	0	0	1
Run **RUN***	1	1	1
Serial Bus 0 **SB0***	1	2	2
Serial Bus 1 **SB1***	1	2	2
Trigger 0 Start and Stop **TR0***	1	1	1
Trigger 1 Start and Stop **TR1***	1	1	1
User Console Interface Master Present **UMP***	1	1	1
System Reset **SR***	1	2	3

The SEM-E Stretch Dual Bus module shall provide pins for two copies of all central and distributed arbitration signals. The Error Correcting configuration module shall provide pins for three copies of the central

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arbitration request lines. Only one grant line shall be provided, however, due to coding on the grant line. The distributed arbitration lines are covered by ECC and TMR as described in the fault tolerance section of this document. The Single 32-bit and Single 64-bit configurations shall provide one set of all central and distributed arbitration signals. All implementations shall provide two +28 V input pins and two +28 V return pins for distributed power.

Table 10-2 shows how the various fault tolerant configurations are overlaid in connector section H. The empty column and row in Table 10-2 show why Single 32-bit modules can operate in backplanes designed for other configurations. This is because the Single 32-bit configuration does not use section H for any of its signals, therefore it does not interfere with them. This allows other modules to use section H as if the Single 32-bit module were not present.

Table 10-2—SEM-E Stretch overlays (Section H)

Futurebus+ Signals	Dual	Error Correcting	Single 32-bit	Single 64-bit
Control:Copy2,A	X	X		
Control:CopyB		X		
AD[31:0]*,FB+1				
AD[31:0]*,FB+2	X	Spares		AD[63:32]*

Table 10-3 shows the combinations possible SEM-E Stretch modules and backplanes containing the same optional features. The size of the backplane is the size of the largest possible configuration (64-bit for the Single Futurebus+, 32-bit (2) for the Dual Futurebus+, and 32-bit for the Error Correcting configuration). “No” is used in Table 10-3 to indicate where full configuration connection cannot be achieved physically. In all cases, a single 32-bit Futurebus+ could work as a degraded mode of any of the modules in any of the backplanes, but this is not recommended for final product; such use is envisioned only in laboratory or prototype environments when existing assets are being utilized in a less than optimum manner. Keying is used to prevent invalid combinations in the final product; however, a non-keyed backpanel used for rapid prototyping or other non-flight demonstrations is envisioned to allow the combinations shown in Table 10-3.

Table 10-3—SEM-E Stretch backplane/module combinations

		MODULE (32-bit/64-bit)		
		Single Futurebus+	**Dual Futurebus+**	**Error Correcting configuration**
BACKPLANE	**Single Futurebus+**	Yes/Yes	No/NA	No/NA
	Dual Futurebus+	Yes/Yes[a]	Yes/NA	No/NA
	Error Correcting configuration	Yes/No	No/NA	Yes/NA

[a] This configuration is possible if the only type of module present is a Single 64-bit Futurebus+.

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	e	f	g	h
17	2-RF*	2-SLD*	3.3 V	2-TED*
18	2-AI*	2-AK*	2-AS*	2-ET*
19	2-DI*	5 V	2-DK*	2-DS*
20	2-CA0*	2-CA1*	2-CA2*	2-CP*
21	GND	2-CM0*	2-CM1*	2-CM2
22	2-CM3*	2-CM4*	2-CM5*	GND
23	2-CM6*	2-CM7*	2-ST0*	2-ST1*
24	2-ST2*	2-ST3*	3.3 V	2-ST4*
25	2-ST5*	2-ST6*	2-ST7*	
26	2-AD2*	5 V	2-AD1*	2-AD0*
27	2-AD5*	2-AD4*	2-AD3*	2-BP0*
28	GND	2-AD7*	2-AD6*	2-AD8*
29	2-AD11*	2-AD10*	2-AD9*	GND
30	2-AD14*	2-AD13*	2-AD12*	2-AD15*
31	2-AD17*	2-AD16*	3.3 V	2-BP1*
32	2-AD21*	2-AD20*	2-AD19*	2-AD18*
33	2-AD23*	5 V	2-AD22*	2-BP2*
34	2-AD27*	2-AD26*	2-AD25*	2-AD24
35	GND	2-AD30*	2-AD29*	2-AD28*
36	2-RE*	2-BP3*	2-AD31*	GND
37	2-SB0*			2-SB1*
38	2-NED*	2-PFI*	3.3 V	
39		2-PN	2-SR*	
40	2-RED*	5 V		2-AR*
41	2-AQ*	2-AP*	2-AC0*	2-AC1*
42	GND	2-RTN-B	2-ABP*	2-28 V-B
43	2-28 V-A	2-AB0*	2-RTN-A	GND
44	2-AB1*	2-AB2*	2-AB3*	2-AB4*
45	2-AB5*	2-AB6*	2-AB7*	2-RQ0*
46	2-RQ1*	2-GR*	3.3 V	2-PE*
47				
48		2.1 V		
49				
50	GND			

Figure 10-18—Pinout for SEM-E Stretch Dual Futurebus+ connector section H

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	e	f	g	h
17			3.3 V	
18	AIA*	AKA*	ASA*	ETA*
19	DIA*	5 V	DKA*	DSA*
20	CAA0*	CAA1*	CAA2*	CC0*
21	GND	CC1*	CC2*	CC3*
22	CC4*	CMS0*	CMS1*	GND
23			STA0*	STA1*
24	STA2*	STA3*	3.3 V	STA4*
25	STA5*	STA6*	STA7*	
26	ADS2*	5 V	ADS1*	ADS0*
27	ADS4*	BCS0*	ADS3*	
28	GND	ADS6*	ADS5*	ADS7*
29	AIB*	AKB*	ASB*	GND
30	ETB*	DIB*	DKB*	DSB*
31	CAB0*	CAB1*	3.3 V	
32	CAB2*	STB0*	STB1*	STB2*
33	STB3*	5 V	STB4*	
34	STB5*	STB6*	STB7*	TMRS3*
35	GND	TMRS4*		
36	REA*	UWSP	BCS1*	GND
37	2-SB0*	UPSP*	PFIB*	2-SB1*
38	NEDA*	PFIA*	3.3 V	PNB
39	SRB*	PNA	SRA*	NEDB*
40	REB*	5 V	RES*	ARA*
41	AQA*	APA*	ACA0*	ACA1*
42	GND	RTN-B	ABC1*	28 V-B
43	28 V-A	ABC2*	RTN-A	GND
44	ABC3*	ABC4*	ABS0*	ABS1*
45	GCP*	GC0*	GC1*	RQA0*
46	RQA1*	GC2*	3.3 V	PEA*
47	GC3*	GC4*	GC5*	GCS*
48	GRS*	2.1 V	ARBS*	PEB*
49	RQB1*	RQB0*	ACB1*	ACB0*
50	GND	APB*	AQB*	ARB*

Figure 10-19—Pinout for SEM-E Stretch Error Correcting configuration connector section H

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	e	f	g	h
17			3.3 V	
18				
19		5 V		
20				
21	GND			
22				GND
23				
24			3.3 V	
25				
26		5 V		
27				
28	GND			
29				GND
30				
31			3.3 V	
32				
33		5 V		
34				
35	GND			
36				GND
37				
38			3.3 V	
39				
40		5 V		
41				
42	GND	RTN-B		28 V-B
43	28 V-A		RTN-A	GND
44				
45				
46			3.3 V	
47				
48		2.1 V		
49				
50	GND			

Figure 10-20—Pinout for SEM-E Stretch Single 32-bit Futurebus+ connector section H

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	e	f	g	h
17			3.3 V	
18				
19		5 V		
20				
21	GND			
22				GND
23				
24			3.3 V	
25				
26	AD34*	5 V	AD33*	AD32*
27	AD37*	AD36*	AD35*	BP4*
28	GND	AD39*	AD38*	AD40*
29	AD43*	AD42*	AD41*	GND
30	AD46*	AD45*	AD44*	AD47*
31	AD49*	AD48*	3.3 V	BP5*
32	AD53*	AD52*	AD51*	AD50*
33	AD55*	5 V	AD54*	BP6*
34	AD59*	AD58*	AD57*	AD56*
35	GND	AD62*	AD61*	AD60*
36		BP7*	AD63*	GND
37				
38			3.3 V	
39				
40		5 V		
41				
42	GND	RTN-B		28 V-B
43	28 V-A		RTN-A	GND
44				
45				
46			3.3 V	
47				
48		2.1 V		
49				
50	GND			

Figure 10-21—Pinout for SEM-E Stretch Single 64-bit Futurebus+ connector section H

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	e	f	g	h
17				
18				
19				
20				
21				
22				
23				
24				
25				User I/O*
26				
27				
28				
29				
30				
31				
32				
33				
34				
35				
36				
37		User I/O*	User I/O*	
38				User I/O*
39	User I/O*			User I/O*
40			User I/O*	
41				
42				
43				
44				
45				
46				
47	User I/O*	User I/O*	User I/O*	User I/O*
48	User I/O*		User I/O*	User I/O*
49	User I/O*	User I/O*	User I/O*	User I/O*
50		User I/O*	User I/O*	User I/O*

Figure 10-22—User-Definable I/O for SEM-E Stretch Dual Futurebus+ connector section H

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	e	f	g	h
17	User I/O*	User I/O*		User I/O*
18				
19				
20				
21				
22				
23	User I/O*	User I/O*		
24				
25				User I/O*
26				
27				User I/O*
28				
29				
30				
31				User I/O*
32				
33				User I/O*
34				
35			User I/O*	User I/O*
36				
37				
38				
39				
40				
41				
42				
43				
44				
45				
46				
47				
48				
49				
50				

Figure 10-23—User-Definable I/O for SEM-E Stretch Error Correcting configuration connector section H

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	e	f	g	h
17	User I/O*	User I/O*		User I/O*
18	User I/O*	User I/O*	User I/O*	User I/O*
19	User I/O*		User I/O*	User I/O*
20	User I/O*	User I/O*	User I/O*	User I/O*
21		User I/O*	User I/O*	User I/O*
22	User I/O*	User I/O*	User I/O*	
23	User I/O*	User I/O*	User I/O*	User I/O*
24	User I/O*	User I/O*		User I/O*
25	User I/O*	User I/O*	User I/O*	User I/O*
26	User I/O*		User I/O*	User I/O*
27	User I/O*	User I/O*	User I/O*	User I/O*
28		User I/O*	User I/O*	User I/O*
29	User I/O*	User I/O*	User I/O*	
30	User I/O*	User I/O*	User I/O*	User I/O*
31	User I/O*	User I/O*		User I/O*
32	User I/O*	User I/O*	User I/O*	User I/O*
33	User I/O*		User I/O*	User I/O*
34	User I/O*	User I/O*	User I/O*	User I/O*
35		User I/O*	User I/O*	User I/O*
36	User I/O*	User I/O*	User I/O*	
37	User I/O*	User I/O*	User I/O*	User I/O*
38	User I/O*	User I/O*		User I/O*
39	User I/O*	User I/O*	User I/O*	User I/O*
40	User I/O*		User I/O*	User I/O*
41	User I/O*	User I/O*	User I/O*	User I/O*
42			User I/O*	
43		User I/O*		
44	User I/O*	User I/O*	User I/O*	User I/O*
45	User I/O*	User I/O*	User I/O*	User I/O*
46	User I/O*	User I/O*		User I/O*
47	User I/O*	User I/O*	User I/O*	User I/O*
48	User I/O*		User I/O*	User I/O*
49	User I/O*	User I/O*	User I/O*	User I/O*
50		User I/O*	User I/O*	User I/O*

Figure 10-24—User-Definable I/O for SEM-E Stretch Single 32-bit Futurebus+ connector section H

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	e	f	g	h
17	User I/O*	User I/O*		User I/O*
18	User I/O*	User I/O*	User I/O*	User I/O*
19	User I/O*		User I/O*	User I/O*
20	User I/O*	User I/O*	User I/O*	User I/O*
21		User I/O*	User I/O*	User I/O*
22	User I/O*	User I/O*	User I/O*	
23	User I/O*	User I/O*	User I/O*	User I/O*
24	User I/O*	User I/O*		User I/O*
25	User I/O*	User I/O*	User I/O*	User I/O*
26				
27				
28				
29				
30				
31				
32				
33				
34				
35				
36	User I/O*			
37	User I/O*	User I/O*	User I/O*	User I/O*
38	User I/O*	User I/O*		User I/O*
39	User I/O*	User I/O*	User I/O*	User I/O*
40	User I/O*		User I/O*	User I/O*
41	User I/O*	User I/O*	User I/O*	User I/O*
42			User I/O*	
43		User I/O*		
44	User I/O*	User I/O*	User I/O*	User I/O*
45	User I/O*	User I/O*	User I/O*	User I/O*
46	User I/O*	User I/O*		User I/O*
47	User I/O*	User I/O*	User I/O*	User I/O*
48	User I/O*		User I/O*	User I/O*
49	User I/O*	User I/O*	User I/O*	User I/O*
50		User I/O*	User I/O*	User I/O*

Figure 10-25—User-Definable I/O for SEM-E Stretch Single 64-bit Futurebus+ connector section H

10.3.3 Central arbiter definition

For central arbiter modules, most of the locations previously reserved for user defined I/O are redefined to support central arbitration. These locations are distributed across connector sections E, F, G, and H. Arbitration lines are assigned starting with section F, then E, then G, and finally H.

Each SEM-E Stretch configuration supports a different number of modules, depending upon the number of arbitration lines required and the number of unused connector pins. Each bus of a Dual Futurebus+ module requires three unique lines: **1-RQ0***, **1-RQ1***, and **1-GR*** or **2-RQ0***, **2-RQ1***, and **2-GR***. When all unused connector pins are assigned to central arbitration this module will support 15 external modules. Each Error Correcting configuration module requires seven unique lines: **RQ0***, **RQA0***, **RQB0***, **RQ1***,

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RQA1*, **RQB1***, and **GR***. When all unused connector pins are assigned to central arbitration this module will support 12 external modules. Both the Single 32-bit Futurebus+ and the Single 64-bit Futurebus+ require only three unique lines for each module: **RQ0***, **RQ1***, and **GR***. These modules easily support the full 31 modules specified by IEEE Std 896.2-1991. The Space Profile Committee only simulated systems with up to 15 slots. Thus systems over 15 slots should be simulated before using.

Note that the Dual Bus central arbiter slot can accept either Dual Bus or Single 32-bit Futurebus+ Profile S central arbiter modules. Like the Dual bus configuration, the Error Correcting configuration can also use Single 32-bit Profile S central arbiter modules, but the error correcting functionality on the Error Correcting configuration modules must be disabled. Single Futurebus+ central arbiter slots can only be occupied by Single Futurebus+ central arbiters, but 32-bit and 64-bit central arbiters will properly operate in a 64-bit backplane, and 32-bit central arbiters will properly operate in a 32-bit backplane.

Figures 10-26 through 10-28 show the central arbitration assignments for all SEM-E Stretch configurations. Note that all central arbiter signals are active low.

The Central Arbiter function for each of the two busses of a Dual Futurebus+ configuration may either be combined into a single slot or spread across two slots. If combined, then Figure 10-26 shall be used to assign the pins. If separate, then Figure 10-28 shall be used to assign the pins for each bus. This allows the same Central Arbiter Module Type to be used for each module. Additionally, more than one slot per bus may be occupied by a central arbiter module. In this case, only one module shall be actively driving Central Arbiter grants (**GR-x***) and preempt (**PE*** during reset) at a time. Others on the same bus must be disabled and tristated or powered off. When redundancy is used, stub lengths and spacings for the **RQ0-x***, **RQ1-x***, and **GR-x*** for each bus shall be maintained. In a single central arbiter per bus system, these signals have no stub length requirements since they are wired point to point.

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	a	b	c	d	e	f	g	h
1								
2								
3								
4								
5								
6	1-RQ1-11*				2-RQ1-7*	2-GR-7*	1-RQ0-8*	1-RQ1-8*
7						1-RQ1-7*	1-GR-7*	2-RQ0-7*
8					2-RQ1-6*	2-GR-6*	1-RQ0-7*	
9					1-RQ0-6*	1-RQ1-6*	1-GR-6*	2-RQ0-6*
10					2-RQ0-5*	2-RQ1-5*		2-GR-5*
11					2-GR-4*	1-RQ0-5*	1-RQ1-5*	1-GR-5*
12	2-RQ1-10*		2-GR-10*	1-RQ0-11*	1-GR-4*		2-RQ0-4*	2-RQ1-4*
13	1-RQ0-10*	1-RQ1-10*	1-GR-10*	2-RQ0-10*	2-RQ1-3*	2-GR-3*	1-RQ0-4*	1-RQ1-4*
14		2-RQ0-9*	2-RQ1-9*	2-GR-9*		1-RQ1-3*	1-GR-3*	2-RQ0-3*
15	1-RQ0-9*	1-RQ1-9*	1-GR-9*		2-RQ1-2*	2-GR-2*	1-RQ0-3*	
16	1-GR-8*	2-RQ0-8*	2-RQ1-8*	2-GR-8*	1-RQ0-2*	1-RQ1-2*	1-GR-2*	2-RQ0-2*
17								
18								
19								
20								
21								
22								
23								
24								
25				2-GR-12*				
26								
27								
28								
29								
30								
31								
32								
33								
34								
35								
36								
37								
38								2-GR-15*
39				2-RQ1-12*	2-RQ0-15*			2-RQ1-15*
40			2-RQ0-12*				1-GR-15*	
41								
42								
43								
44								
45								
46								
47	2-GR-11*	1-RQ0-12*	1-RQ1-12*	1-GR-12*	2-RQ1-14*	2-GR-14*	1-RQ0-15*	1-RQ1-15*
48	1-GR-11*		2-RQ0-11*	2-RQ1-11*	1-RQ1-14*		1-GR-14*	2-RQ0-14*
49					2-RQ0-13*	2-RQ1-13*	2-GR-13*	1-RQ0-14*
50						1-RQ0-13*	1-RQ1-13*	1-GR-13*

Figure 10-26—Maximum central arbiter definition for SEM-E Stretch Dual Futurebus+

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	a	b	c	d	e	f	g	h
1								
2								
3								
4								
5								
6	RQB0-7*				RQA1-2*	RQB0-2*	RQB1-2*	RQA0-3*
7						RQ1-12*	GR-12*	RQA0-2*
8					RQ1-11*	GR-11*	RQ0-12*	
9					RQ0-10*	RQ1-10*	GR-10*	RQ0-11*
10					RQ0-9*	RQ1-9*		GR-9*
11					GR-7*	RQ0-8*	RQ1-8*	GR-8*
12	RQB1-6*		RQA0-7*	RQA1-7*	GR-6*		RQ0-7	RQ1-7*
13	RQB1-5*	RQA0-6*	RQA1-6*	RQB0-6*	RQ1-5*	GR-5*	RQ0-6*	RQ1-6*
14		RQA0-5*	RQA1-5*	RQB0-5*		RQ1-4*	GR-4*	RQ0-5*
15	RQA1-4*	RQB0-4*	RQB1-4*		RQ1-3*	GR-3*	RQ0-4*	
16	RQA1-3*	RQB0-3*	RQB1-3*	RQA0-4*	RQ0-2*	RQ1-2*	GR-2*	RQ0-3*
17						RQB1-10*		
18								
19								
20				RQB0-10*				
21								
22								
23								
24					RQB0-12*	RQB1-12*		
25				RQA1-10*				RQA1-12*
26								
27								RQA0-12*
28								
29								
30								
31								RQB1-11*
32								
33								RQB0-11*
34								
35							RQA0-11*	RQA1-11*
36								
37								
38								
39				RQA0-10*				
40	RQB0-9*		RQB1-9*					
41								
42								
43								
44								
45								
46								
47	RQB0-8*	RQB1-8*	RQA0-9*	RQA1-9*				
48	RQB1-7*		RQA0-8*	RQA1-8*				
49								
50								

Figure 10-27—Maximum central arbiter definition for SEM-E Stretch Dual Futurebus+

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	a	b	c	d	e	f	g	h
1								
2								
3								
4								
5								
6	RQ1-20*				RQ1-13*	GR-13*	RQ0-14*	RQ1-14*
7						RQ1-12*	GR-12*	RQ0-13*
8					RQ1-11*	GR-11*	RQ0-12*	
9					RQ0-10*	RQ1-10*	GR-10*	RQ0-11*
10					RQ0-9*	RQ1-9*		GR-9*
11					GR-7*	RQ0-8*	RQ1-8*	GR-8*
12	RQ1-19*		GR-19*	RQ0-20*	GR-6*		RQ0-7*	RQ1-7*
13	RQ0-18*	RQ1-18*	GR-18*	RQ0-19*	RQ1-5*	GR-5*	RQ0-6*	RQ1-6*
14		RQ0-17*	RQ1-17*	GR-17*		RQ1-4*	GR-4*	RQ0-5*
15	RQ0-16*	RQ1-16*	GR-16*		RQ1-3*	GR-3*	RQ0-4*	
16	GR-14*	RQ0-15*	RQ1-15*	GR-15*	RQ0-2*	RQ1-2*	GR-2*	RQ0-3*
17								
18								
19								
20								
21								
22								
23								
24								
25				GR-23*				
26								
27								
28								
29								
30								
31								
32								
33								
34								
35								
36								
37								
38								GR-29*
39				RQ1-23*	RQ0-29			RQ1-29*
40			RQ0-23**				GR-28*	
41								
42								
43								
44								
45					RQ0-31*	RQ1-31*	GR-31*	
46					RQ0-30*	RQ1-30*		GR-30*
47	GR-21*	RQ0-22*	RQ1-22*	GR-22*	RQ1-27*	GR-27*	RQ0-28*	RQ1-28*
48	GR-20*		RQ-21*	RQ1-21*	RQ1-26*		GR-26*	RQ0-27*
49					RQ0-25*	RQ1-25*	GR-25*	RQ0-26*
50						RQ0-24*	RQ1-24*	GR-24*

Figure 10-28—Maximum central arbiter definition for SEM-E Stretch Single 32-bit and Single 64-bit Futurebus+

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10.3.4 Power pin assignments

All connector sections shall be utilized for supplying digital power to Profile S SEM-E Stretch modules. Connector sections E, F, G, and H shall be utilized for supplying digital ground to Profile S SEM-E Stretch modules in all configurations. Connector sections C and D shall also be used to supply ground in non-fiber applications. The power pin assignments for the connector sections shall be as shown in Figure 10-29. If unused on the module, these pins shall remain reserved.

Table 10-4 lists the required (+28 V, +5 V, +2.1 V, and +3.3 V) power pins per voltage level and ground pins for the SEM-E Stretch module. Wiring of +28 V, +5 V, +2.1 V and +3.3 V in the backplane is required. Support of these voltages on the modules, beyond maintaining the required pin assignments, is optional. Additional power pins may be implemented on connector sections E, F, G, and H if appropriate keying definitions are created.

The +28 V supplies have been labeled A and B in case independent supplies are provided. A module may use power from either +28 V supply or both. A module shall treat the two supplies as separate power sources and provide separate return paths to the appropriate return signals.

Two +5 V and two +3.3 V pins have been designated as unswitched power inputs, **5 V US** and **3.3 V US**. If there is any power switching in the system, then these signals shall be used to pass unswitched power to the module separate from the switched power passed on the other **+5 V** and **+3.3 V** power inputs in order to power specific elements continuously (such as clocks or non-volatile memory). Both switched and unswitched power returns shall use 0 V (**GND**). If a module is always powered it shall only use the switched power pins.

The pin assignments for power and ground for all SEM-E Stretch implementations are given in Figure 10-29.

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	a	b	c	d	e	f	g	h
1				GND				GND
2								
3			3.3 V				3.3 V	
4								
5		5 V				5 V		
6								
7	GND				GND			
8				GND				GND
9								
10			2.1 V				3.3 V US	
11								
12		5 V				5 V US		
13								
14	GND				GND			
15				GND				GND
16								
17			3.3 V				3.3 V	
18								
19		5 V				5 V		
20								
21	GND				GND			
22				GND				GND
23								
24			3.3 V				3.3 V	
25								
26		5 V				5 V		
27								
28	GND				GND			
29				GND				GND
30								
31			3.3 V				3.3 V	
32								
33		5 V				5 V		
34								
35	GND				GND			
36				GND				GND
37								
38			3.3 V				3.3 V	
39								
40		5 V				5 V		
41								
42	GND				GND	RTN-B		28 V-B
43				GND	28 V-A		RTN-A	GND
44		RTN-B		28 V-B				
45	28 V-A		RTN-A					
46			3.3 V				3.3 V US	
47								
48		2.1 V				5 V US		
49								
50					GND			

Figure 10-29—Power pin assignments for module SEM-E Stretch

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Table 10-4—Required power pins per voltage level for module SEM-E Stretch

Voltage	Number of pins
+5 V	13
+5 V US	2
+3.3 V	13
+3.3 V US	2
2.1 V	2
+28 V	4
28 V-RTN	4
GND (5 V, 3.3 V and 2.1 V RTN)	27

10.3.5 Connector keying

Keying is a required feature used to avoid interoperability conflicts between Profile S modules, or between modules that belong to different profiles but have compatible mechanical characteristics. Keying puts constraints on which modules can be inserted into which slots. Keying is necessary where a backplane has been built with slot-unique characteristics. Keying is also necessary when non-IEEE Std 896.10-1997 electrical compliant drivers may assert signals on user defined lines. Each SEM-E Stretch module shall contain two keying pins: alpha and beta (referenced and defined in EIA IS E700A). Each of these keys shall have eight different positions. The alpha key shall be located at the end of the connector labelled with the lowest row number. The beta key shall be located at the end of the connector labelled with the highest row number. All SEM-E Stretch modules shall use keying. It is required that matching keying is used on all Profile S SEM-E Stretch backplanes although the absence of such keying is allowed in a lab environment at a degraded level (single bus) for demonstrations and concept proving activities.

The alpha key shall be used to represent the bus size and configuration. The keys used shall be

Position A: 32-Bit Single Futurebus+
Position B: 32-Bit Dual Futurebus+
Position C: 32-Bit Error Correcting configuration
Position D: 64-Bit Single Futurebus+
Position E–H: Reserved

The beta key shall be used to represent the various options present: The keys used shall be

Position A: No options present
Position B: MIL-STD-1553B present
Position C: Central Arbiter present
Position D: MIL-STD-1553B and Central Arbiter present
Position E–H: Reserved

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11. Detailed specification, Physical layer—10 SU

11.1 Mechanical

The physical characteristics for the 10 SU module shall be in accordance with the conduction cooled version of the 10 SU module detailed in IEEE Std 1101.3-1993. Critical interface requirements between the module and subrack shall also be as outlined in IEEE Std 1101.3-1993 and shall be followed in order to maintain interchangeability among modules.

Environmental performance levels shall be in accordance with IEEE Std 1156.4-1997 instead of IEEE Std 1156.1-1993 (as required in IEEE Std 1101.3-1993). IEEE Std 1101.3-1993 allows for a module profile of 1.93 cm (0.760 in) on a 1.99 cm (0.787 in) minimum pitch. Since the free span of the 10 SU module is relatively large compared to the SEM-E Stretch module, careful attention must be given to ensure that module deflections during shock and vibration do not allow for possible damage due to excessive deflections. This is especially true for shock and vibe levels II and III of the IEEE Std 1156.4-1997 environmental specification.

11.1.1 Unoccupied slots

The system integrator is responsible for ensuring that a configuration having unoccupied slots meets the internal environmental standards specified in IEEE Std 1156.4-1997. Additionally, it is the integrator's responsibility to ensure that all applicable EMI standards are met for the applications in which the systems are intended to operate.

11.1.2 Backplane capacity

The backplane and subrack assembly shall support at least as many slots as are required for a given application but no more that 31 slots.

The space working group has used 14 slots as a "typical" system size and has used this number for electrical studies. Because mechanical analysis is completely system-dependent, no mechanical or thermal analyses performed by the working group should be substituted for this analysis. This analysis should be supported by product literature.

11.1.3 Injector/Elector mechanism

If insertion/extraction levers are used, they must be retained so that they do not vibrate or rattle during shock and random vibration.

11.2 Input/Output

If there are non-Futurebus+ signals passing into or out of a 10 SU module, those signals should connect through the backplane user I/O area. Connection to dual or redundant or secondary buses on the backplane is permitted for 10 SU modules.

11.3 Profile connector, power, and signal pin assignments

11.3.1 Connector naming conventions and connector assignment

Figure 11-1 shows the connector naming convention for 10 SU modules. The entire connector consists of 70 rows (1–70) and 8 columns (a–h) of pins and is built from fourteen segments, each 5 rows by 8 columns. For pinout reference, the connector is partitioned into six sections: C, D, E, F, G, and H. Sections C and D consist of 5 rows by 4 columns (20 pin locations) each. Sections E and F consist of 18 rows by 4 columns (72

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pin locations) each. Sections G and H consist of 47 rows by 4 columns (188 pin locations) each. These connector sections are defined for both the 10 SU Dual Futurebus+ and the 10 SU Error Correcting configuration. The 10 SU Single 32-bit, 64-bit, and 128-bit Futurebus+ profiles are modifications of these two base definitions. For all implementations, sections C and D may optionally contain fiber connections. Connector section E contains two optional dual-redundant MIL-STD-1553 serial buses and user-defined I/O. Connector section F contains user-defined I/O only. Connector section G contains the data, control, utility, and arbitration lines needed to implement a Single 64-bit Futurebus+ (and Single 32-bit Futurebus+). This section is also used for Futurebus+ 1 in the Dual Bus Futurebus+ configuration. In the Error Correcting configuration, connector section G contains the data lines and the base copy of the control, utility, and arbitration lines. Connector section G contains 28 V power connections in all configurations. Connector section H contains the data, control, utility, and arbitration lines needed for the Futurebus+ 2 bus in the Dual Bus configuration. In the single bus configurations, connector section H contains the required data lines (for the 128-bit bus) and user-defined I/O lines. In the Error Correcting configuration, connector section H contains the A and B copies of the control, utility, and arbitration lines, and the spare lines. In all configurations, connector section H contains 28 V power connections. Power (+5 V and +3.3 V) and ground is distributed across all connector sections.

Pins are referenced by row number and column letter as shown. Pin locations 1a and 1c do not exist and are replaced by the first or alpha key. Pin locations 70b and 70d do not exist and are replaced by the second or beta key. The third or gamma key is located in the support area in the center of the 10 SU connector and does not use up pin locations. The total number of pins in the connector is 556. Sides “A” and “B” of the connector are referenced as shown in Figure 11-1. Pins in each row (a–h) are alternately staggered vertically as shown in Figure 11-1.

All connector views in this section show the backplane connector pinout as seen from the front of the rack. Note that other documents may refer to a through h as rows and 1 through 70 as columns. The convention described above was chosen in order to simplify the connector figures in this document and is consistent with the Futurebus+ Military Profile, ISO/IEC 14536: 1995.

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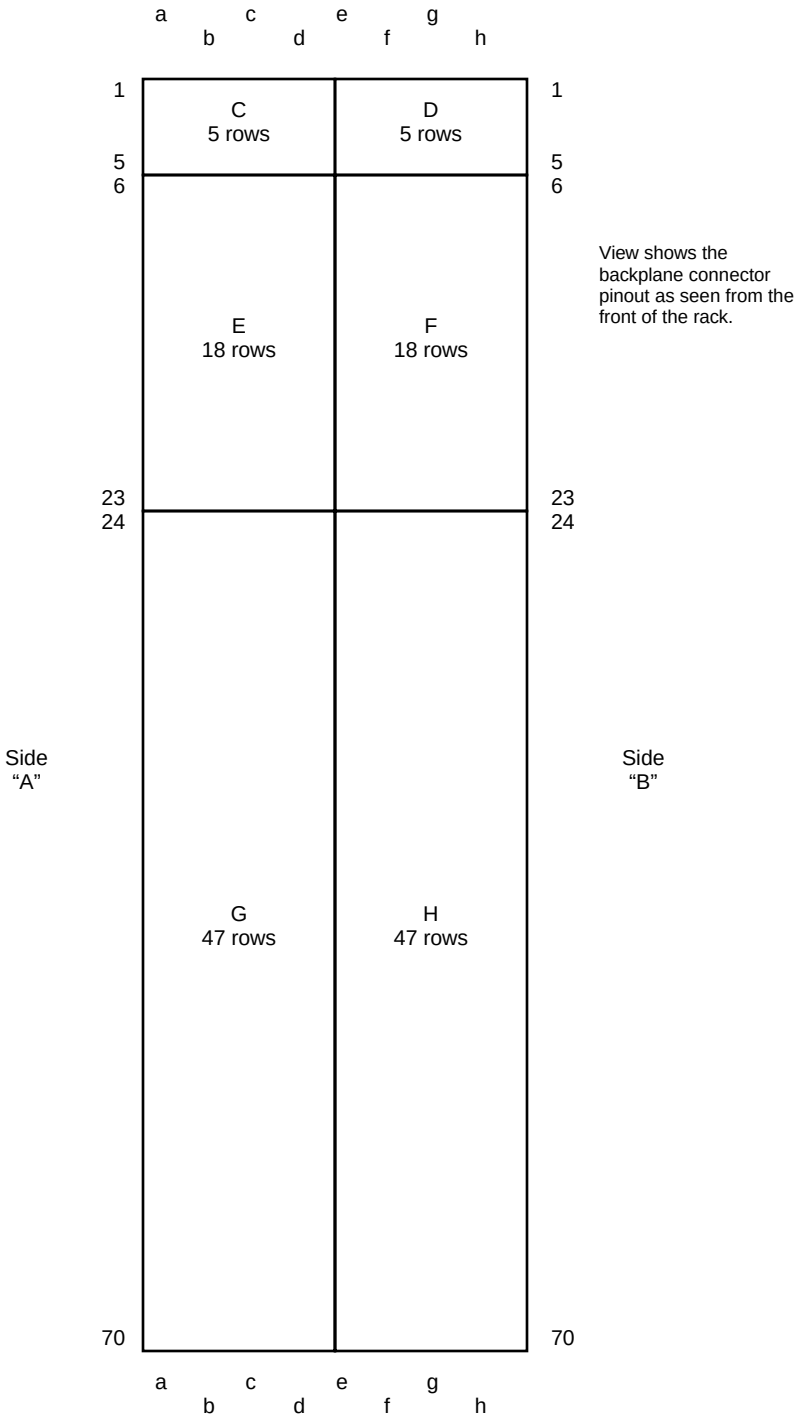

Figure 11-1—Module 10 SU connector naming conventions

11.3.2 Signal pin assignments

Initial attempts were made to develop a space profile pin definition that matched the military profile. This proved impossible for the following reasons. First, the military profile requires many more power and ground connections due to the high power dissipation of the module. Second, the military profile does not support the Error Correcting configuration or have adequate spare lines.

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Work was done with the pinouts to allow easy card layout for all possible transceiver implementations (using 8-bit and 9-bit transceivers and separate protocol chips). The pinouts allow for a discrete interface where individual transceivers and separate protocol chips are used, a completely integrated interface where transceivers and protocol chips are combined in the same package, and a range of partially integrated implementations between these two extremes. Due to the limited space on 10 SU cards, a partially or completely integrated interface is recommended.

Whenever possible, signals overlap between the 10 SU Dual Futurebus+, the 10 SU Error Correcting configuration, the 10 SU 32-bit Single Futurebus+, the 10 SU 64-bit Single Futurebus+, and the 10 SU 128-bit Single Futurebus+. Figures 11-2 through 11-6 show how the signals are distributed on the connector for the 10 SU module configurations.

User-Defined I/O signals are shown in Figures 11-2 through 11-6. These allow maximum flexibility for non-bused signals and are defined in connector sections E–H. When the optional central arbiter or MIL-STD-1553 bus is implemented, some, most or all of the user-defined I/O pinouts are utilized to provide the additional signal paths required. See 11.3.3 for the definition of the Central Arbitration usage of user-defined I/O for that module.

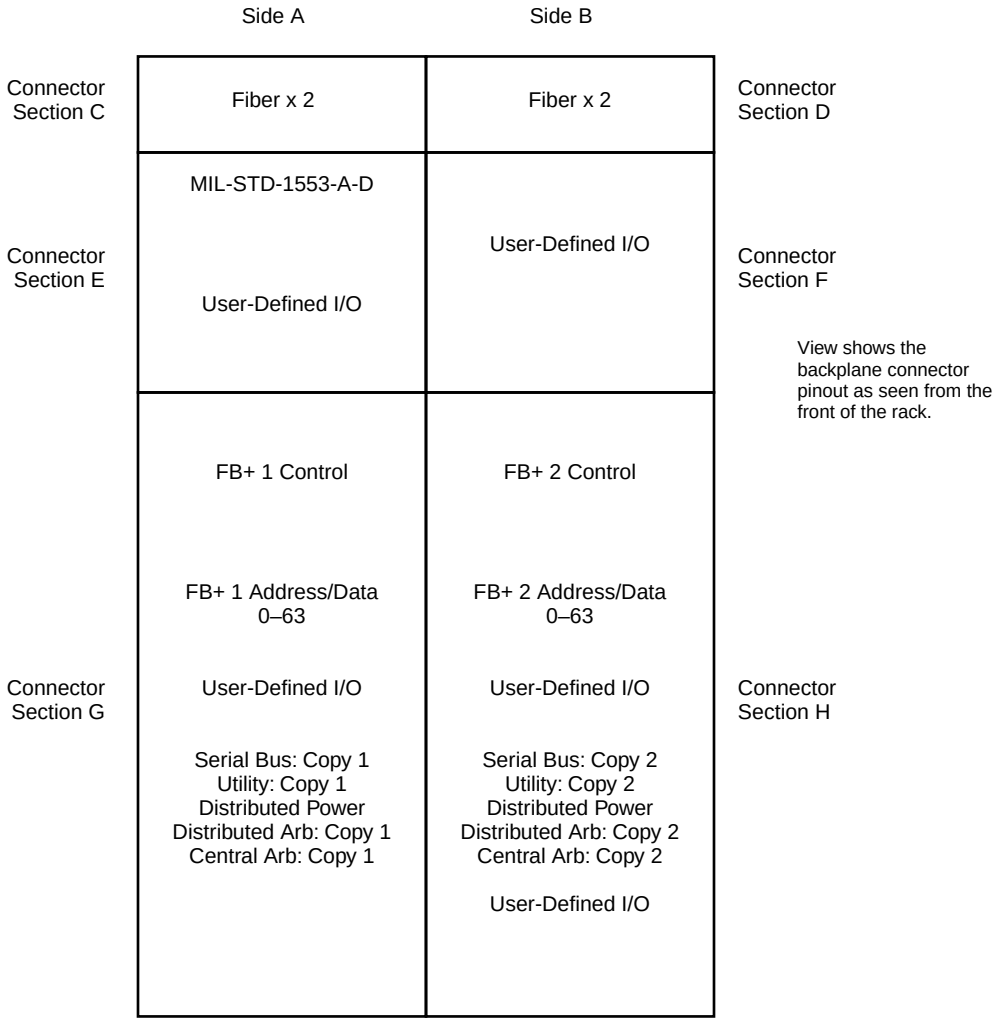

Figure 11-2—Module 10 SU connector usage (Dual Futurebus+)

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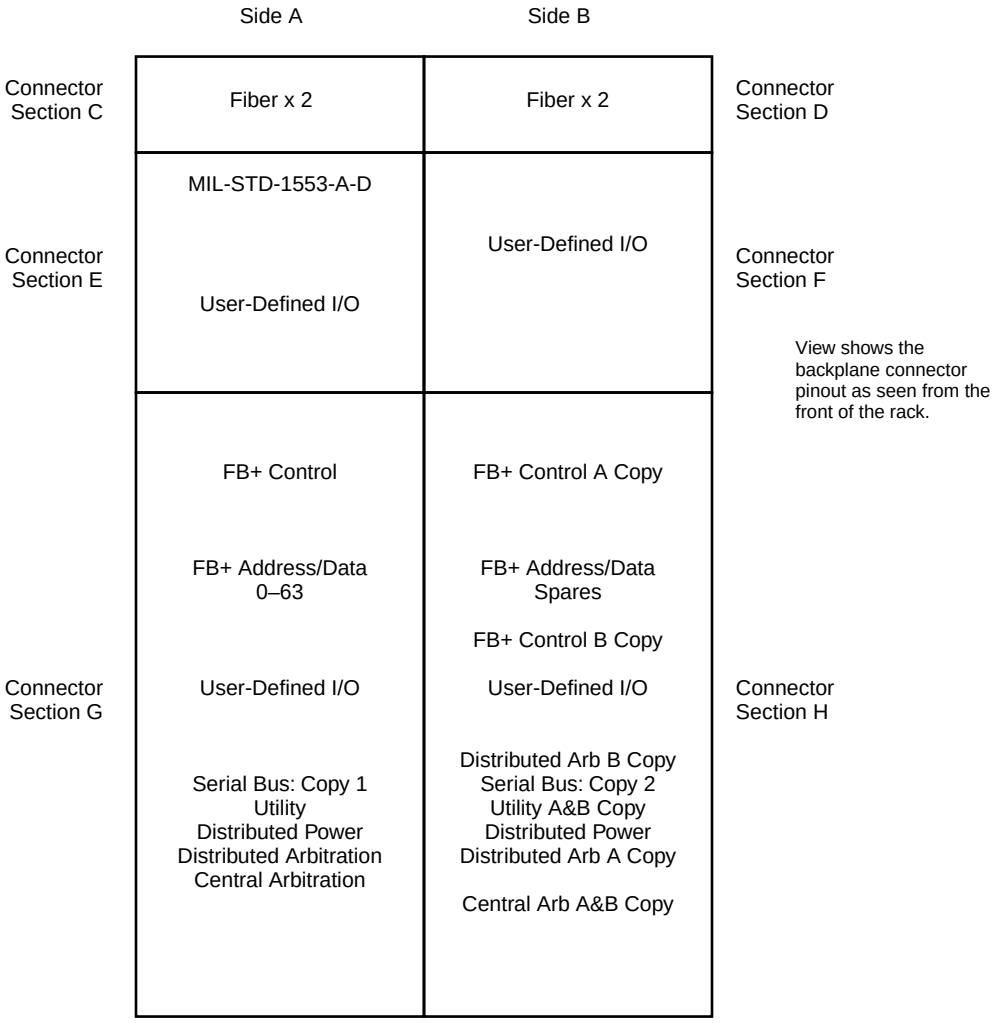

Figure 11-3—Module 10 SU connector usage (Error Correcting configuration)

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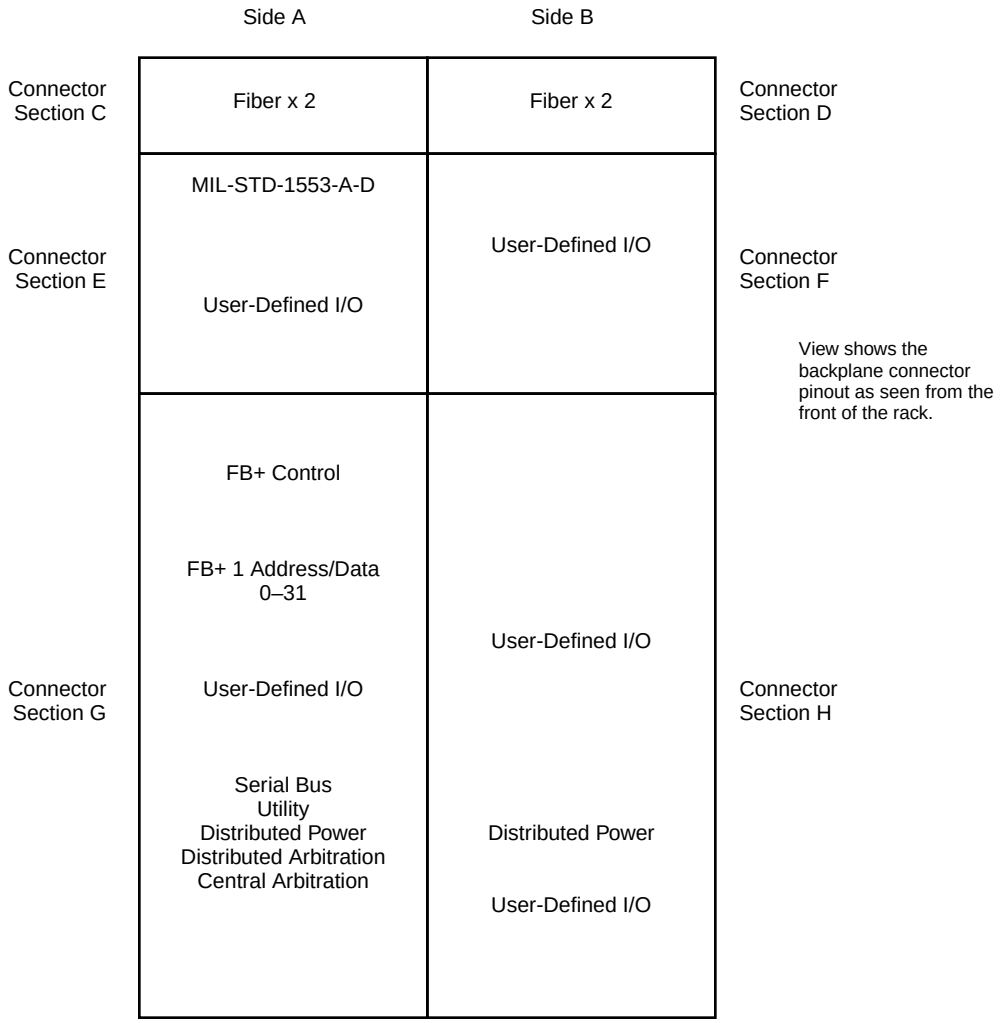

Figure 11-4—Module 10 SU connector usage (32-bit Single Futurebus+)

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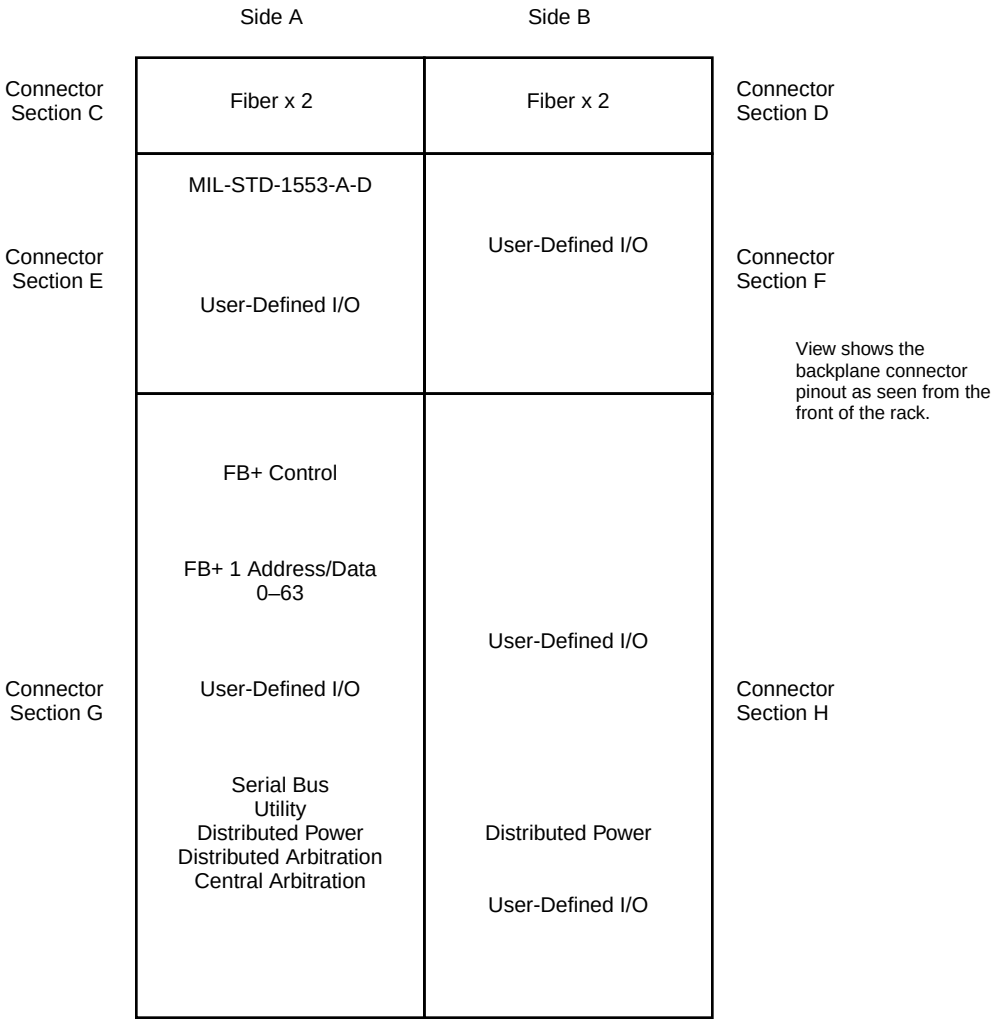

Figure 11-5—Module 10 SU connector usage (64-bit Single Futurebus+)

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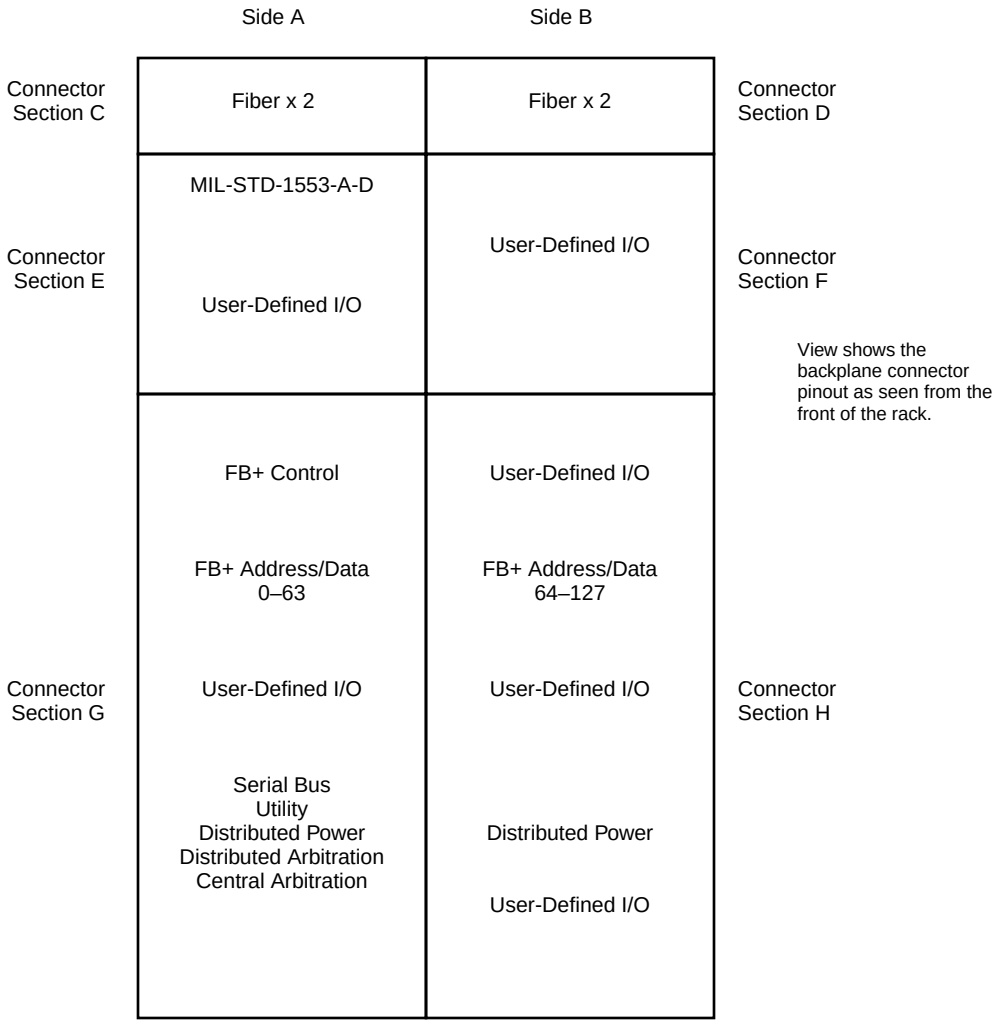

Figure 11-6—Module 10 SU connector usage (128-bit Single Futurebus+)

11.3.2.1 Connector sections C and D

If fiber is implemented, connector sections C and D shall be used for the four fiber connections. These pins replace one segment of the connector. The connector only supports a fiber segment at one end of the connector. This resulted in the choice of sections C and D. This implies two fiber connections for each side of the card. If the fiber connections are not implemented, the original connector section may be used for user-defined I/O.

Figures 11-7 and 11-8 show the pinouts for sections C and D for all connector definitions. If used for fiber, section C shall contain a keying pin occupying two pin locations and two fiber connections. Section D shall also contain two fiber connections. If the fiber connections are not implemented, section C shall contain 15 user-defined connections, two keying pin locations, one +5 V connection, one +3.3 V connection, and one ground connection. Similarly, section D shall contain 17 user-defined connections, one +5 V connection, one +3.3 V connection, and one ground connection.

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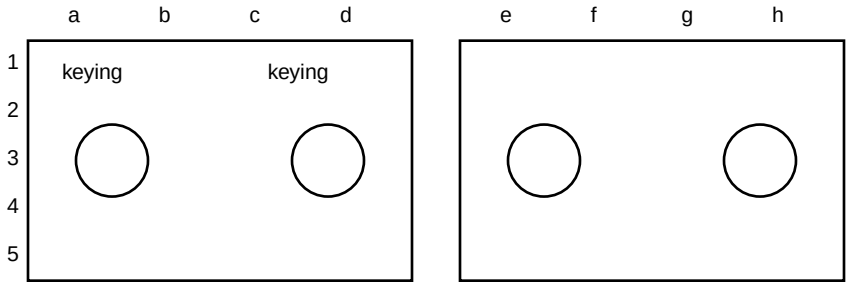

Figure 11-7—10 SU connector sections C and D with fiber connections

	a	b	c	d	e	f	g	h
1	KEY	User I/O*	KEY	GND	User I/O*	User I/O*	User I/O*	GND
2	User I/O*	User I/O*	User I/O*	User I/O*	User I/O*	User I/O*	User I/O*	User I/O*
3	User I/O*	User I/O*	3.3 V	User I/O*	User I/O*	User I/O*	3.3 V	User I/O*
4	User I/O*	User I/O*	User I/O*	User I/O*	User I/O*	User I/O*	User I/O*	User I/O*
5	User I/O*	5 V	User I/O*	User I/O*	User I/O*	5 V	User I/O*	User I/O*

Figure 11-8—10 SU connector sections C and D without Fiber

11.3.2.2 Connector section E

Due to the proliferation of the MIL-STD-1553B interface in the space community, connector section E contains one optional dual-redundant MIL-STD-1553B serial buses as shown in Figure 11-9. The remainder of section E is used for user-defined I/O as shown in Figure 11-10. If the MIL-STD-1553B interface is not used, Figure 11-11 shows user-defined I/O covering the entire connector section E. To use a specific bus with external transformers, the Bus X+ and Bus X– signals should be used. Either a direct-coupled or transformer-coupled implementation may be used. To use a specific bus on the other side of a transformer, the Bus X dc+ and Bus X dc– should be used. Only one of these are required to be used for a given bus X.

	a	b	c	d
6				
7	GND			
8		Bus A–	Bus B–	GND
9		Bus A dc+		
10		Bus A+	2.1 V	Bus B+
11		Bus A dc–	Bus B dc+	Bus B dc–
12		5 V		
13				
14	GND			
15				GND
16				
17			3.3 V	
18				
19		5 V		
20				
21	GND			
22				GND
23				

Figure 11-9—Pinout for 10 SU connector section E (with MIL-STD-1553B)

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	a	b	c	d
6	User I/O*	User I/O*	User I/O*	User I/O*
7		User I/O*	User I/O*	User I/O*
8	User I/O*			
9	User I/O*		User I/O*	User I/O*
10	User I/O*			
11	User I/O*			
12	User I/O*		User I/O*	User I/O*
13	User I/O*	User I/O*	User I/O*	User I/O*
14		User I/O*	User I/O*	User I/O*
15	User I/O*	User I/O*	User I/O*	
16	User I/O*	User I/O*	User I/O*	User I/O*
17	User I/O*	User I/O*		User I/O*
18	User I/O*	User I/O*	User I/O*	User I/O*
19	User I/O*		User I/O*	User I/O*
20	User I/O*	User I/O*	User I/O*	User I/O*
21		User I/O*	User I/O*	User I/O*
22	User I/O*	User I/O*	User I/O*	
23	User I/O*	User I/O*	User I/O*	User I/O*

Figure 11-10—User-Definable I/O for 10 SU connector section E (with MIL-STD-1553B)

	a	b	c	d
6	User I/O*	User I/O*	User I/O*	User I/O*
7		User I/O*	User I/O*	User I/O*
8	User I/O*	User I/O*	User I/O*	
9	User I/O*	User I/O*	User I/O	User I/O*
10	User I/O*	User I/O*		User I/O*
11	User I/O*	User I/O*	User I/O*	User I/O*
12	User I/O*		User I/O*	User I/O*
13	User I/O*	User I/O*	User I/O*	User I/O*
14		User I/O*	User I/O*	User I/O*
15	User I/O*	User I/O*	User I/O*	
16	User I/O*	User I/O*	User I/O*	User I/O*
17	User I/O*	User I/O*		User I/O*
18	User I/O*	User I/O*	User I/O*	User I/O*
19	User I/O*		User I/O*	User I/O*
20	User I/O*	User I/O*	User I/O*	User I/O*
21		User I/O*	User I/O*	User I/O*
22	User I/O*	User I/O*	User I/O*	
23	User I/O*	User I/O*	User I/O*	User I/O*

Figure 11-11—User-Definable I/O for 10 SU connector section E (without MIL-STD-1553B)

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11.3.2.3 Connector section F

Connector section F contains user-defined I/O as shown in Figure 11-12.

	e	f	g	h
6	User I/O*	User I/O*	User I/O*	User I/O*
7		User I/O*	User I/O*	User I/O*
8	User I/O*	User I/O*	User I/O*	
9	User I/O*	User I/O*	User I/O*	User I/O*
10	User I/O*	User I/O*		User I/O*
11	User I/O*	User I/O*	User I/O*	User I/O*
12	User I/O*		User I/O*	User I/O*
13	User I/O*	User I/O*	User I/O*	User I/O*
14		User I/O*	User I/O*	User I/O*
15	User I/O*	User I/O*	User I/O*	
16	User I/O*	User I/O*	User I/O*	User I/O*
17	User I/O*	User I/O*		User I/O*
18	User I/O*	User I/O*	User I/O*	User I/O*
19	User I/O*		User I/O*	User I/O*
20	User I/O*	User I/O*	User I/O*	User I/O*
21		User I/O*	User I/O*	User I/O*
22	User I/O*	User I/O*	User I/O*	
23	User I/O*	User I/O*	User I/O*	User I/O*

Figure 11-12—User-Definable I/O for 10 SU connector section F

11.3.2.4 Connector section G

Connector section G shall contain the Futurebus+ data, control, utility, and arbitration signals. In the 10 SU Dual Futurebus+ configuration, connector section G shall be used for Futurebus+ 1, power, ground, and two key pins. In the 10 SU Error Correcting configuration, connector section G shall be used for a single 64-bit Futurebus+, power, ground, and two key pins. The Single 32-bit or 64-bit Futurebus+ configuration may be implemented as a subset of either the Dual Futurebus+ or the Error Correcting configurations. This is possible because the same pin locations are used for both the Dual Futurebus+ and the Error Correcting configuration pin assignments.

Connector section G shall also be used for central arbitration signals, distributed arbitration signals, +28 V, power, and ground. Modules shall support central arbitration, but distributed arbitration is optional. If distributed arbitration is not implemented, the pins may be used for user-defined I/O. All 10 SU configurations provide at least one set of all central and distributed arbitration signals for each bus implemented.

Figures 11-13 through 11-16 show the implementations for the 10 SU configurations in section G. Figures 11-17 through 11-18 show the user-definable I/O signal locations for each 10 SU configuration in section G. Note that all signals in section G (except **PN** and the sparing pins) are active low.

The I/Os shown with an asterisk in Figures 11-13 through 11-16 are very few in number and isolated from the larger groups on other sections of the connector. For this reason, the user should use these last.

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	a	b	c	d
24	1-RF*	1-SLD*	3.3 V	1-TED*
25	1-AI*	1-AK*	1-AS*	1-ET*
26	1-DI*	5 V	1-DK*	1-DS*
27	1-CA0*	1-CA1*	1-CA2*	1-CP*
28	GND	1-CM0*	1-CM1*	1-CM2*
29	1-CM3*	1-CM4*	1-CM5*	GND
30	1-CM6*	1-CM7*	1-ST0*	1-ST1*
31	1-ST2*	1-ST3*	3.3 V	1-ST4*
32	1-ST5*	1-ST6*	1-ST7*	
33	1-AD2*	5 V	1-AD1*	1-AD0*
34	1-AD5*	1-AD4*	1-AD3*	1-BP0*
35	GND	1-AD7*	1-AD6*	1-AD8*
36	1-AD11*	1-AD10*	1-AD9*	GND
37	1-AD14*	1-AD13*	1-AD12*	1-AD15*
38	1-AD17*	1-AD16*	3.3 V	1-BP1*
39	1-AD21*	1-AD20*	1-AD19*	1-AD18*
40	1-AD23*	5 V	1-AD22*	1-BP2*
41	1-AD27*	1-AD26*	1-AD25*	1-AD24*
42	GND	1-AD30*	1-AD29*	1-AD28*
43	1-AD32*	1-BP3*	1-AD31*	GND
44	1-AD36*	1-AD35*	1-AD34*	1-AD33*
45	1-AD38*	1-AD37*	3.3 V	1-AD39*
46	1-AD42*	1-AD41*	1-AD40*	1-BP4*
47	1-AD44*	5 V	1-AD43*	1-AD47*
48	1-AD48*	1-AD46*	1-AD45*	1-BP5*
49	GND	1-AD51*	1-AD50*	1-AD49*
50	1-AD54*	1-AD53*	1-AD52*	GND
51	1-AD57*	1-AD56*	1-BP6*	1-AD55*
52	1-AD59*	1-AD58	3.3 V	1-AD63
53	1-AD62*	1-AD61*	1-AD60*	1-BP7*
54		5 V		
55				
56	GND			
57				GND
58				
59	1-SB0*	1-RED*	3.3 V	1-SB1*
60	1-TR0*	1-TR1*	1-NED*	1-PFI*
61	1-UMP*	5 V	1-RUN*	1-PN
62	1-RE*	1-SR*	1-AR*	1-AQ*
63	GND	1-RTN-B	1-AP*	1-28 V-B
64	1-28 V-A	1-AC0*	1-RTN-A	GND
65	1-AC1*	1-ABP*	1-AB0*	1-AB1*
66	1-AB2*	1-AB3*	3.3 V	1-AB4*
67	1-AB5*	1-AB6*	1-AB7*	1-RQ0*
68	1-RQ1*	2.1 V	1-GR*	1-PE*
69	GAP*	GA0*	GA1*	GA2*
70	GA3*	KEY	GA4*	KEY

Figure 11-13—Pinout for 10 SU Dual Futurebus+ connector section G

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	a	b	c	d
24	TMRS0*	TMRS1*	3.3 V	TMRS2*
25	AI*	AK*	AS*	ET*
26	DI*	5 V	DK*	DS*
27	CA0*	CA1*	CA2*	CC0*
28	GND	CM0*	CM1*	CM2*
29	CM3*	CM4*	CM5*	GND
30	CM6*	CM7*	ST0*	ST1*
31	ST2*	ST3*	3.3 V	ST4*
32	ST5*	ST6*	ST7*	
33	AD2*	5 V	AD1*	AD0*
34	AD5*	AD4*	AD3*	BC0*
35	GND	AD7*	AD6*	AD8*
36	AD11*	AD10*	AD9*	GND
37	AD14*	AD13*	AD12*	AD15*
38	AD17*	AD16*	3.3 V	BC1*
39	AD21*	AD20*	AD19*	AD18*
40	AD23*	5 V	AD22*	BC2*
41	AD27*	AD26*	AD25*	AD24*
42	GND	AD30*	AD29*	AD28*
43	AD32*	BC3*	AD31*	GND
44	AD36*	AD35*	AD34*	AD33*
45	AD38*	AD37*	3.3 V	AD39*
46	AD42*	AD41*	AD40*	BC4*
47	AD44*	5 V	AD43*	AD47*
48	AD48*	AD46*	AD45*	BC5*
49	GND	AD51*	AD50*	AD49*
50	AD54*	AD53*	AD52*	GND
51	AD57*	AD56*	BC6*	AD55*
52	AD59*	AD58*	3.3 V	AD63*
53	AD62*	AD61*	AD60*	BC7*
54		5 V		
55				
56	GND			
57				GND
58				
59	1-SB0*	REB*	3.3 V	1-SB1*
60	TR0*	TR1*	NED*	PFI*
61	UMP*	5 V	RUN*	PN
62	RE*	SR*	AR*	AQ*
63	GND	1-RTN-B	AP*	1-28 V-B
64	1-28 V-A	AC0*	1-RTN-A	GND
65	AC1*	ABC0*	AB0*	AB1*
66	AB2*	AB3*	3.3 V	AB4*
67	AB5*	AB6*	AB7*	RQ0*
68	RQ1*	2.1 V	GR*	PE*
69	GAP*	GA0*	GA1*	GA2*
70	GA3*	KEY	GA4*	KEY

Figure 11-14—Pinout for 10 SU Error Correcting configuration connector section G

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	a	b	c	d
24	RF*	SLD*	3.3 V	TED*
25	AI*	AK*	AS*	ET*
26	DI*	5 V	DK*	DS*
27	CA0*	CA1*	CA2*	CP*
28	GND	CM0*	CM1*	CM2*
29	CM3*	CM4*	CM5*	GND
30	CM6*	CM7*	ST0*	ST1*
31	ST2*	ST3*	3.3 V	ST4*
32	ST5*	ST6*	ST7*	
33	AD2*	5 V	AD1*	AD0*
34	AD5*	AD4*	AD3*	BP0*
35	GND	AD7*	AD6*	AD8*
36	AD11*	AD10*	AD9*	GND
37	AD14*	AD13*	AD12*	AD15*
38	AD17*	AD16*	3.3 V	BP1*
39	AD21*	AD20*	AD19*	AD18*
40	AD23*	5 V	AD22*	BP2*
41	AD27*	AD26*	AD25*	AD24*
42	GND	AD30*	AD29*	AD28*
43		BP3*	AD31*	GND
44				
45			3.3 V	
46				
47		5 V		
48				
49	GND			
50				GND
51				
52			3.3 V	
53				
54		5 V		
55				
56	GND			
57				GND
58				
59	SB0*	RED*	3.3 V	SB1*
60	TR0*	TR1*	NED*	PFI*
61	UMP*	5 V	RUN*	PN
62	RE*	SR*	AR*	AQ*
63	GND	1-RTN-B	AP*	1-28 V-B
64	1-28 V-A	AC0*	1-RTN-A	GND
65	AC1*	ABP*	AB0*	AB1*
66	AB2*	AB3*	3.3 V	AB4*
67	AB5*	AB6*	AB7*	RQ0*
68	RQ1*	2.1 V	GR*	PE*
69	GAP*	GA0*	GA1*	GA2*
70	GA3*	KEY	GA4*	KEY

Figure 11-15—Pinout for 10 SU 32-bit Single Futurebus+ connector section G

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	a	b	c	d
24	RF*	SLD*	3.3 V	TED*
25	AI*	AK*	AS*	ET*
26	DI*	5 V	DK*	DS*
27	CA0*	CA1*	CA2*	CP*
28	GND	CM0*	CM1*	CM2*
29	CM3*	CM4*	CM5*	GND
30	CM6*	CM7*	ST0*	ST1*
31	ST2*	ST3*	3.3 V	ST4*
32	ST5*	ST6*	ST7*	
33	AD2*	5 V	AD1*	AD0*
34	AD5*	AD4*	AD3*	BP0*
35	GND	AD7*	AD6*	AD8*
36	AD11*	AD10*	AD9*	GND
37	AD14*	AD13*	AD12*	AD15*
38	AD17*	AD16*	3.3 V	BP1*
39	AD21*	AD20*	AD19*	AD18*
40	AD23*	5 V	AD22*	BP2*
41	AD27*	AD26*	AD25*	AD24*
42	GND	AD30*	AD29*	AD28*
43	AD32*	BP3*	AD31*	GND
44	AD36*	AD35*	AD34*	AD33*
45	AD38*	AD37*	3.3 V	AD39*
46	AD42*	AD41*	AD40*	BP4*
47	AD44*	5 V	AD43*	AD47*
48	AD48*	AD46*	AD45*	BP5*
49	GND	AD51*	AD50*	AD49*
50	AD54*	AD53*	AD52*	GND
51	AD57*	AD56*	BP6*	AD55*
52	AD59*	AD58*	3.3 V	AD63*
53	AD62*	AD61*	AD60*	BP7*
54		5 V		
55				
56	GND			
57				GND
58				
59	SB0*	RED*	3.3 V	SB1*
60	TR0*	TR1*	NED*	PFI*
61	UMP*	5 V	RUN*	PN
62	RE*	SR*	AR*	AQ*
63	GND	1-RTN-B	AP*	1-28 V-B
64	1-28 V-A	AC0*	1-RTN-A	GND
65	AC1*	ABP*	AB0*	AB1*
66	AB2*	AB3*	3.3 V	AB4*
67	AB5*	AB6*	AB7*	RQ0*
68	RQ1*	2.1 V	GR*	PE*
69	GAP*	GA0*	GA1*	GA2*
70	GA3*	KEY	GA4*	KEY

Figure 11-16—Pinout for 10 SU 64-bit and 128-bit Single Futurebus+ connector section G

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	a	b	c	d
24				
25				
26				
27				
28				
29				
30				
31				
32				Reserved
33				
34				
35				
36				
37				
38				
39				
40				
41				
42				
43				
44				
45				
46				
47				
48				
49				
50				
51				
52				
53				
54	User I/O*		User I/O*	User I/O*
55	User I/O*	User I/O*	User I/O*	User I/O*
56		User I/O*	User I/O*	User I/O*
57	User I/O*	User I/O*	User I/O*	
58	User I/O*	User I/O*	Reserved	Reserved
59				
60				
61				
62				
63				
64				
65				
66				
67				
68				
69				
70				

Figure 11-17—User-Definable I/O for 10 SU Dual, Error Correcting, 64-bit Single, and 128-bit Single Futurebus+ connector section G

--`,,`-`-`,,`,,`,`,,`---

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	a	b	c	d
24				
25				
26				
27				
28				
29				
30				
31				
32				Reserved
33				
34				
35				
36				
37				
38				
39				
40				
41				
42				
43	User I/O*			
44	User I/O*	User I/O*	User I/O*	User I/O*
45	User I/O*	User I/O*		User I/O*
46	User I/O*	User I/O*	User I/O*	User I/O*
47	User I/O*		User I/O*	User I/O*
48	User I/O*	User I/O*	User I/O*	User I/O*
49		User I/O*	User I/O*	User I/O*
50	User I/O*	User I/O*	User I/O*	
51	User I/O*	User I/O*	User I/O*	User I/O*
52	User I/O*	User I/O*		User I/O*
53	User I/O*	User I/O*	User I/O*	User I/O*
54	User I/O*		User I/O*	User I/O*
55	User I/O*	User I/O*	User I/O*	User I/O*
56		User I/O*	User I/O*	User I/O*
57	User I/O*	User I/O*	User I/O*	
58	User I/O*	User I/O*	Reserved	Reserved
59				
60				
61				
62				
63				
64				
65				
66				
67				
68				
69				
70				

Figure 11-18—User-Definable I/O for 10 SU 32-bit Single Futurebus+ connector section G

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11.3.2.5 Connector section H

Connector section H shall contain data, control, utility, and arbitration lines for the Dual Bus, Error Correcting, and Single 128-bit configurations. In the Dual Bus configuration, section H shall contain the entire Futurebus+ 2. In the Error Correcting configuration, section H shall contain the A and B copies of the control, utility, and arbitration lines and the spare lines. In the Single 128-bit configuration, section H shall contain the address and data lines corresponding to **AD[127..64]***. No signals shall be reserved in the Single 32-bit or Single 64-bit configurations.

For the Dual Futurebus+ and the Error Correcting configuration, several of the system control lines are duplicated to provide fault tolerance. Details of this feature are given in Table 11-1. The remaining area may be used for any local interconnects or user-defined I/O. As a minimum, connector section H shall contain the power pattern specified in Figure 11-21. The user may also define additional power and ground pins, if a unique keying is assigned to that configuration. Figures 11-19 through 11-22 show the pinouts for the 10 SU configurations in section H. Figures 11-23 through 11-26 show the user-definable I/O signal locations for each 10 SU configuration in section H. Note that all signals in section H (except **PN** and the sparing pins) are active low.

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To implement the Single 128-bit Futurebus+, the user should start with the Dual Futurebus+ implementation. The 128-bit Futurebus+ is a modification of the Dual Futurebus+ where the second Futurebus+ pin definition is renamed to define address/data bits 64 through 127 and parity bits 8 through 15. The second set of control signals should be deleted. Note that a Dual Bus backplane may have Dual Bus modules, Single 32-bit modules, and Single 64-bit modules all present concurrently. Single 128-bit modules may be plugged into a Dual Bus backplane if all other modules on the backplane are also Single 128-bit modules. Also note that an Error Correcting configuration backplane may have Error Correcting configuration modules, Single 32-bit modules, and Single 64-bit modules all present concurrently, but the error correction mechanism on the Error Correcting configuration modules must be disabled. Single 64-bit backplanes may contain Single 64-bit modules and Single 32-bit modules concurrently, and Single 128-bit backplanes may contain Single 128-bit modules, Single 32-bit modules, and Single 64-bit modules all present concurrently. Modules present in backplanes that contain modules from more than one configuration may have to operate with reduced functionality.

Table 11-1—Occurrence of space profile system control lines

Signal	32/64/12 Single Futurebus+	Dual Futurebus+	Error Correcting configuration
Utility Spares **UPSP*, UWSP**	0	0	2
Nuclear Event Detect **NED***	1	2	3
Power Failure Imminent **PFI***	1	2	3
Power Normal **PN**	1	2	3
Reset **RE***	1	2	3
Duplicate Reset **RED***	1	2	0
Reset Spare **RES***	0	0	1
Run **RUN***	1	1	1
Serial Bus 0 **SB0***	1	2	2
Serial Bus 1 **SB1***	1	2	2
Trigger 0 Start and Stop **TR0***	1	1	1
Trigger 1 Start and Stop **TR1***	1	1	1
User Console Interface Master Present **UMP***	1	1	1
System Reset **SR***	1	2	3

The 10 SU Dual Bus configuration module shall provide pins for two copies of all central and distributed arbitration signals. The Error Correcting configuration module shall provide pins for three copies of the central arbitration request lines. Only one grant line shall be provided, however, due to coding on the grant line. The distributed arbitration lines are covered by ECC and TMR as described in the fault tolerance section of this document. The Single 32-bit, 64-bit, and 128-bit configurations shall provide one set of all central and

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distributed arbitration signals. All implementations shall provide two +28 V input pins and two +28 V return pins for distributed power.

Table 11-2 shows how the various fault tolerant configurations are overlaid in connector section H. The empty columns and row in Table 11-2 show why Single 32-bit and Single 64-bit modules can operate in backplanes designed for other configurations. This is because the Single 32-bit and Single 64-bit configurations do not use section H for any of their signals, therefore they do not interfere with them. This allows other modules to use section H as if the Single 32-bit or Single 64-bit module were not present.

Table 11-2—10 SU application overlays (section H)

Futurebus+ signals	Dual	Error Correcting	Single 32-bit	Single 64-bit	Single 128-bit
Control:Copy2,A	X	X			
Control:CopyB		X			
AD[63:0]*, BP[7:0]* FB+ 1					
AD[63:0]*, BP[7:0]* FB+ 2	X	Spares			AD[127:64]*, BP[15:8]*

Table 11-3 shows the combinations possible for 10 SU modules and backplanes with equivalent optional features. The size of the backplane is the size of the largest base configuration (128-bit for the Single Futurebus+, 64-bit (2) for the Dual Futurebus+, and 64-bit for the Error Correcting configuration). “No” is used in Table 11-3 to indicate where full configuration connection cannot be achieved physically. In all cases, a single 32-bit Futurebus+ could work as a degraded mode of any of the modules in any of the backplanes, but this is not recommended for final product; such use is envisioned only in laboratory or prototype environments when existing assets are being utilized in a less than optimum manner. Keying is used to prevent invalid combinations in the final product; however, a non-keyed backpanel used for rapid prototyping or other non-flight demonstrations is envisioned to allow the combinations shown in Table 11-3.

Table 11-3—10 SU backplane/module combinations

		MODULE (32-bit/64-bit/128-bit)		
		Single Futurebus+	**Dual Futurebus+**	**Error Correcting configuration**
BACKPLANE	**Single Futurebus+**	Yes/Yes/Yes	No/No/NA	No/No/NA
	Dual Futurebus+	Yes/Yes/Yes[a]	Yes/Yes/NA	No/No/NA
	Error Correcting configuration	Yes/Yes/No	No/No/NA	Yes/Yes/NA

[a] This configuration is possible if the only type of module present is a Single 64-bit Futurebus+.

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	e	f	g	h
24	2-RF*	2-SLD*	3.3 V	2-TED*
25	2-AI*	2-AK*	2-AS*	2-ET*
26	2-DI*	5 V	2-DK*	2-DS*
27	2-CA0*	2-CA1*	2-CA2*	2-CP*
28	GND	2-CM0*	2-CM1*	2-CM2*
29	2-CM3*	2-CM4*	2-CM5*	GND
30	2-CM6*	2-CM7*	2-ST0*	2-ST1*
31	2-ST2*	2-ST3*	3.3 V	2-ST4*
32	2-ST5*	2-ST6*	2-ST7*	
33	2-AD2*	5 V	2-AD1*	2-AD0*
34	2-AD5*	2-AD4*	2-AD3*	2-BP0*
35	GND	2-AD7*	2-AD6*	2-AD8*
36	2-AD11*	2-AD10*	2-AD9*	GND
37	2-AD14*	2-AD13*	2-AD12*	2-AD15*
38	2-AD17*	2-AD16*	3.3 V	2-BP1*
39	2-AD21*	2-AD20*	2-AD19*	2-AD18*
40	2-AD23*	5 V	2-AD22*	2-BP2*
41	2-AD27*	2-AD26*	2-AD25*	2-AD24*
42	GND	2-AD30*	2-AD29*	2-AD28*
43	2-AD32*	2-BP3*	2-AD31*	GND
44	2-AD36*	2-AD35*	2-AD34*	2-AD33*
45	2-AD38*	2-AD37*	3.3 V	2-AD39*
46	2-AD42*	2-AD41*	2-AD40*	2-BP4*
47	2-AD44*	5 V	2-AD43*	2-AD47*
48	2-AD48*	2-AD46*	2-AD45*	2-BP5*
49	GND	2-AD51*	2-AD50*	2-AD49*
50	2-AD54*	2-AD53*	2-AD52*	GND
51	2-AD57*	2-AD56*	2-BP6*	2-AD55*
52	2-AD59*	2-AD58*	3.3 V	2-AD63*
53	2-AD62*	2-AD61*	2-AD60*	2-BP7*
54		5 V		
55				
56	GND			
57				GND
58				
59	2-SB0*	2-RED*	3.3 V	2-SB1*
60			2-NED*	2-PFI*
61		5 V		2-PN
62	2-RE*	2-SR*	2-AR*	2-AQ*
63	GND	2-RTN-B	2-AP*	2-28 V-B
64	2-28 V-A	2-AC0*	2-RTN-A	GND
65	2-AC1*	2-ABP*	2-AB0*	2-AB1*
66	2-AB2*	2-AB3*	3.3 V	2-AB4*
67	2-AB5*	2-AB6*	2-AB7*	2-RQ0*
68	2-RQ1*	2.1 V	2-GR*	2-PE*
69				
70	GND			

Figure 11-19—Pinout for 10 SU Dual Futurebus+ connector section H

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	e	f	g	h
24			3.3 V	
25	AIA*	AKA*	ASA*	ETA*
26	DIA*	5 V	DKA*	DSA*
27	CAA0*	CAA1*	CAA2*	
28	GND	CC1*	CC2*	CC3*
29	CC4*	CMS0*	CMS1*	GND
30			STA0*	STA1*
31	STA2*	STA3*	3.3 V	STA4*
32	STA5*	STA6*	STA7*	
33	ADS2*	5 V	ADS1*	ADS0*
34	ADS5*	ADS4*	ADS3*	
35	GND	ADS7*	ADS6*	BCS0*
36	ADS10*	ADS9*	ADS8*	GND
37	ADS13*	ADS12*	ADS11*	ADS14*
38	BCS1*	ADS15*	3.3 V	
39	AIB*	AKB*	ASB*	ETB*
40	DIB*	5 V	DKB*	
41	DSB*	CAB0*	CAB1*	CAB2*
42	GND	STB0*	STB1*	STB2*
43	STB3*		STB4*	GND
44	STB5*	STB6*	STB7*	TMRS3*
45	TMRS4*		3.3 V	
46				
47		5 V		
48				
49	GND			
50				GND
51				
52			3.3 V	
53				
54		5 V		
55				UWSP
56	GND			UPSP*
57	ARB*	AQB*	APB*	GND
58	ACB0*	ACB1*	NEDB*	ARBS*
59	2-SB0*	RES*	3.3 V	2-SB1*
60	SRB*	PFIB*	NEDA*	PFIA*
61	PNB	5 V	PEB*	PNA
62	REA*	SRA*	ARA*	AQA*
63	GND	2-RTN-B	APA*	2-28 V-B
64	2-28 V-A	ACA0*	2-RTN-A	GND
65	ACA1*	ABC1*	ABC2*	ABC3*
66	ABC4*	ABS0*	3.3 V	ABS1*
67	GCP*	GC0*	GC1*	RQA0*
68	RQA1*	2.1 V	GC2*	PEA*
69	GC3*	GC4*	GC5*	GCS*
70	GND	GRS*	RQB0*	RQB1*

Figure 11-20—Pinout for 10 SU Error Correcting configuration connector section H

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	e	f	g	h
24			3.3 V	
25				
26		5 V		
27				
28	GND			
29				GND
30				
31			3.3 V	
32				
33		5 V		
34				
35	GND			
36				GND
37				
38			3.3 V	
39				
40		5 V		
41				
42	GND			
43				GND
44				
45			3.3 V	
46				
47		5 V		
48				
49	GND			
50				GND
51				
52			3.3 V	
53				
54		5 V		
55				
56	GND			
57				GND
58				
59			3.3 V	
60				
61		5 V		
62				
63	GND	2-RTN-B		2-28 V-B
64	2-28 V-A		2-RTN-A	GND
65				
66			3.3 V	
67				
68		2.1 V		
69				
70	GND			

Figure 11-21—Pinout for 10 SU 32-bit and 64-bit Single Futurebus+ connector section H

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	e	f	g	h
24			3.3 V	
25				
26		5 V		
27				
28	GND			
29				GND
30				
31			3.3 V	
32				
33	AD66*	5 V	AD65*	AD64*
34	AD69*	AD68*	AD67*	BP8*
35	GND	AD71*	AD70*	AD72*
36	AD75*	AD74*	AD73*	GND
37	AD78*	AD77*	AD76*	AD79*
38	AD81*	AD80*	3.3 V	BP9*
39	AD85*	AD84*	AD83*	AD82*
40	AD87*	5 V	AD86*	BP10*
41	AD91*	AD90*	AD89*	AD88*
42	GND	AD94*	AD93*	AD92*
43	AD96*	BP11*	AD95*	GND
44	AD100*	AD99*	AD98*	AD97*
45	AD102*	AD101*	3.3 V	AD103*
46	AD106*	AD105*	AD104*	BP12*
47	AD108*	5 V	AD107*	AD111*
48	AD112*	AD110*	AD109*	BP13*
49	GND	AD115*	AD114*	AD113*
50	AD118*	AD117*	AD116*	GND
51	AD121*	AD120*	BP14*	AD119*
52	AD123*	AD122*	3.3 V	AD127*
53	AD126*	AD125*	AD124*	BP15*
54		5 V		
55				
56	GND			
57				GND
58				
59			3.3 V	
60				
61		5 V		
62				
63	GND	2-RTN-B		2-28 V-B
64	2-28 V-A		2-RTN-A	GND
65				
66			3.3 V	
67				
68		2.1 V		
69				
70	GND			

Figure 11-22—Pinout for 10 SU 128-bit Single Futurebus+ connector section H

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	e	f	g	h
24				
25				
26				
27				
28				
29				
30				
31				
32				Reserved
33				
34				
35				
36				
37				
38				
39				
40				
41				
42				
43				
44				
45				
46				
47				
48				
49				
50				
51				
52				
53				
54	User I/O*		User I/O*	User I/O*
55	User I/O*	User I/O*	User I/O*	User I/O*
56		User I/O*	User I/O*	User I/O*
57	User I/O*	User I/O*	User I/O*	
58	User I/O*	User I/O*	User I/O*	User I/O*
59				
60	User I/O*	User I/O*		
61	User I/O*		User I/O*	
62				
63				
64				
65				
66				
67				
68				
69	User I/O*	User I/O*	User I/O*	User I/O*
70		User I/O*	User I/O*	User I/O*

Figure 11-23—User-Definable I/O for 10 SU Dual Futurebus+ connector section H

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	e	f	g	h
24	User I/O*	User I/O*		User I/O*
25				
26				
27				User I/O*
28				
29				
30	User I/O*	User I/O*		
31				
32				User I/O*
33				
34				User I/O*
35				
36				
37				
38				User I/O*
39				
40				User I/O*
41				
42				
43		User I/O*		
44				
45		User I/O*		User I/O*
46	User I/O*	User I/O*	User I/O*	User I/O*
47	User I/O*		User I/O*	User I/O*
48	User I/O*	User I/O*	User I/O*	User I/O*
49		User I/O*	User I/O*	User I/O*
50	User I/O*	User I/O*	User I/O*	
51	User I/O*	User I/O*	User I/O*	User I/O*
52	User I/O*	User I/O*		User I/O*
53	User I/O*	User I/O*	User I/O*	User I/O*
54	User I/O*		User I/O*	User I/O*
55	User I/O*	User I/O*	User I/O*	
56		User I/O*	User I/O*	
57				
58				
59				
60				
61				
62				
63				
64				
65				
66				
67				
68				
69				
70				

Figure 11-24—User-Definable I/O for 10 SU Error Correcting configuration connector section H

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	e	f	g	h
24	User I/O*	User I/O*		User I/O*
25	User I/O*	User I/O*	User I/O*	User I/O*
26	User I/O*		User I/O*	User I/O*
27	User I/O*	User I/O*	User I/O*	User I/O*
28		User I/O*	User I/O*	User I/O*
29	User I/O*	User I/O*	User I/O*	
30	User I/O*	User I/O*	User I/O*	User I/O*
31	User I/O*	User I/O*		User I/O*
32	User I/O*	User I/O*	User I/O*	User I/O*
33	User I/O*		User I/O*	User I/O*
34	User I/O*	User I/O*	User I/O*	User I/O*
35		User I/O*	User I/O*	User I/O*
36	User I/O*	User I/O*	User I/O*	
37	User I/O*	User I/O*	User I/O*	User I/O*
38	User I/O*	User I/O*		User I/O*
39	User I/O*	User I/O*	User I/O*	User I/O*
40	User I/O*		User I/O*	User I/O*
41	User I/O*	User I/O*	User I/O*	User I/O*
42		User I/O*	User I/O*	User I/O*
43	User I/O*	User I/O*	User I/O*	
44	User I/O*	User I/O*	User I/O*	User I/O*
45	User I/O*	User I/O*		User I/O*
46	User I/O*	User I/O*	User I/O*	User I/O*
47	User I/O*		User I/O*	User I/O*
48	User I/O*	User I/O*	User I/O*	User I/O*
49		User I/O*	User I/O*	User I/O*
50	User I/O*	User I/O*	User I/O*	
51	User I/O*	User I/O*	User I/O*	User I/O*
52	User I/O*	User I/O*		User I/O*
53	User I/O*	User I/O*	User I/O*	User I/O*
54	User I/O*		User I/O*	User I/O*
55	User I/O*	User I/O*	User I/O*	User I/O*
56		User I/O*	User I/O*	User I/O*
57	User I/O*	User I/O*	User I/O*	
58	User I/O*	User I/O*	User I/O*	User I/O*
59	User I/O*	User I/O*		User I/O*
60	User I/O*	User I/O*	User I/O*	User I/O*
61	User I/O*		User I/O*	User I/O*
62	User I/O*	User I/O*	User I/O*	User I/O*
63			User I/O*	
64		User I/O*		
65	User I/O*	User I/O*	User I/O*	User I/O*
66	User I/O*	User I/O*		User I/O*
67	User I/O*	User I/O*	User I/O*	User I/O*
68	User I/O*		User I/O*	User I/O*
69	User I/O*	User I/O*	User I/O*	User I/O*
70		User I/O*	User I/O*	User I/O*

Figure 11-25—User-Definable I/O for 10 SU 32-bit and 64-bit Single Futurebus+ connector section H

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	e	f	g	h
24	User I/O*	User I/O*		User I/O*
25	User I/O*	User I/O*	User I/O*	User I/O*
26	User I/O*		User I/O*	User I/O*
27	User I/O*	User I/O*	User I/O*	User I/O*
28		User I/O*	User I/O*	User I/O*
29	User I/O*	User I/O*	User I/O*	
30	User I/O*	User I/O*	User I/O*	User I/O*
31	User I/O*	User I/O*		User I/O*
32	User I/O*	User I/O*	User I/O*	User I/O*
33				
34				
35				
36				
37				
38				
39				
40				
41				
42				
43				
44				
45				
46				
47				
48				
49				
50				
51				
52				
53				
54	User I/O*		User I/O*	User I/O*
55	User I/O*	User I/O*	User I/O*	User I/O*
56		User I/O*	User I/O*	User I/O*
57	User I/O*	User I/O*	User I/O*	
58	User I/O*	User I/O*	User I/O*	User I/O*
59	User I/O*	User I/O*		User I/O*
60	User I/O*	User I/O*	User I/O*	User I/O*
61	User I/O*		User I/O*	User I/O*
62	User I/O*	User I/O*	User I/O*	User I/O*
63			User I/O*	
64		User I/O*		
65	User I/O*	User I/O*	User I/O*	User I/O*
66	User I/O*	User I/O*		User I/O*
67	User I/O*	User I/O*	User I/O*	User I/O*
68	User I/O*		User I/O*	User I/O*
69	User I/O*	User I/O*	User I/O*	User I/O*
70		User I/O*	User I/O*	User I/O*

Figure 11-26—User-Definable I/O for 10 SU 128-bit Single Futurebus+ connector section H

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11.3.3 Central arbiter definition

For central arbiter modules, most of the locations previously reserved for user-defined I/O are redefined to support central arbitration. These locations are distributed across connector sections E, F, G, and H. Arbitration lines are assigned starting with section F, then E, then G, and finally H.

Each 10 SU configuration supports a different number of modules, depending upon the number of arbitration lines required and the number of unused connector pins. Each bus of a Dual Futurebus+ module requires three unique lines: **1-RQ0***, **1-RQ1***, and **1-GR***, or **2-RQ0***, **2-RQ1***, and **2-GR***. When all unused connector pins are assigned to central arbitration this module will support 26 external modules. Each Error Correcting configuration module requires seven unique lines: **RQ0***, **RQA0***, **RQB0***, **RQ1***, **RQA1***, **RQB1***, and **GR***. When all unused connector pins are assigned to central arbitration this module will support 25 external modules. Any of the Single Futurebus+ Configurations require only three unique lines for each module: **RQ0***, **RQ1***, and **GR***. These modules easily support the full 31 modules specified by IEEE Std 896.2-1991. The Space Profile Working Group only simulated systems up to 15 slots. Building a system above 15 slots should be preceded by sufficient simulation to guarantee its operation.

Note that the Dual Bus central arbiter slot can accept either Dual Bus or Single Futurebus+ (32-bit or 64-bit) Profile S central arbiter modules. A Single Futurebus+ central arbiter module can properly operate only the first 16 backplane slots in a Dual Bus backplane. Like the Dual Bus configuration, the Error Correcting configuration can also use Single Futurebus+ (32-bit or 64-bit) Profile S central arbiter modules, but the error correcting functionality on the Error Correcting configuration modules must be disabled. Single Futurebus+ central arbiter slots can only be occupied by Single Futurebus+ central arbiters, but 32-bit, 64-bit, and 128-bit central arbiters will properly operate in a 128-bit backplane, and 32-bit and 64-bit central arbiters will properly operate in a 64-bit backplane, and 32-bit central arbiters will properly operate in a 32-bit backplane.

Figures 11-27 through 11-29 show the central arbitration assignments for all 10 SU configurations. Note that all central arbitration signals are active low.

The Central Arbiter function for each of the two busses of a Dual Futurebus+ configuration may either be combined into a single slot or spread across two slots. If combined, then Figure 11-27 shall be used to assign the pins. If separate, then Figure 11-29 shall be used to assign the pins for each bus. This allows the same Central Arbiter Module Type to be used for each module. Additionally, more than one slot per bus may be occupied by a central arbiter module. In this case, only one module shall be actively driving Central Arbiter grants (**GR-x***) and preempt (**PE*** during reset) at a time. Others on the same bus must be disabled and tristated or powered off. When redundancy is used, stub lengths and spacings for the **RQ0-x*, RQ1-x*, and GR-x*** for each bus shall be maintained. In a single central arbiter per bus system, these signals have no stub length requirements since they are wired point to point.

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	a	b	c	d	e	f	g	h
1								
2								
3								
4								
5								
6	1-RQ1-19*				2-RQ1-11*	2-GR-11*	1-RQ0-12*	1-RQ1-12*
7						1-RQ1-11*	1-GR-11*	2-RQ0-11*
8					2-RQ1-10*	2-GR-10*	1-RQ0-11*	
9					1-RQ0-10*	1-RQ1-10*	1-GR-10*	2-RQO-10*
10					2-RQ0-9*	2-RQ1-9*		2-GR-9*
11					2-GR-8*	1-RQ0-9*	1-RQ1-9*	1-GR-9*
12	2-RQ1-18*		2-GR-18*	1-RQ0-19*	1-GR-8*		2-RQ0-8*	2-RQ1-8*
13	1-RQ0-18*	1-RQ1-18*	1-GR-18*	2-RQ0-18*	2-RQ1-7*	2-GR-7*	1-RQ0-8*	1-RQ1-8*
14		2-RQ0-17*	2-RQ1-17*	2-GR-17*		1-RQ1-7*	1-GR-7*	2-RQ0-7*
15	1-RQ0-17*	1-RQ1-17*	1-GR-17*		2-RQ1-6*	2-GR-6*	1-RQ0-7*	
16	1-GR-16*	2-RQ0-16*	2-RQ1-16*	2-GR-16*	1-RQ0-6*	1-RQ1-6*	1-GR-6*	2-RQ0-6*
17	2-GR-15*	1-RQ0-16*		1-RQ1-16*	2-RQ0-5*	2-RQ1-5*		2-GR-5*
18	1-RQ1-15*	1-GR-15*	2-RQ0-15*	2-RQ1-15*	2-GR-4*	1-RQ0-5*	1-RQ0-5*	1-GR-5*
19	2-RQ1-14*		2-GR-14*	1-RQ0-15*	1-GR-4*		2-RQ0-4*	2-RQ1-4*
20	1-RQ0-14*	1-RQ1-14*	1-GR-14*	2-RQ0-14*	2-RQ1-3*	2-GR-3*	1-RQ0-4*	1-RQ1-4*
21		2-RQ0-13*	2-RQ1-13*	2-GR-13*		1-RQ1-3*	1-GR-3*	2-RQ0-3*
22	1-RQ0-13*	1-RQ1-13*	1-GR-13*		2-RQ1-2*	2-GR-2*	1-RQ0-3*	
23	1-GR-12*	2-RQ0-12*	2-RQ1-12*	2-GR-12*	1-RQ0-2*	1-RQ1-2*	1-GR-2*	2-RQ0-2*
24								
25								
26								
27								
28								
29								
30								
31								
32								2-GR-26*
33								
34								
35								
36								
37								
38								
39								
40								
41								
42								
43								
44								
45								
46								
47								
48								
49								
50								

Figure 11-27—Maximum central arbiter definition for 10 SU Dual Futurebus+

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	a	b	c	d	e	f	g	h
51								
52								
53								
54	2-RQ1-21*		2-GR-21*	1-RQ0-22*	1-GR-26*		2-RQ0-26*	2-RQ1-26*
55	1-RQ0-21*	1-RQ1-21*	1-GR-21*	2-RQ0-21*	2-RQ1-25*	2-GR-25*	1-RQ0-26*	1-RQ1-26*
56		2-RQ0-20*	2-RQ1-20*	2-GR-20*		1-RQ1-25*	1-GR-25*	2-RQ0-25*
57	1-RQ0-20*	1-RQ1-20*	1-GR-20*		2-RQ1-24*	2-GR-24*	1-RQ0-25*	
58	1-GR-19*	2-RQ0-19*	2-RQ1-19*	2-GR-19*	1-RQ0-24*	1-RQ1-24*	1-GR-24*	2-RQ0-24*
59								
60								
61					2-RQ1-23*	2-GR-23*		
62					1-GR-23*		2-RQ0-23*	
63								
64								
65								
66								
67								
68								
69					2-RQ1-22	2-GR-22	1-RQ0-23	1-RQ1-23
70						1-RQ1-22	1-GR-22	2-RQ0-22

Figure 11-27—Maximum central arbiter definition for 10 SU Dual Futurebus+ *(continued)*

	a	b	c	d	e	f	g	h
1								
2								
3								
4								
5								
6	RQB1-9*				RQ1-21*	GR-21*	RQ0-22*	RQ1-22*
7						RQ1-20*	GR-20*	RQ0-21*
8					RQ1-19*	GR-19*	RQ0-20*	
9					RQ0-18*	RQ1-18*	GR-18*	RQ0-19*
10					RQ0-17*	RQ1-17*	GR-17*	
11					GR-15*	RQ0-16*	RQ1-16*	GR-16*
12	RQA0-9*		RQA1-9*	RQB0-9*	GR-14*		RQ0-15*	RQ1-15*
13	RQA0-8*	RQA1-8*	RQB0-8*	RQB1-8*	RQ1-13*	GR-13*	RQ0-14*	RQ1-14*
14		RQA1-7*	RQB0-7*	RQB1-7*		RQ1-12*	GR-12*	RQ0-13*
15	RQB0-6*	RQB1-6*	RQA0-7*		RQ1-11*	GR-11*	RQ0-12*	
16	RQB0-5*	RQB1-5*	RQA0-6*	RQA1-6*	RQ0-10*	RQ1-10*	GR-10*	RQ0-11*
17	RQB1-4*	RQA0-5*		RQA1-5*	RQ0-9*	RQ1-9*		GR-9*
18	RQB1-3*	RQA0-4*	RQA1-4*	RQB0-4*	GR-7*	RQ0-8*	RQ1-8*	GR-8*
19	RQA0-3*		RQA1-3*	RQB0-3*	GR-6*		RQ0-7*	RQ1-7*
20	RQA0-2*	RQA1-2*	RQB0-2*	RQB1-2*	RQ1-5*	GR-5*	RQ0-6*	RQ1-6*
21		RQ0-25*	RQ1-25*	GR-25*		RQ1-4*	GR-4*	RQ0-5*
22	RQ0-24*	RQ1-24*	GR-24*		RQ1-3*	GR-3*	RQ0-4*	
23	GR-22*	RQ0-23*	RQ1-23*	GR-23*	RQ0-2*	RQ1-2*	GR-2*	RQ0-3*

Figure 11-28—Maximum central arbiter definition for 10 SU Error Correcting configuration

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	a	b	c	d	e	f	g	h
24								RQB1-15*
25								
26								
27								
28								
29								
30					RQB0-25*	RQB1-25*		
31								
32				RQA1-14*				RQA1-25*
33								
34								RQA0-25*
35								
36								
37								
38								RQB1-24*
39								
40								RQB0-24*
41								
42								
43						RQA1-24*		
44								
45						RQB1-23*		RQA0-24*
46					RQB1-22*	RQA0-23*	RQA1-23*	RQB0-23*
47					RQA0-22*		RQA1-22*	RQB0-22*
48					RQA0-21*	RQA1-21*	RQB0-21*	RQB1-21*
49						RQA1-20*	RQB0-20*	RQB1-20*
50					RQB0-19*	RQB1-19*	RQA0-20*	
51					RQB0-18*	RQB1-18*	RQA0-19*	RQA1-19*
52					RQB1-17*	RQA0-18*		RQA1-18*
53					RQB1-16*	RQA0-17*	RQA1-17*	RQB0-17*
54	RQB0-13*		RQB1-13*	RQA0-14*	RQA0-16*		RQA1-16*	RQB0-16*
55	RQB0-12*	RQB1-12*	RQA0-13*	RQA1-13*	RQA0-15*	RQA1-15*	RQB0-15*	
56		RQB1-11*	RQA0-12*	RQA1-12*		RQB0-14*	RQB1-14*	
57	RQA0-11*	RQA1-11*	RQB0-11*					
58	RQA0-10*	RQA1-10*	RQB0-10*	RQB1-10*				
59								
60								
61								
62								
63								
64								
65								
66								
67								
68								
69								
70								

Figure 11-28—Maximum central arbiter definition for 10 SU Error Correcting configuration *(continued)*

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	a	b	c	d	e	f	g	h
1								
2								
3								
4								
5								
6					RQ1-21*	GR-21*	RQ0-22*	RQ1-22*
7						RQ1-20*	GR-20*	RQ0-21*
8					RQ1-19*	GR-19*	RQ0-20*	
9					RQ0-18*	RQ1-18*	GR-18*	RQ0-19*
10					RQ0-17*	RQ1-17*	GR-17*	
11					GR-15*	RQ0-16*	RQ1-16*	GR-16*
12					GR-14*		RQ0-15*	RQ1-15*
13					RQ1-13*	GR-13*	RQ0-14*	RQ1-14*
14						RQ1-12*	GR-12*	RQ0-13*
15					RQ1-11*	GR-11*	RQ0-12*	
16	GR-30*	RQ0-31*	RQ1-31*	GR-31*	RQ0-10*	RQ1-10*	GR-10*	RQ0-11*
17	GR-29*	RQ0-30*		RQ1-30*	RQ0-9*	RQ1-9*		GR-9*
18	RQ1-28*	GR-28*	RQ0-29*	RQ1-29*	GR-7*	RQ0-8*	RQ1-8*	GR-8*
19	RQ1-27*		GR-27*	RQ0-28*	GR-6*		RQ0-7*	RQ1-7*
20	RQ0-26*	RQ1-26*	GR-26*	RQ0-27*	RQ1-5*	GR-5*	RQ0-6*	RQ1-6*
21		RQ0-25*	RQ1-25*	GR-25*		RQ1-4*	GR-4*	RQ0-5*
22	RQ0-24*	RQ1-24*	GR-24*		RQ1-3*	GR-3*	RQ0-4*	
23	GR-22*	RQ0-23*	RQ1-23*	GR-23*	RQ0-2*	RQ1-2*	GR-2*	RQ0-3*
24								
25								
26								
27								
28								
29								
30								
31								
32								
33								
34								
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44								
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46								
47								
48								
49								

Figure 11-29—Maximum central arbiter definition for 10 SU 32-bit, 64-bit and 128-bit Single Futurebus+

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	a	b	c	d	e	f	g	h
50								
51								
52								
53								
54								
55								
56								
57								
58								
59								
60								
61								
62								
63								
64								
65								
66								
67								
68								
69								
70								

Figure 11-29—Maximum central arbiter definition for 10 SU 32-bit, 64-bit and 128-bit Single Futurebus+ *(continued)*

11.3.4 Power pin assignments

All connector sections shall be utilized for supplying digital power to Profile 10 SU modules. Connector sections E, F, G, and H shall be utilized for supplying digital ground to Profile 10 SU modules in all configurations. Connector sections C and D shall also be used to supply ground in non-fiber applications. The power pin assignments for the connector sections shall be as shown in Figure 11-30. If unused on the module, these pins shall remain reserved.

Table 11-4 lists the required (+5 V, +3.3 V, +2.1 V, and +28 V) power pins per voltage level and ground pins for the 10 SU module. Wiring of +5 V, +3.3 V, +2.1 V, and +28 V in the backplane is required. Support of these voltages on the modules, beyond maintaining the required pin assignments, is optional. Additional power pins may be implemented on connector sections E, F, G, and H if appropriate keying definitions are created.

The +28 V supplies have been labeled A and B in case independent supplies are provided. A module may use power from either +28 V supply or both. A module shall treat the two supplies as separate power sources and provide separate return paths to the appropriate return signals.

Two +5 V and two +3.3 V pins have been designated as unswitched power inputs, **5 V US** and **3.3 V US**. If there is any power switching in the system, then these signals shall be used to pass unswitched power to the module separate from the switched power passed on the other +5 V and +3.3 V power inputs in order to power specific elements continuously (such as clocks or non-volatile memory). Both switched and unswitched power returns shall use 0 V (**GND**). If a module is always powered it shall only use the switched power pins.

The pin assignments for power and ground for all 10 SU implementations are given in Figure 11-30.

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	a	b	c	d	e	f	g	h
1				GND				GND
2								
3			3.3 V				3.3 V	
4								
5		5 V				5 V		
6								
7	GND				GND			
8				GND				GND
9								
10			2.1 V				3.3 V US	
11								
12		5 V				5 V US		
13								
14	GND				GND			
15				GND				GND
16								
17			3.3 V				3.3 V	
18								
19		5 V				5 V		
20								
21	GND				GND			
22				GND				GND
23								
24			3.3 V				3.3 V	
25								
26		5 V				5 V		
27								
28	GND				GND			
29				GND				GND
30								
31			3.3 V				3.3 V	
32								
33		5 V				5 V		
34								
35	GND				GND			
36				GND				GND
37								
38			3.3 V				3.3 V	
39								
40		5 V				5 V		
41								
42	GND				GND			
43				GND				GND
44								
45			3.3 V				3.3 V	
46								
47		5 V				5 V		
48								
49	GND				GND			
50				GND				GND

Figure 11-30—Power pin assignments for module 10 SU

--`,,`-`-`,,`,,`,`,,`---

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	a	b	c	d	e	f	g	h
51								
52			3.3 V				3.3 V	
53								
54		5 V				5 V		
55								
56	GND				GND			
57				GND				GND
58								
59			3.3 V				3.3 V	
60								
61		5 V				5 V		
62								
63	GND	RTN-B		28 V-B	GND	RTN-B		28 V-B
64	28 V-A		RTN-A	GND	28 V-A		RTN-A	GND
65								
66			3.3 V				3.3 V US	
67								
68		2.1 V				5 V US		
69								
70					GND			

Figure 11-30—Power pin assignments for module 10 SU *(continued)*

Table 11-4—Required power pins per voltage level for module 10 SU

Voltage	Number of pins
+5 V	19
+5 V US	2
+3.3 V	19
+3.3 V US	2
2.1 V	2
+28 V	2
28 V-RTN	2
GND (+5 V, +3.3 V, and +2.1 V RTN)	39

11.3.5 Connector keying

Keying is a required feature used to avoid interoperability conflicts between Profile S modules, or between modules that belong to different profiles but have compatible mechanical characteristics. Keying puts constraints on which modules can be inserted into which slots. Keying is necessary where a backplane has been built with slot-unique characteristics. Keying is also necessary when non-IEEE Std 896.10-1997 electrical compliant drivers may assert signals on user defined lines. Each 10 SU module shall contain three keying pins: alpha, beta, and gamma (defined and referenced in EIA PN 2933A). Each of these keys shall have eight different positions. The alpha key shall be located at the end of the connector labelled with the lowest row number. The beta key shall be located at the end of the connector labelled with the highest row number. The gamma key shall be located in the middle of the connector. All 10 SU modules shall use keying. It is required that matching keying is used on all 10 SU backplanes although the absence of such keying is allowed in a lab environment for a degraded level (single bus) for demonstrations and concept proving activities.

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The alpha key shall be used to represent the bus size and configuration. The keys used shall be

Position A: 32-Bit Single Futurebus+
Position B: 32-Bit Dual Futurebus+
Position C: 32-Bit Error Correcting configuration
Position D: 64-Bit Single Futurebus+
Position E: 64-Bit Dual Futurebus+
Position F: 64-Bit Error Correcting configuration
Position G: 128-Bit Single Futurebus+
Position H: Reserved

The beta key shall be used to represent the various options present: The keys used shall be

Position A: No options present
Position B: MIL-STD-1553B present
Position C: Central Arbiter present
Position D: MIL-STD-1553B and Central Arbiter present
Position E–H: Reserved

The gamma key is reserved for vendor applications.

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12. Profile S electrical

12.1 Backplane characteristics and design requirements

This subclause ensures electrical interoperability between Profile S modules by specifying backplane signalling requirements. First, output driver functions (either push-pull or wire-or) for each backplane signal are identified. Then backplane bus signalling voltage levels are specified, along with characteristics of these signals such as incident wave switching and rise and fall times. Finally, backplane signal voltage level threshold regions are detailed to ensure proper translation between the backplane and Profile S modules.

12.1.1 Geographical address lines

The geographical address pins, **GA[4..0]***, shall provide a binary encoded number on the connector representing the slot number in which it is located, with **GA4*** being the most significant bit, and **GA0*** being the least significant bit. The slots shall be numbered in ascending order. The numbering should be contiguous (note that slot 31 is reserved by IEEE Std 896.2-1991). The leftmost slot, when viewed from the front of the rack, is slot number 1. **GAP*** shall provide even parity across **GA[4..0]***.

On the **GA[4..0]*** and **GAP*** pins, logic zero is represented by an open circuit on the backplane and logic one by grounding the pin on the backplane.

12.1.2 Impedance

Backplane signal traces, including the backplane halves of the signal connectors and vias but not including add-in circuit modules, shall present an effective characteristic impedance, Z_o, between 62 Ω and 72 Ω with a nominal value of 67 Ω.

12.1.3 Resistance

The maximum signal trace resistance corresponding to the maximum possible signal path length (i.e,. from one end of the bus to the other end) shall not exceed 1 Ω. All 0 V logic pins shall be tied to the 0 V dc ground plane at their connector pin positions.

12.1.4 Maximum propagation delay

The maximum one-way propagation delay on a push-pull signal line, in a fully loaded system having modules exhibiting the maximum loading capacitance specified in this profile, shall not be greater than 4 ns (8 ns round trip). [This parameter is derived using a 15-slot backplane built with a polyimide permittivity material (Er = 3.5) and fully populated on a folded backplane with an electrical pitch two times the mechanical pitch of the module.]

The maximum one-way propagation delay on a wire-or signal line, in a fully loaded system having modules exhibiting the maximum loading capacitance specified in this profile, shall not be greater than 5 ns (10 ns round trip). [This parameter is derived using a 15-slot backplane built with a polyimide permittivity material (Er = 3.5) and fully populated on a straight backplane with an electrical pitch equal to the mechanical pitch of the module.]

12.1.5 Termination

All push-pull signals shall be actively terminated on each module to either 2.1 V or 1.0 V depending on the current state of each signal line. No bus termination is required on the backplane for these signals. The backplane shall use a folded looped termination for these signals where two traces are run for each push-pull signal. Every other slot will tie to each trace. These traces are then tied together on each end of the backpanel so

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that a continuous loop or folded termination is maintained such that a signal may reach a board from either direction without reflection. Figure 12-1 illustrates the various types of termination.

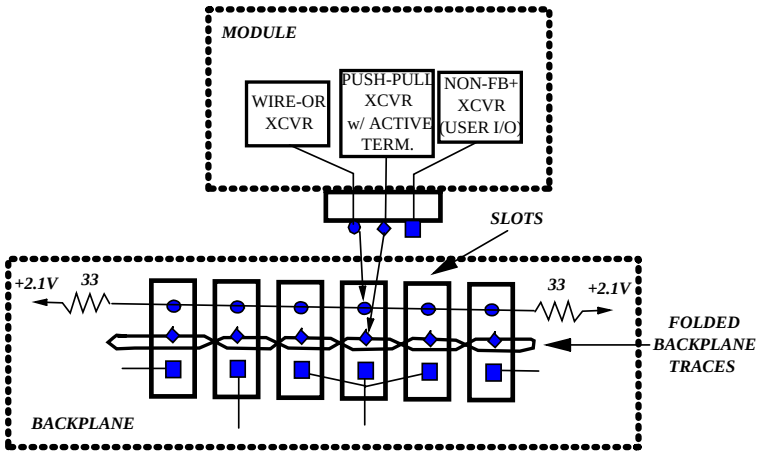

Figure 12-1—Backplane termination

Active termination is affected when the input bias strength is close to the characteristic impedance of the backplane and the bias direction tracks the backplane logic level. When an incident wave arrives at the input of the backplane I/O buffer, it encounters a matching impedance biased to the previously driven logic state. After the backplane voltage crosses the input switching threshold voltage of the input buffer, both the output of the input buffer and the input bias direction switch to match the new backplane logic level. If the reactive energy of the backplane trace is not fully dissipated at this point, the backplane voltage step would double if not for the active feedback regulation that clamps the backplane voltage between VCL and VCH. The initial current associated with this clamp action is just equal to the current that a matching resistor would draw. The clamp current goes to zero as the reactive trace energy is dissipated. In this manner, the active termination automatically adjusts its duration to properly terminate any trace.

All wire-or signals shall be terminated on the backplane to 2.1 V through a 33 Ω resistor at each end of the backplane. No termination is required on the module for these signals.

12.1.6 Parallel protocol signal lines

All parallel protocol signal lines for a given Futurebus+ configuration shall be implemented as shown in Table 12-1. These signals shall be bused to all Futurebus+ slots.

12.1.7 Central arbitration signal lines

ISO/IEC 10857: 1994 defines a set of central arbitration signal lines **RQ[1,0]***, **GR***, **PE***, and **ET***. These signals shall be as shown in Table 12-1. **RQ[1,0]*** and **GR*** shall be radially connected from each central arbiter to each Profile S Futurebus+ slot. **PE*** and **ET*** shall be bused to all Futurebus+ slots of Profile S backplanes.

12.2 Module electrical characteristics and design requirements

12.2.1 Geographical address lines

A module shall attach each of its five **GA[4...0]*** pins and its **GAP*** pin through a resistor to a voltage (V_r) that, when interfaced with the appropriate logic on the module, is interpreted as a logic zero by that logic if the backplane does not ground that pin. The resistor shall limit current on any GA line to 500 μA maximum.

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Table 12-1—Number of drivers for each configuration

	Configurations (Single/Dual/Error Correcting)	
Signal name	**Push-Pull**	**Wire-or**
Information lines		
AD[]*: 32-bit	32/64/32	0/0/0
64-bit	64/128/64	0/0/0
128-bit	128/-/-	0/-/-
ADS[]* 32-bit	0/0/8	0/0/0
64-bit	0/0/16	0/0/0
BP[]*: 32-bit	4/8/0	0/0/0
64-bit	8/16/0	0/0/0
128-bit	16/-/-	0/-/-
BCS[]*	0/0/2	0/0/0
BC[]*	-/-/8	-/-/0
CM[]*	8/16/8	0/0/0
CMS[]*	0/0/2	0/0/0
CP*	1/2/-	0/0/-
CC[]*	-/-/5	-/-/0
RF*	1/2/-	0/0/-
ST[]*	0/0/0	8/16/24
TED*	0/0/0	1/2/0
SLD*	0/0/0	1/2/0
CA[]*	0/0/0	3/6/9
TMRS[]*	0/0/0	0/0/5
Synchronization lines		
AS*	1/2/3	0/0/0
AK*	0/0/0	1°/2°/3°
AI*	0/0/0	1°/2°/3°
DS*	1/2/3	0/0/0
DK*	0/0/0	1°/2°/3°
DI*	0/0/0	1°/2°/3°
ET*	1/2/3	0/0/0
Utility		
NED*	1/2/3	0/0/0
PN	0/0/0	1/2/3
PFI*	1/2/3	0/0/0
RUN	1/1/1	0/0/0
TR0	0/0/0	1/1/1
TR1	0/0/0	1/1/1
UMP	1/1/1	0/0/0
SR*	1/2/3	0/0/0
UPSP*/UWSP	0/0/1	0/0/1
Central arbitration lines		
RQ[]*	2/4/6	0/0/0
GR*	1/2/2	0/0/0
PE*	1/2/3	0/0/0
GRS*/GCS*	0/0/2	0/0/0

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Table 12-1—Number of drivers for each configuration *(continued)*

		Configurations (Single/Dual/Error Correcting)	
Signal name		**Push-Pull**	**Wire-or**
Arbitrated message lines			
AB[]*		0/0/0	8°/16°/8°
ABP*		0/0/0	1/2/0
ABC[]*		0/0/0	0/0/5°
AP*		0/0/0	1°/2°/3°
AQ*		0/0/0	1°/2°/3°
AR*		0/0/0	1°/2°/3°
AC[]*		0/0/0	2°/4°/6°
ABS[]*, ARBS*		0/0/0	0/0/3°
Reset/Bus initialization lines			
RE*		0/0/0	1°/2°/3°
RED*		0/0/0	1°/2°/0
RES*		0/0/0	0/0/1°
Geographical address lines (Transceiver not required)			
GA[]*		0/0/0	0/0/0
GAP*		0/0/0	0/0/0
Serial bus (backplane)			
SB0*		0/0/0	1/2/2
SB1*		0/0/0	1/2/2
Total (Central Arbitration)	32-bit 64-bit 128-bit	58/114/98 94/186/138 166/-/-	24/46/64 24/46/64 24/-/-
Total (Distributed Arbitration)	32-bit 64-bit 128-bit	58/114/98 94/186/138 166/-/-	38/74/95 38/74/95 38/-/-

NOTES
1—Signals marked with (°) require glitch filtering.
2—Spare signals required for the Error Correcting Configuration are not included in the above counts.
3—Signals marked with (-) represent configurations not supported by Profile S.

Optionally, the module may also bypass each of its **GA[4...0]*** pins and its **GAP*** pin with a low-inductance capacitor of 100 pF to module GND. See Figure 12-2.

12.2.2 Stub lengths

Stub length of conductors from the top surface of the transceiver pad to the top of surface of the connector pad on the module, not including connector pin length or the transceiver lead length, shall not exceed 51 mm (2 in). A stub length of 40 mm (1.57 in) or less is recommended. Transceivers may be mounted on one or both sides of the SEM-E Stretch or 10 SU module.

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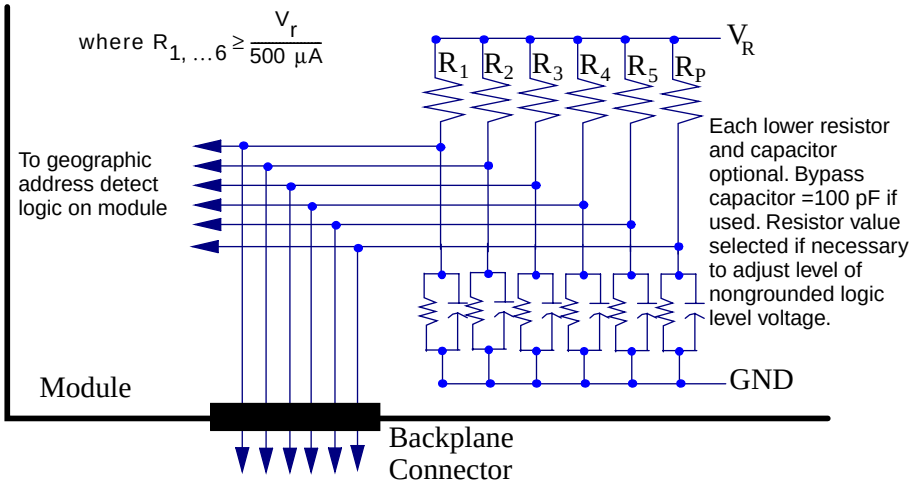

Figure 12-2—Geographic address lines

12.2.3 Driver characteristics

In order to comply with the signal protocol specified in this document, a Profile S module provides two types of backplane output drivers: wire-or and push-pull. Wired-or drivers permit multiple drivers on a single backplane trace. Push-pull drivers, however, are used where the protocol ensures that only one driver is active. Table 12-1 identifies the number of each type of line in each configuration.

12.2.4 Switching voltage characteristics

The backplane delivers signalling information from one Profile S module to another. The signalling information specified is represented by binary data and is transmitted in the form of voltage levels.

12.2.4.1 Logic voltage levels

A logic zero voltage level shall be represented by a voltage equal to or greater than 2.0 V and less than or equal to 3.0 V. A logic one shall be represented by a voltage equal to or greater than 0.2 V and less than or equal to 1.1 V. These levels are shown in Figure 12-3.

12.2.4.2 Input threshold voltages

The center threshold voltage is 1.55 V. The threshold voltage range for a logic one to logic zero transition shall be equal to or greater than 1.65 V and less than or equal to 1.8 V. The threshold voltage range for a logic zero to logic one transition shall be equal to or less than 1.45 V and greater than or equal to 1.3 V. These threshold ranges are shown in Figure 12-4.

12.2.4.3 Incident wave switching

Incident wave switching is employed in high-performance systems to eliminate settling time (time waiting for reflections to assist with logic transitions). Incident wave switching requires that the initial voltage step launched by the driver exceeds the input switching threshold levels of all receivers. This minimizes skew between modules and ensures clean logic transitions. Profile S modules shall employ incident wave switching.

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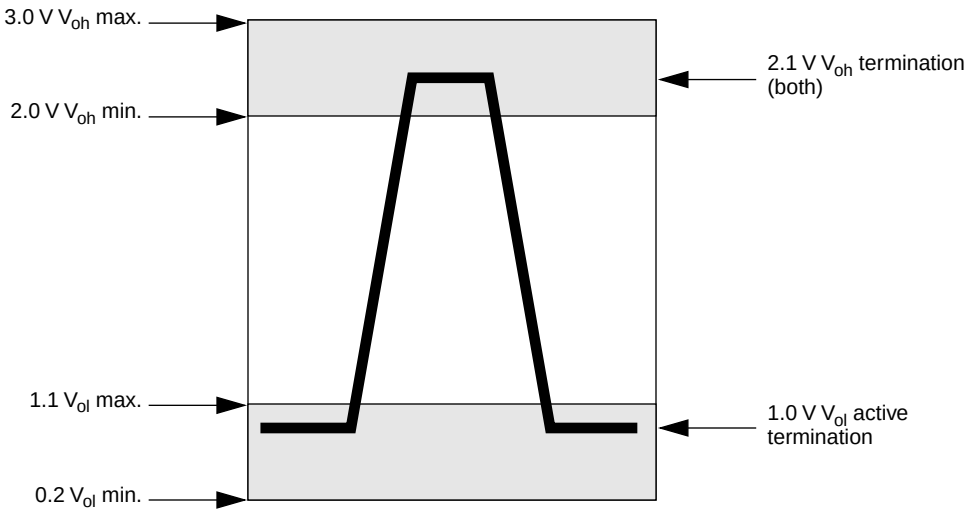

Figure 12-3—Backplane operating voltage levels

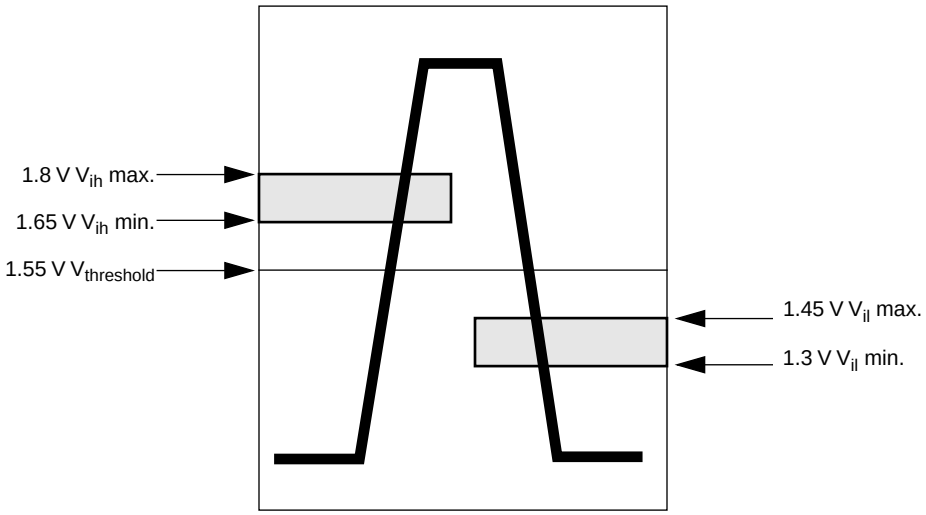

Figure 12-4—Backplane operating threshold voltage levels

12.2.4.4 Rise and fall times

The minimum rise or fall time shall be 2 ns and the maximum rise or fall time shall be 6 ns.

12.2.5 Wire-or driver glitch filtering

Signal traces with wire-or drivers have the unavoidable side effect of glitches. Glitches occur when individual drivers release the load applied to the shared signal line. Since rise times are less than the propagation time of a signal to travel from one end of the backplane to the other, glitches will be detected as legitimate signals unless filtering is provided. The amount of filtering is measured by the maximum glitch pulse width to be extracted before passing the signal to the bus protocol logic. The amount of filtering varies with system configurations and is equal to the time it takes for a signal to propagate from one end of the system and back. The lines requiring glitch filtering are designated in Table 12-1 with (°).

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Profile S modules shall provide glitch filtering for 4 ns, 8 ns, and 12 ns glitch pulse widths. Profile S modules shall also be capable of turning off glitch filtering. Glitch filtering shall be a programmable feature of all Profile S modules.

12.2.6 Transceiver power-on and disabling

Transceivers shall power-up without generating active low glitches and shall be capable of being disabled so all signal lines are released on the bus. Transceivers shall tolerate any power-up and power-down sequence of supply voltage (Device Vcc) and 2.1 V Termination Supply without damage. All Profile S modules shall be cold-spareable, that is a powered down Profile S module shall not preclude operation of the backplane between other Profile S modules that are powered.

12.2.7 Utility signals

The Utility signal discretes defined in 4.2.4 shall have the same electrical characteristics as other Futurebus+ signal lines. Table 12-1 indicates whether they are push-pull or wire-or.

12.2.8 Extender cards

Only active extender cards may be used on the bus. Active extender cards may be used in any card slot. Bus interface circuits on any extender card shall adhere to this specification in full.

12.2.9 Capacitive loading

The maximum capacitive loading of any node's transceiver on a bused backpanel signal shall be 7 pF. For maximum performance, a goal of 5 pF should be pursued.

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13. Profile S power

This clause specifies power distribution and behavior for Profile S modules and systems. Requirements for modules and for the systems they plug into are specified in separate subclauses.

Profile S performance requirements impose constraints on module and backplane design in order to satisfy the following requirements:

— Distribute signal return and power pins to equalize current concentrations.
— Maintain power supply voltages within required tolerances for a wide range of module power requirements.
— Align power and power return pins to satisfy connector mechanical requirements.

All voltage measurements of the power rails or power distribution system shall be made relative to the nearest 0 V dc power supply return pin on the same or nearest connector on the backplane, unless otherwise specified. All measurements of signal voltages shall be made relative to the closest (signal) GND return pin for digital signals. See Figure 13-1 for a diagram of the Profile S power rails.

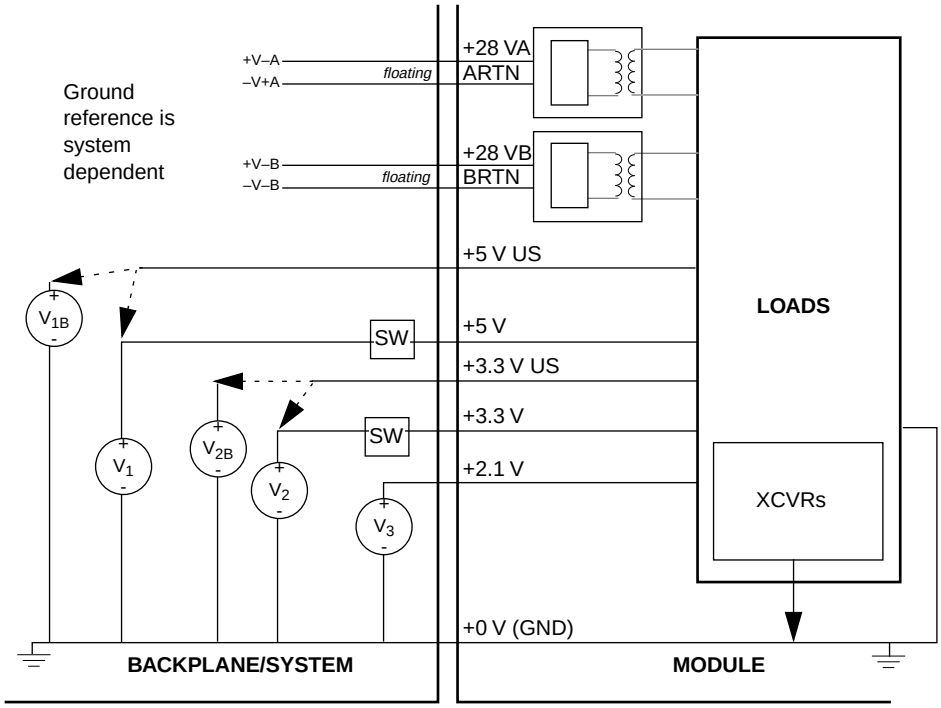

Figure 13-1—Profile S power rails

13.1 Module power

13.1.1 Power consumption limits

The current passing through any power supply pin or power return pin shall not exceed 1.0 A (averaged across all pins) for each supply voltage.

For Profile S modules, published specifications for module current demand at each supply voltage are based on an assumption that a given processor, memory, or input/output module will employ 5 V and/or 3.3 V

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components and that any given module shall not exceed 40 W of total power including the Futurebus+ interface itself (which should be less than 5 W for the bus transceiver, protocol, and control circuitry on any given module).

A Profile S module's *maximum current* at a given supply voltage is the sum of the I_{max} values for active devices plus nominal currents for passive components. *Maximum power* is the sum of the products of maximum current times the corresponding nominal voltage.

13.1.2 Module bypass capacitance and *di/dt*

Module bypass capacitance shall be sufficient to prevent operating *di/dt* from forcing any supply voltage out of regulation at the backplane connectors. Regulation tolerances are specified below in 13.2.4.

13.2 Host system power supplies

One or more different power supply types may be employed depending on configuration requirements. These could include

— *Chassis-Mounted supply.* A supply mounted adjacent to the bus that is connected to the bus via cabling.
— *Plugged-In bused supplies.* One or more supplies for the same voltage(s) may reside on the bus. Multiple sources are used for redundancy or load distribution. Adequate protection networks and load balancing circuitry shall be employed. The advantage of this method is that power supplies can be plugged in like any other board.
— *Fully distributed power conversion.* Individual dc–dc power converters are used on each board to develop the required voltages from the 28 V dc bused on the backplane.

13.2.1 Power rails

Backplane power pin assignments provide for six power rails: +V, +V RTN +5 V, +3.3 V, +2.1 V, and 0 V dc. The +5 V, +2.1 V, and +3.3 V supplies are regulated voltages and use 0 V dc for power return.

The +V supply is normal spacecraft power (28 V dc ± 6 V). It may be preregulated. It uses the +V RTN for power return.

The supply voltages specified in the connector pin assignments shall be connected to their assigned power pins on the backplane. Systems designed for high reliability using on-module regulation may choose to provide 28 V from two independent sources; if this is done the two sources shall connect to the 28 V supply pins as described in the power pinout subclause of this profile. If some form of power switching or battery backup is employed in the system, then two of each of the switchable voltage (+5 V and +3.3 V) pins shall be connected to the unswitched power as described in the power pinout subclause of this profile. Modules could use these voltages connections to power elements that had to always be active while the rest of the module could be switched off. If no power switching or battery backup is provided in a system, the backplane shall be wired to connect the switched and unswitched +5 V lines together and the switched and unswitched 3.3 V lines together. Modules shall connect to all assigned power pins as specified in 10.3.4.

If a supply voltage is not provided by a particular system power supply, the pins assigned to that voltage shall be reserved. Modules shall not connect the unswitched +5 V or +3.3 V to the switched 5 V or 3.3 V rails on the module. In addition, 0 V dc power returns and 0 V signal grounds shall be connected to backplane ground plane(s) at all connector positions.

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13.2.2 Rise time and power sequencing

The supply voltage waveform for all power supplies at turn-on shall be damped so there is no voltage overshoot greater than the maximum limit for that supply, as specified in 13.2.3. Rise time shall be less than 200 ms from 10% to 90% of the nominal voltage under all specified loading conditions.

For Profile S modules and systems the power down and power fail sequence is beyond the scope of this document.

Observation: Power fail can occur on any voltage, therefore modules must be designed to protect against situations where any of the voltages may not be present if more than one voltage source is used. For systems that are reconfigured in orbit, it is difficult to predict system current requirements for all applications. When adding or deleting modules from a preconfigured system, the current draw from the power supply will change. During power down, the collapse rate will vary from configuration to configuration. Again, Profile S modules will experience a variety of power down sequences and should be designed not to cause a failure under a variety of applications.

13.2.3 Voltage variation

Ripple will be limited to a single, continuous, sinusoidal wave with the following amplitudes:

— 3 V from 30 Hz to 500 Hz
— 1 V from 500 Hz to 150 kHz
— 0.53 V from 150 kHz to 10 MHz

These voltages are superimposed on the nominal 28 V input voltage.

Broadband signals will include both positive and negative spikes of up to 28 V superimposed on the nominal +28 V input voltage line-to-line and ±14 V spikes, referenced to chassis, applied from each line to chassis. The spikes will have a wave shape as shown in Figure 13-2, with duration of 10 μs and a rate of 15 spikes per second over a 5 min minimum interval.

The regulated voltages (2.1 V, 3.3 V, and 5.5 V, switched and unswitched) supplied to the Profile S modules must remain within 5% of the nominal value.

13.2.4 Overvoltage/Undervoltage limits

Voltage surges may be random, and both positive and negative of up to 5 V, but not exceeding the 22 to 34 V input range (28 V ± 6 V). Surges may be sustained (at the 5 V level) for greater than 100 ms, rising at a rate of at least 0.5 V/μs and falling at a rate of no more than 5.0 V/ms.

The subsystem shall survive reductions in input voltage from 30 V to 12 V in less than 10 μs, remaining at 12 V for 20 ms, then returning to 30 V, and increases in voltage from 24 V to 42 V in less than 20 μs, then returning to 24 V. The subsystem shall operate normally after the input voltage returns to a nominal 28 V.

13.2.5 Isolation

The subsystem shall be compatible with a single point ground for primary power with separate positive and return wires brought out to the power input connector. Primary input power returns to the subsystem shall be isolated from the case (chassis) and secondary power circuitry by a minimum dc resistance of 1 MΩ. The case (chassis) or mounting structure shall not be used to conduct power currents.

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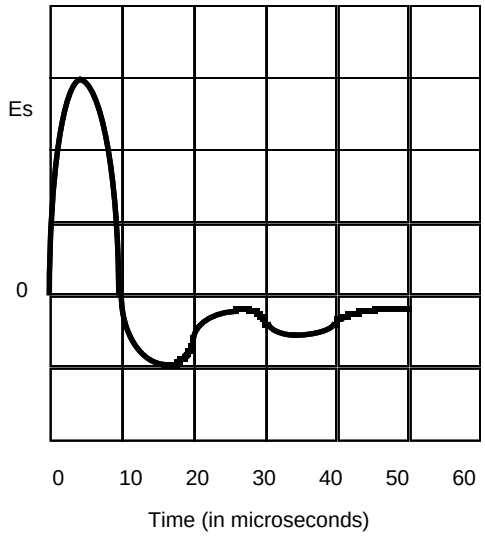

Es =±28 V line-to-line
Es = ±14 V line-to-chassis

Figure 13-2—Broadband spike waveshape

13.2.6 Power supply peak current and *di/dt* capability

Common mode currents and stray currents conducted via the path formed by the mounting structure (upon which the unit is mounted) and the primary power input and return lines, shall be limited to 5 mA peak.

The inrush current to the subsystem, after application and stabilization of bus power, when executing any commanded switching, shall not exceed 1.0 A and shall settle to nominal operating values within 100 ms.

13.2.7 Power fail

Under all operating conditions, the power supply or its agent can optionally provide a **power fail** arbitration message at least 100 μs prior to the time any dc supply goes out of regulation.

During the 100 μs power fail period, all dc outputs shall remain within the limits specified in 13.2.4. After the indication of **power fail,** all power voltages supplied to Profile S modules shall drop to below 0.5 V dc within 10 s. It is the responsibility of the module to ensure proper power-down sequencing for the module.

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14. Profile S environmental specifications

Environmental requirements impact this standard to the extent that they dictate module interfaces and the capability of modules to be used in the same rack with other modules meeting this standard.

14.1 System environmental requirements

System level environmental requirements and test procedures are beyond the scope of this standard. Moreover, meeting the module level environmental requirements imposed by this standard does not alleviate the need to meet any system and platform level environmental requirements and test procedures that may be imposed.

14.2 Module environmental requirements

Fully compliant Profile S modules shall be designed for and conform to the environmental requirements and test procedures of IEEE Std 1156.4-1997 Performance Levels I, II, III, IV, or IVa. Each module shall be clearly marked as to the highest IEEE Std 1156.4-1997 performance level it meets in each of the main categories. The operating and nonoperating environmental requirements set forth in IEEE Std 1156.4-1997 are derived from a survey of the space community. IEEE Std 1156.4-1997 references military standard MIL-STD-1540C.

IEEE Std 1156.4-1997 defines Level I as an environment primarily intended for missions with relatively benign mechanical and radiation environments. This is the least demanding of the three levels. A short-lived LEO spacecraft placed into orbit with a launcher with a “soft ride” might be a typical application. This performance level is further quantified within IEEE Std 1156.4-1997. All Profile S modules shall meet Level I requirements in all major categories.

IEEE Std 1156.4-1997 defines Level II as an environment primarily intended for missions of longer duration with more severe mechanical and radiation environments. This performance level has more demanding requirements than level I, but less demanding requirements than level III. It is expected that Profile S modules will be built that meet level II requirements in one or more major classes.

IEEE Std 1156.4-1997 defines Level III as an environment primarily intended for missions of longest duration with most severe mechanical and severe radiation environments. It is expected that Profile S modules will be built that meet level III requirements in one or more major classes.

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15. Recommended practices

The following subclauses address requirements that should be followed by each individual application consistent with the overall system design.

15.1 Thermal considerations

Modules should be designed to meet thermal and reliability criteria regardless of the direction of heat conduction on either rail.

It is strongly recommended that a thermal analysis as defined in 15.1.1 be conducted on every module, backplane, and chassis design. This is especially necessary if the amount of power consumed by a module is close to the allowed maximum of 40 W or if a specific component consumes more than 2.5 W.

15.1.1 Thermal analysis

There are many different methods of thermal analysis and any accurate method may be used. However, any method that is used should be verified in some manner through testing, other analysis, etc. At any time the module designer may be required to prove or demonstrate the validity of the analysis methods.

15.1.2 Reliability

A parts stress reliability prediction in accordance with MIL-HDBK-217F [B2][1] should be performed for each module under the worst-case mounting surface conditions given in 15.1.2.1 and the thermal junction temperatures as defined in IEEE Std 1156.4-1997. Parts stress predictions performed to some other method may be submitted for review and/or approval.

15.1.2.1 Derating

To ensure that modules are capable of operating under the thermal interface conditions and to ensure that the overall system reliability is met, the modules should meet the derating requirements of MIL-STD-1547 or contractor derating requirements based on the above documents.

15.1.3 Structural considerations

In order to ensure that the modules will survive the shock and random vibration levels of IEEE Std 1156.4-1997, a structural and dynamic analysis of each module should be performed. This analysis is especially critical for the 10 SU module design to the Level II and Level III environments because of its larger free span. If the entire 19.3 mm (0.760 in) module profile is utilized by components on the 10 SU module, a larger module pitch or special stiffeners may be required to keep adjacent modules from hitting each other when they deflect.

15.2 Power consumption

The total power consumption per board slot (side 1 and side 2) should not exceed 30 W.

15.2.1 Power control

The SP_CONTROL CSR should be implemented on processors to support Power Control.

[1]The numbers in brackets preceded by the letter B correspond to those of the bibliography in Annex A.

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15.3 Pinouts

Profile S modules should use the backplane to pass all user signals out of the module.

User I/O signal positions in connector section G of either form factor should only be used if other I/O areas are saturated.

15.4 Bus performance analysis

A Futurebus+ system may be generally represented as in Figure 15-1. Three modules are shown interconnected where each has a CPU and memory.

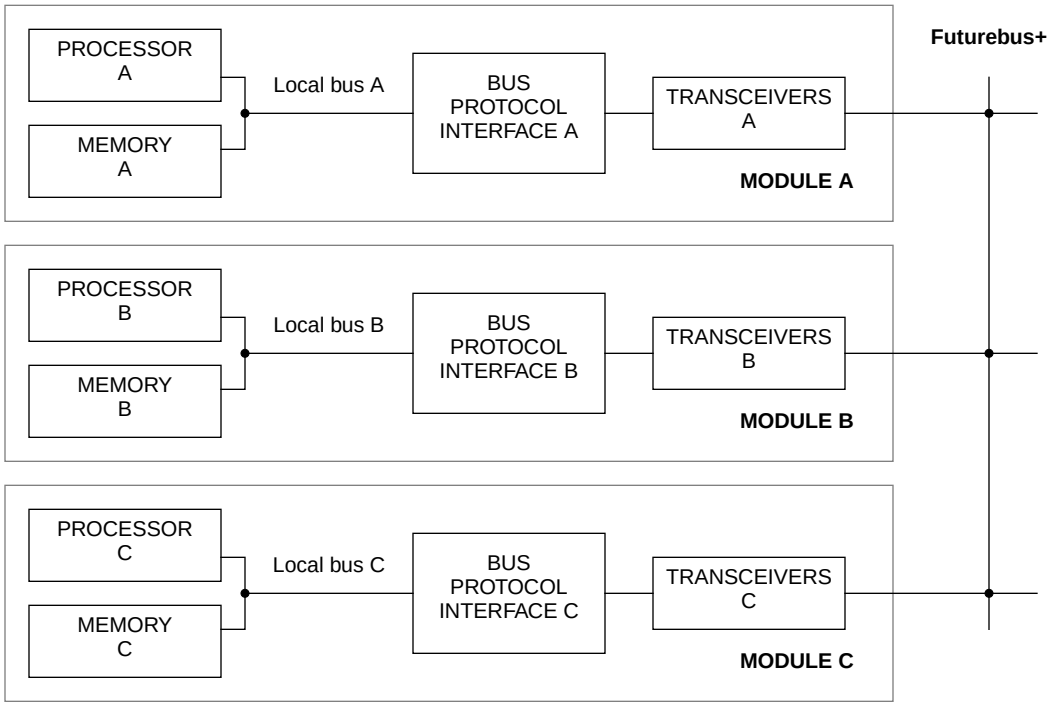

Figure 15-1—Sample Futurebus+ system

The following phases typify a Futurebus+ compelled-read transaction. Depending on the particular implementation, some of these phases may be combined but all components should be accountable in a typical read transaction. Equivalent diagrams of other transactions may be similarly constructed.

1) Processor A acquires mastership of its Local Bus (A).
2) Processor A's Transaction is accepted by Bus Protocol Interface (BPI) over Local Bus.
3) BPI A arbitrates for Futurebus+ with other modules and wins.
4) Futurebus+ Connection Phase directed by BPI A—Address and Command passed to BPI B.
5) BPI B acquires mastership of its Local Bus.
6) Data read from Memory on Local Bus B passed back to BPI B.
7) BPI B passes data to BPI A over Futurebus+ during Data Phase.
8) BPI A passes data to Processor A over Local Bus A.
9) Steps 6–8 repeated for entire transfer.
10) Local Bus B freed.
11) Futurebus+ Disconnect Phase directed by BPI A.
12) Local Bus A freed.

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In order to allow a system performance analysis to be constructed when using interoperable modules, a module provider should provide phase-related performance data for the module. Include minimum, typical, and maximum specifications for each item. Each different implemented transaction should be included. For example, in the read transaction listed above, the module provider should provide the following:

— Internal Local Transaction Time (1 and 2)
— Nonoverlapped Arbitration Time (3)
— Connection Phase Time (4)
— Data Received by Master and Stored Time (5, 6, and 8)
— Data Requested from Slave and Provided Time (5, 6, and 7)
— Master Data Phase Completed Time (10)
— Slave Data Phase Completed Time (10)
— Slave Disconnect Phase Time (11)
— Master Disconnect Phase Time (11 and 12)

The numbers in parentheses refer to the phases of the Futurebus+ read transaction given in the numbered list above.

15.5 Bandwidth considerations

The performance of any bus depends on the protocol of the bus, the architecture of the modules connected to the bus and the specific application being analyzed. In order to estimate the performance of Profile S systems, four applications were selected to demonstrate the use of different parameters for determining Futurebus+ performance. These high-bandwidth or data latency sensitive applications include multiple active bus masters, real-time computing, data producer/consumer, and shared memory multiprocessing. Each of these is discussed in the following subclauses and unique bandwidth parameters are identified.

15.5.1 Multiple active bus masters

One application of Futurebus+ is to provide a high-bandwidth backplane for systems that contain many data sources or sinks that produce a high aggregate data transfer rate. An example of a multiple active master system is a communications switch that uses memory on the backplane as the switch fabric. Data may arrive in fixed size packets as in asynchronous transfer mode networks or vary in length as in ISO/IEC 8802-3 (ANSI/IEEE 802.3) Carrier Sense Multiple Access with Collision Detection (CSMA/CD) networks. An example of a multiple bus master system is shown in Figure 15-2.

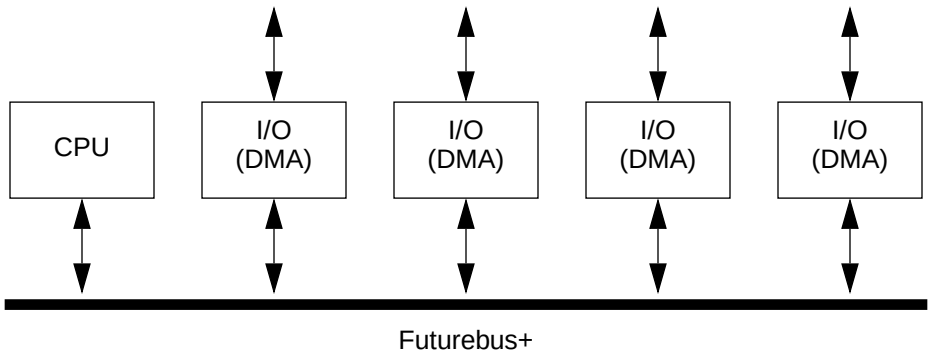

Figure 15-2—Multiple active bus masters system diagram

Memory-based switch fabric systems often employ methods to eliminate or reduce backplane data traffic. One way to eliminate some backplane data traffic is to provide local data processing and routing. In other

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cases, the use of point-to-multipoint transfers supported directly by Futurebus+ are employed to reduce or eliminate multiple copies of the same data on the bus.

These high aggregate bandwidth systems buffer data on the input/output modules and send or receive data over the Futurebus+ in bursts. In order to determine the bandwidth available for the multiple masters, burst data transfer characteristics of the modules must be known to the user. These are listed below.

— Connection time (minimum)
— Data transfer time (minimum)
— Disconnection time (minimum)

15.5.2 Real-Time control

Real-Time computing systems process and transfer time-critical data on the Futurebus+. Data is passed between processors using burst operations such a message passing. When data arrives at the destination module, an interrupt is issued. The receiving processor is interrupted when data arrives. Contributions to data latency are from the priority inversion time experienced before sending the data, the message passing rate capability of the modules involved and time required to get data into the subsystem where the processor can use it. Figure 15-3 shows an example real-time system.

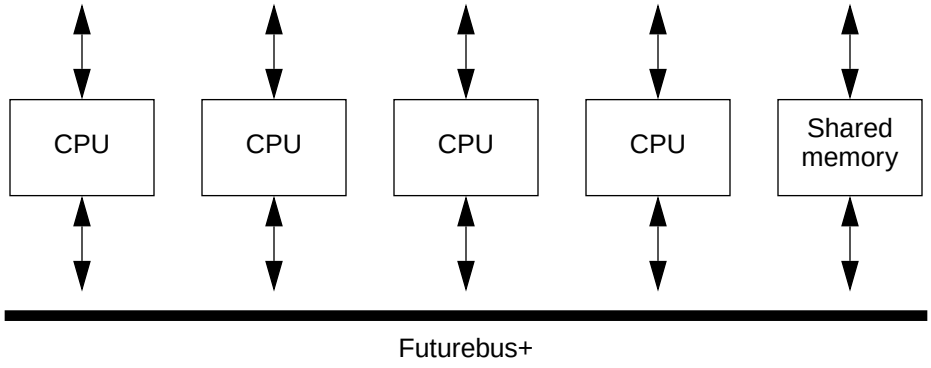

Figure 15-3—Real-Time control application

One method used to minimize the latency introduced by priority inversion on Futurebus+ is to dynamically adjust priority levels using arbitrated messages. The ability to request preemption of current bus activity is another feature to reduce priority inversion supported by Futurebus+. A third method not directly supported is the use of queueing techniques involving priority-based buffer management. The time it takes for a module to receive data and issue an interrupt is also critical.

Real-Time systems often need a distributed clock to produce an accurate system time for tagging data.

In order for a user to determine the suitability of a module for use in a real-time computing system requires access to detailed operation parameters such as those listed below.

— Preemption response time (maximum)
— Data transaction rate (minimum) or
— Message passing transfer/reception rate (peak)
— Queueing management support (software)
— Support for distributed clock synchronization

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15.5.3 Data producer/consumer

In some systems, most of the data traffic on the Futurebus+ is produced and consumed by one or a few modules. An example producer/consumer system contains a high-bandwidth video sensor input module. This differs from the multiple active bus masters example above in that one or a few modules account for nearly all the data transactions and data appears to flow in a continuous stream. Point-to-Point data transactions are common. Figure 15-4 depicts the producer/consumer system.

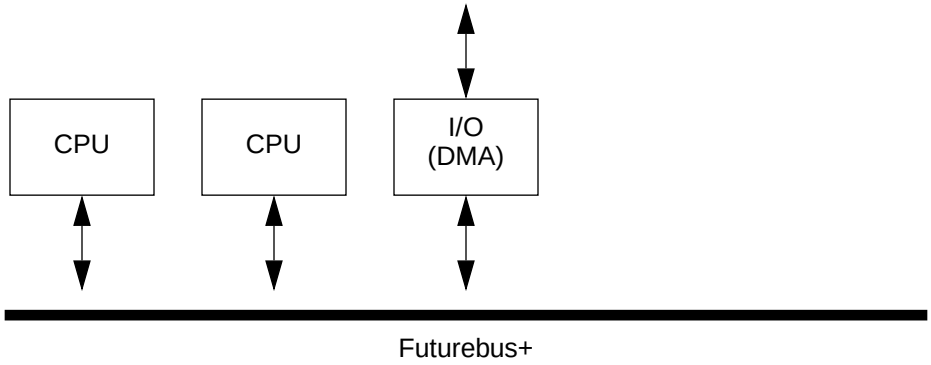

Figure 15-4—Data producer/consumer application

Measures taken to reduce data transfers on Futurebus+ involve processing on the I/O module such as lossy amplitude thresholding algorithms or more complex adaptive bit allocation techniques with discrete cosine transform coding. Important module characteristics of these systems are listed below.

— Data input rate (sustained and possibly peak)
— Data output transaction rates (sustained and possibly peak)

15.5.4 Backplane data coherence systems

Applications involving shared memory multiprocessing take advantage of the snoopy data coherence features provided by Futurebus+. Point-to-Point transactions from multiple masters is common. Figure 15-5 shows an example shared memory multiprocessing system.

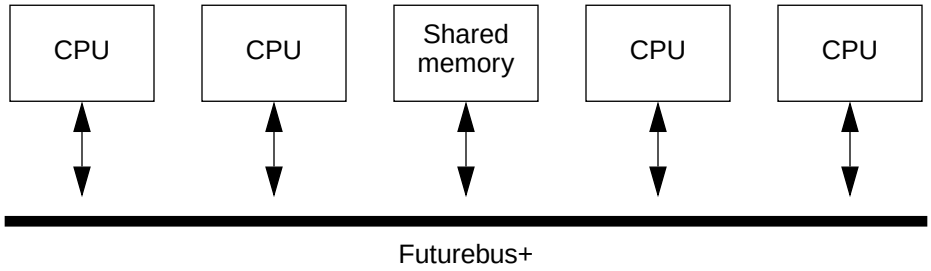

Figure 15-5—Shared memory multiprocessing system

The available backplane bandwidth may be reduced due to processing performance loss from preemption of a transaction and transaction extension on a cache miss. Cache design for reducing the performance loss due to preemption is not directly supported by Futurebus+. Transactions in shared memory multiprocessing systems on Futurebus+ are extended when the need for updating a data cache arises. In order to evaluate the available bandwidth for a shared memory system, one parameter for systems employing data coherence is given below.

— Cycle extension due to snooping (maximum)

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16. Profile S module selection criteria

16.1 Introduction

One of the goals of this document is to provide interoperable subassemblies for any configuration specified. Since the actual contents of a module are not specified, there are many details that are only known after an interoperable module is designed and built.

This subclause specifies a set of values that shall be provided by vendors of Profile S compliant modules. These parameters are applicable to all markets and applications. The goal of requiring vendors to measure/calculate and identify these values is to provide system integrators with sufficient data to enable them to judge whether the module can be successfully deployed for a specific application without requiring extensive procurement cycles.

Values that vendors are required to identify are specified in 16.2. A set of guidelines and recommendations intended to assist module developers produce these values is provided in Clause 15.

16.2 Profile S modules

The information in the following subclauses shall be provided by Profile S module vendors in their product literature.

16.2.1 Form, fit, and function

The vendor shall indicate the capabilities of the module by indicating which of the capabilities listed in Tables 4-5 through 4-9 and 9-2 through 9-6 are implemented.

The vendor shall provide a functional block diagram of the module.

The vendor shall provide an I/O listing including all reserved and user I/O signals.

16.2.2 Module power

The vendor shall state the amount of power dissipated by a module by voltage and how that power is divided between side 1 and side 2 of the module. The conditions under which the power was measured and assumptions shall be stated.

Maximum and typical current for each voltage shall be specified. This should be shown for each major frequency that the module is designed to operate at.

Module specifications shall state the maximum *di/dt* (change in module current demand) for each voltage in normal operation (other than power-up).

16.2.2.1 Mezzanine card power

For Futurebus+ modules capable of housing mezzanine cards, the vendor shall state the amount of power allocated to the mezzanine card(s).

16.2.3 Environmental

The vendor shall state the results of EMI scans and the conditions under which the tests were performed.

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Results of any thermal analysis shall be stated by the module designer.

The vendor shall state the module's expected MTTF (Mean-Time To Failure), reliability, and part junction temperature for each expected operating environment and how each is computed or determined.

A module vendor shall identify specific environmental and performance levels to which compliance has been achieved.

The vendor shall state the results of all environmental testing according to IEEE Std 1156.4-1997.

16.3 Profile S systems

A subrack shall provide a minimum coldplate interface according to IEEE Std 1156.4-1997.

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17. Alternate profile S module connector

IEEE Std 1101.7-1995 provides an alternate connector for the SEM-E Stretch form factor. This connector replaces 24 pins in the middle of the pin field with a center support and a third keying pin. Since this connector was allowed in IEEE Std 1101.7-1995 and because the connector is gaining in popularity over the standard 396-pin connector specified in other clauses of this standard, a Space Profile module may be implemented with this connector (with or without the fiber optic inserts in connector sections C and D).

17.1 Mechanical

The physical characteristics for the SEM-E Stretch module shall be in accordance with IEEE Std 1101.7-1995. Because of the high module bus I/O requirements yet a desire for a more reliable connector, the 372-pin connector version may be used. Critical requirements between the module and the subrack shall also be as outlined in IEEE Std 1101.7-1995.

17.1.1 Unoccupied slots

The system integrator is responsible for ensuring that a configuration having unoccupied slots meets the internal environmental standards specified in IEEE Std 1156.4-1997. Additionally, it is the integrator's responsibility to ensure that all applicable EMI standards are met for the applications in which the systems are intended to operate.

17.1.2 Backplane capacity

The backplane and subrack assembly shall support no more than 31 slots.

The space working group has used 14 slots as a "typical" system size and has used this number for electrical studies. Because mechanical analysis is completely system-dependent, no mechanical or thermal analyses performed by the working group should be substituted for this analysis. This analysis should be supported by product literature.

17.1.3 Injector/Elector mechanism

If insertion/extraction levers are used, they shall be retained so that they do not rattle during shock and random vibration.

17.2 Input/Output

If there are non-Futurebus+ signals passing into or out of a SEM-E Stretch module, those signals should connect through the backplane user I/O area. Connection to dual or redundant or secondary buses on the backplane is permitted for SEM-E Stretch modules.

17.3 Profile connector, power, and signal pin assignments

17.3.1 Connector naming conventions and connector assignment

Figure 17-1 shows the connector naming convention for SEM-E Stretch modules. The entire connector consists of 50 rows (1–50) and 8 columns (a–h) of pins and is built from ten segments, each 5 rows by 8 columns. For pinout reference, the connector is partitioned into six sections: C, D, E, F, G, and H. Sections C and D consist of 5 rows by 4 columns (20 pin locations) each. Sections E and F consist of 20 rows by 4 columns (80 pin locations) each. Sections G and H consist of 25 rows by 4 columns (100 pin locations) each. Signals in rows 25 and 26 of the connector are replaced with a support structure and a third keying pin.

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These connector sections are defined for both the SEM-E Stretch Dual Futurebus+ and the SEM-E Stretch Error Correcting configuration. The SEM-E Stretch Single 32-bit and SEM-E Stretch Single 64-bit Futurebus+ profiles are modifications of these two base definitions. For all implementations, sections C and D may optionally contain fiber connections. Connector section F optionally may contain one dual-redundant MIL-STD-1553 serial buses. Connector sections E and G contain the data, control, utility, and arbitration lines needed to implement a Single 32-bit Futurebus+. These sections are also used for the Futurebus+ 1 Bus in the Dual Bus Futurebus+ configuration. In the Error Correcting configuration, connector sections E and G contains the data lines and the base copy of the control, utility, and arbitration lines. Connector section F and H contain the data, control, utility, and arbitration lines needed for the Futurebus+ 2 bus in the Dual Bus configuration. In the single bus configurations, connector sections F and H contains the required data lines for the 64-bit bus and user-defined I/O lines. In the Error Correcting configuration, connector sections F and H contains the A and B copies of the control, utility, and arbitration lines, and the spare lines. Power and ground is distributed across all connector sections.

Pins are referenced by row number and column letter as shown. Pin locations 1a and 1c do not exist and are replaced by the first or alpha key. Pin locations 50b and 50d also do not exist and are replaced by the second or beta key. The third or gamma key is located in the support area in the center of the connector and uses up twenty two pin locations. The total number of pins in the connector is 372. Sides “A” and “B” of the connector are referenced as shown in Figure 17-1. Pins in each row (a–h) are alternately staggered vertically as shown in Figure 17-1.

All connector views in this section show the backplane connector pinout as seen from the front of the rack. Note that other documents may refer to a through h as rows and 1 through 50 as columns. The convention described above was chosen in order to simplify the connector figures in this document.

17.3.2 Signal pin assignments

Initial attempts were made to develop a space profile pin definition which matched the military profile. This proved impossible for the following reasons. First, the military profile requires many more power and ground connections due to the high power dissipation of the modules. Second, the military profile does not support the Error Correcting configuration or have adequate spare lines.

Work was done with the pinouts to allow easy card layout for all possible transceiver implementations (using 8-bit and 9-bit transceivers and separate protocol chips). The pinouts allow for a discrete interface where individual transceivers and separate protocol chips are used, a completely integrated interface where transceivers and protocol chips are combined in the same package, and a range of partially integrated implementations between these two extremes. Due to the limited space on SEM-E Stretch cards, a partially or completely integrated interface is recommended. Pinouts were adjusted to make sure that no different powers and grounds were next to each other either on the connector or on pins that attach to a printed wiring board from a connector.

Whenever possible, signals overlap between the SEM-E Stretch Dual Futurebus+, the SEM-E Stretch Error Correcting configuration, the SEM-E Stretch Single 32-bit Futurebus+, and the SEM-E Stretch Single 64-bit Futurebus+. Figures 17-2 through 17-5 show how the signals are distributed on the connector for the SEM-E Stretch module configurations.

User-Defined I/O signals are shown in Figure 17-2 through 17-5. These allow maximum flexibility for non-bused signals and are defined in connector sections E–H. When the optional central arbiter or MIL-STD-1553 bus is implemented, some, most or all of the user defined I/O pinouts are utilized to provide the additional signal paths required. See 17.3.3 for the definition of the Central Arbitration usage of user-defined I/O for that module.

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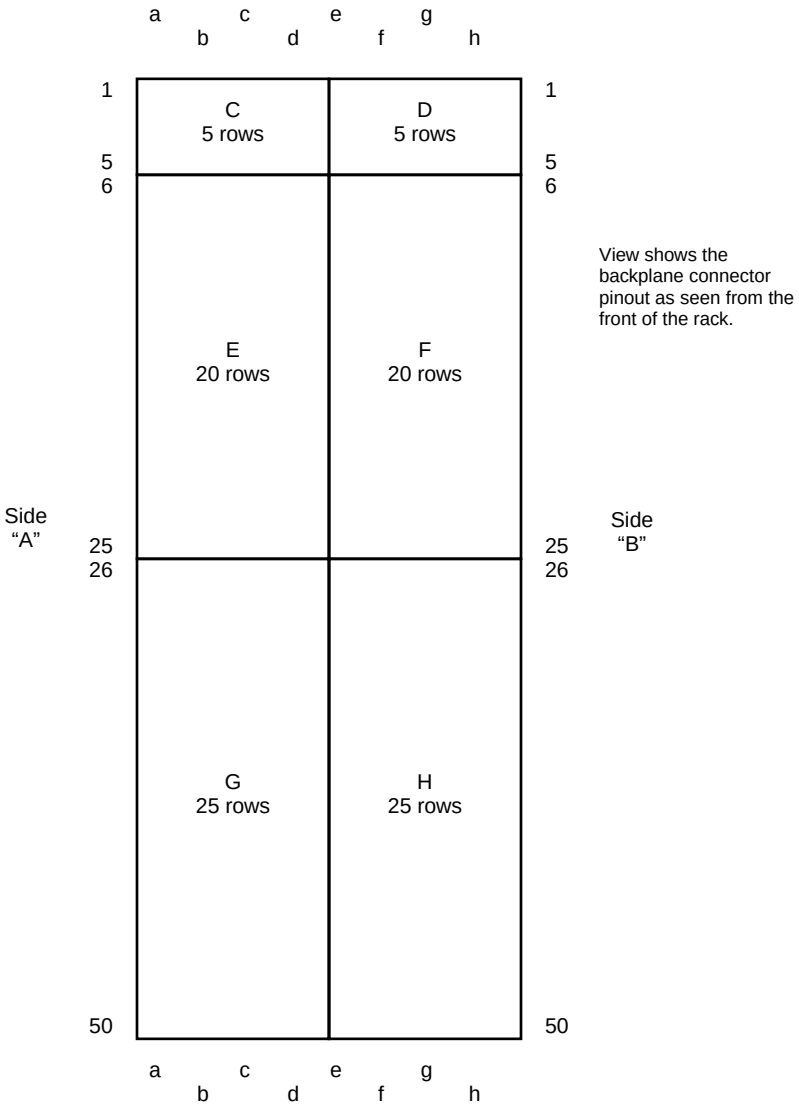

Figure 17-1—Module SEM-E Stretch connector naming conventions

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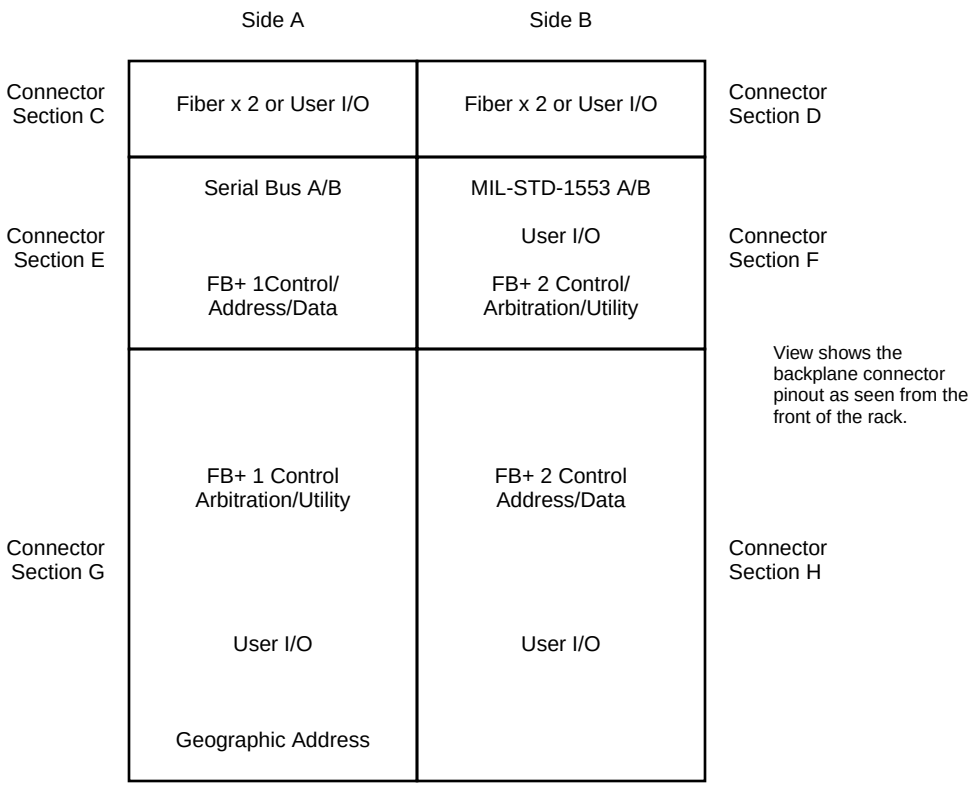

Figure 17-2—Module SEM-E Stretch connector usage (Dual Futurebus+)

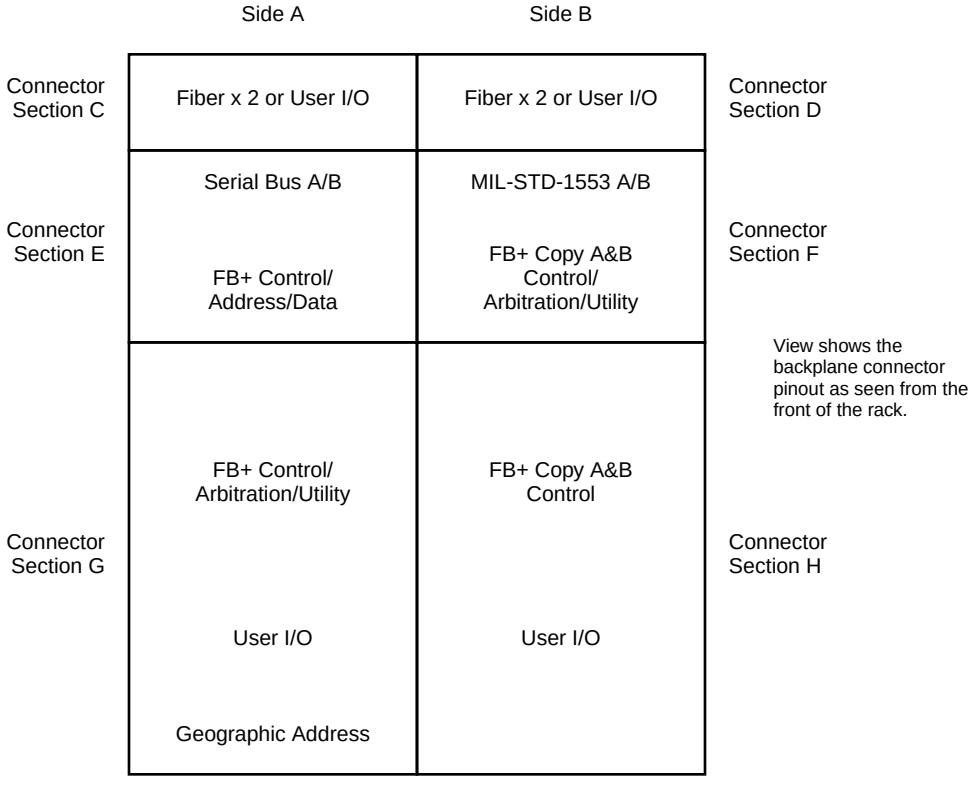

Figure 17-3—Module SEM-E Stretch connector usage (Error Correcting configuration)

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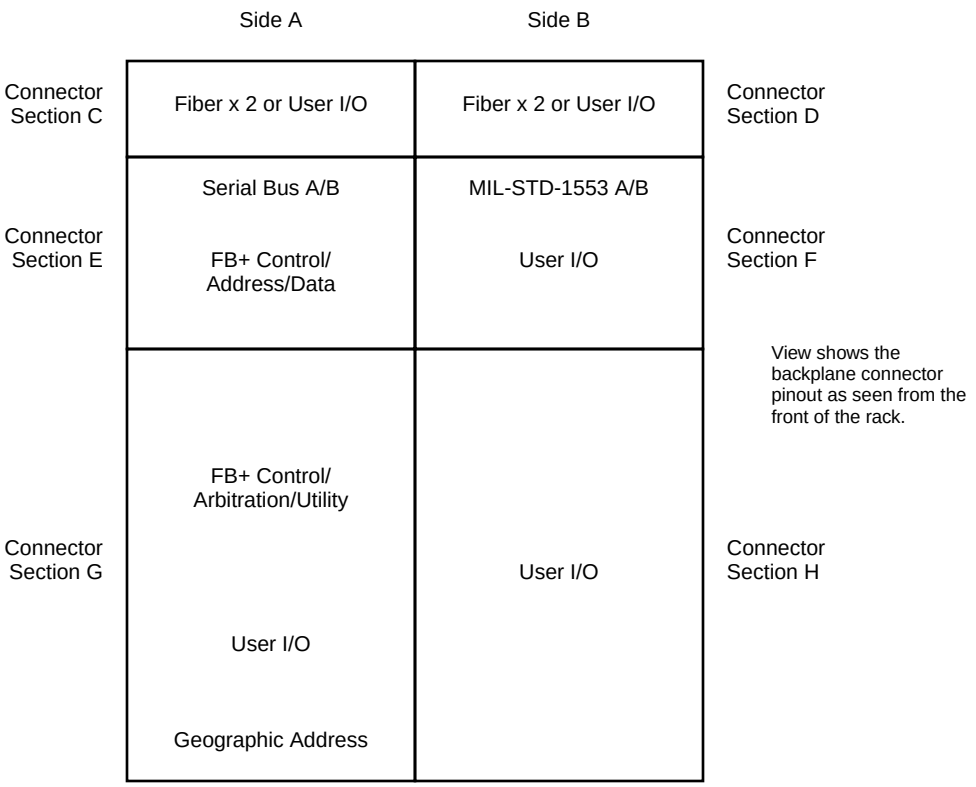

Figure 17-4—Module SEM-E Stretch connector usage (single 32-bit Futurebus+)

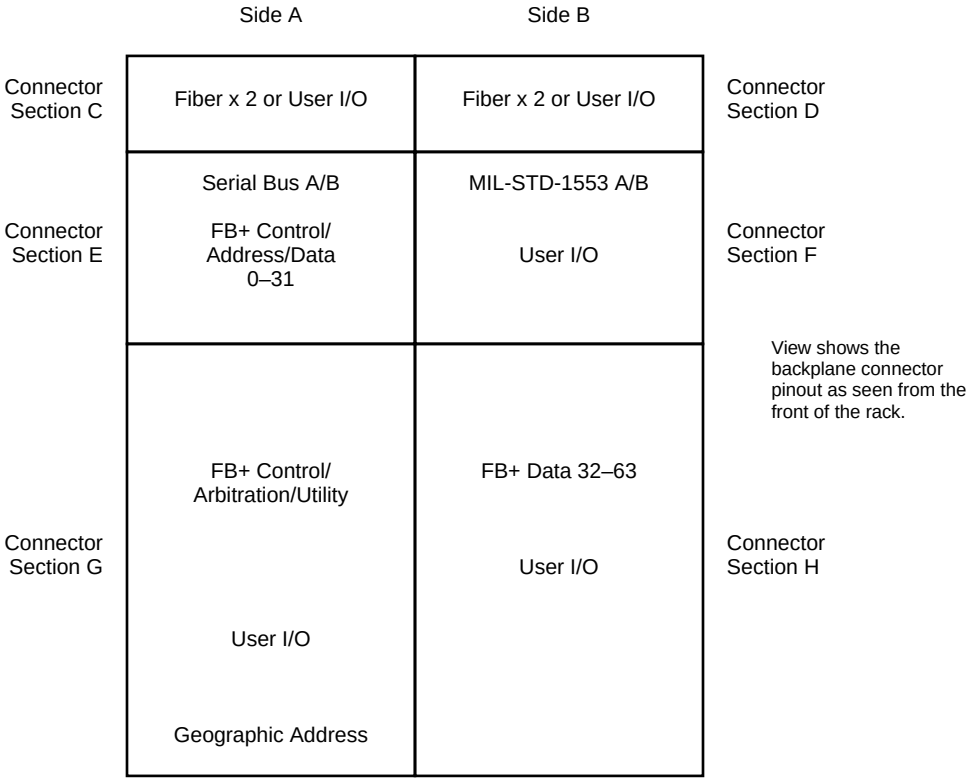

Figure 17-5—Module SEM-E Stretch connector usage (single 64-bit Futurebus+)

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17.3.2.1 Connector sections C and D

If fiber is implemented, connector sections C and D shall be used for the four fiber connections. These pins replace one segment of the connector. The connector only supports a fiber segment at one end of the connector. This resulted in the choice of sections C and D. This implies two fiber connections for each side of the card. If the fiber connections are not implemented, the original connector section may be used for user-defined I/O.

Figures 17-6 and 17-7 show the pinouts for sections C and D for all connector definitions. If used for fiber, section C shall contain a keying pin occupying two pin locations and two fiber connections. Section D shall also contain two fiber connections. If the fiber connections are not implemented, section C shall contain 15 user-defined connections, two keying location pins, one +5 V connection, and two ground connections. Similarly, section D shall contain 17 user-defined connections, one +5 V connection, and two ground connections.

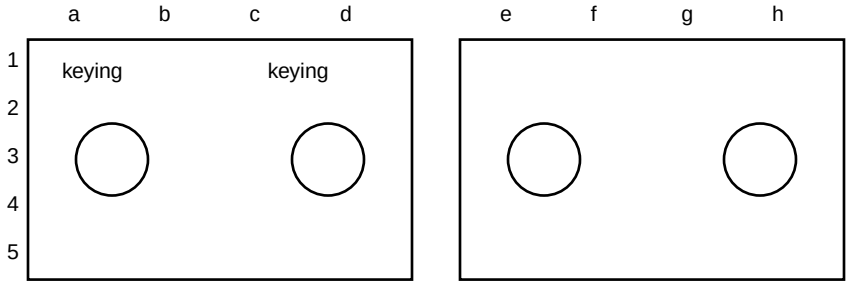

Figure 17-6—SEM-E Stretch sections C and D with fiber connections

	a	b	c	d	e	f	g	h
1	KEY	User I/O*	KEY	User I/O*	N/A	User I/O*	N/A	User I/O*
2	GND	User I/O*	User I/O*	User I/O*	GND	User I/O*	User I/O*	User I/O*
3	User I/O*	User I/O*	User I/O*	GND	User I/O*	User I/O*	User I/O*	GND
4	User I/O*	User I/O*	User I/O*	User I/O*	User I/O*	User I/O*	User I/O*	User I/O*
5	+5 V	User I/O*	User I/O*	User I/O*	+5 V	User I/O*	User I/O*	User I/O*

Figure 17-7—Pinout for SEM-E Stretch connector sections C and D without fiber

Due to the proliferation of the MIL-STD-1553B interface in the space community, connector section D contains one optional dual-redundant MIL-STD-1553B serial bus as shown in Figure 17-22. These replace the same User I/O defined in Figure 17-7. To use a specific bus with external transformers, the Bus X+ and Bus X– signals should be used. Either a direct-coupled or transformer-coupled implementation may be used. To use a specific bus on the other side of a transformer, the Bus X dc+ and Bus X dc– should be used. Only one of these are required to be used for a given bus X.

17.3.2.2 Connector sections E and G

Connector sections E and G shall contain the Futurebus+ data bits 0 to 31, associated parity bits, utility, distributed arbiter, and the control signals as well as one or both serial busses. These connector sections shall be used for Futurebus+ 1, power, ground, and Serial Buses A and B in the SEM-E Stretch Dual Futurebus+ configuration. In the Error Correcting configuration, these same bits will be used for the original Futurebus+ and both Serial Busses. The single 32-bit Futurebus+ is a subset of either the Dual Futurebus+ or the Error Correcting configuration implementations. This is possible because the same pin locations are used for common pins in both the dual Futurebus+ and the Error Correcting configuration pin assignments.

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Figure 17-8 shows the connector sections E and G pinouts for a Dual Bus Configuration. Figure 17-9 shows these pinouts for the Error Correcting configuration. Figure 17-10 shows these pinouts for a Single 32-bit or Single 64-bit configuration. Figures 17-11 through 17-13 show the corresponding User I/O pins in each configuration.

	a	b	c	d
6		1-AS*		+3.3 V
7	1-ET*	1-CA0*	1-DS*	1-RF*
8	GND	1-SLD*	1-CA1*	1-RED*
9	1-SB1*	1-AD0*	1-SB0*	+5 V
10	1-AD2*	1-AD4*	1-AD1*	1-AD3*
11	+3.3 V	1-AD7*	1-AD5*	1-AD6*
12	1-AD8*	1-AD9*	1-BP0*	GND
13	1-AD11*	1-AD13*	1-AD10*	1-AD12*
14	+5 V US	1-BP1*	1-AD14*	1-AD15*
15		1-ST0*		GND
16	1-ST2*	1-AI*	1-ST1*	1-ST3*
17	+5 V	1-CA2*	1-DI*	1-RE*
18	2-SB1*	1-AD16*	2-SB0*	GND
19	1-AD18*	1-AD20*	1-AD17*	1-AD19*
20	+28 V A	1-AD23*	1-AD21*	1-AD22*
21	1-AD24*	1-AD25*	1-BP2*	+28 V A RTN
22	1-AD27*	1-AD29*	1-AD26*	1-AD28*
23	GND	1-BP3*	1-AD30*	1-AD31*
24		N/A		+2.1 V
27		1-ST5*	N/A	1-ST4*
28	GND	1-AK*	1-ST6*	1-ST7*
29	1-TED*	1-PN	1-DK*	+28 RTN A
30	TR1*	1-CM1*	TR0*	1-CM0*
31	+28 V A	1-CM4*	1-CM2*	1-CM3*
32	1-CM6*	1-CM7*	1-CM5*	GND
33		1-PFI*	1-CP*	1-NED*
34	-15 V	1-GR*	RUN*	1-SR*
35	1-RQ0*	1-RQ1*	1-PE*	GND
36		1-AQ*		1-AR*
37	+3.3 V US	1-AC1*	1-AP*	1-AC0*
38	1-AB1*	1-AB2*	1-AB0*	GND
39	1-AB4*	1-AB6*	1-AB3*	1-AB5*
40	+5 V		1-AB7*	1-ABP*
41				+3.3 V
42				
43	GND			
44				+5 V
45				
46	+3.3 V			
47				GND
48		GA0*		
49	GND	GA3*	GA1*	GA2*
50	GA_PARITY*	N/A	GA4*	N/A

Figure 17-8—Pinout for SEM-E Stretch Dual Futurebus+ 372-pin connector sections E and G

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	a	b	c	d
6		AS*		+3.3 V
7	ET*	CA0*	DS*	TMRS0*
8	GND	TMRS1*	CA1*	
9	1-SB1*	AD0*	1-SB0*	+5 V
10	AD2*	AD4*	AD1*	AD3*
11	+3.3 V	AD7*	AD5*	AD6*
12	AD8*	AD9*	BC0*	GND
13	AD11*	AD13*	AD10*	AD12*
14	+5 V US	BC1*	AD14*	AD15*
15		ST0*		GND
16	ST2*	AI*	ST1*	ST3*
17	+5 V	CA2*	DI*	RE*
18	2-SB1*	AD16*	2-SB0*	GND
19	AD18*	AD20*	AD17*	AD19*
20	+28 V A	AD23*	AD21*	AD22*
21	AD24*	AD25*	BC2*	+28 V A RTN
22	AD27*	AD29*	AD26*	AD28*
23	GND	BC3*	AD30*	AD31*
24		N/A		+2.1 V
27		ST5*	N/A	ST4*
28	GND	AK*	ST6*	ST7*
29	TMRS2*	PN	DK*	+28 RTN A
30	TR1*	CM1*	TR0*	CM0*
31	+28 V A	CM4*	CM2*	CM3*
32	CM6*	CM7*	CM5*	GND
33		PFI*		NED*
34	-15 V	GR*	RUN*	SR*
35	RQ0*	RQ1*	PE*	GND
36	5	1-AQ*		AR*
37	+3.3 V US	AC1*	AP*	AC0*
38	AB1*	AB2*	AB0*	GND
39	AB4*	AB6*	AB3*	AB5*
40	+5 V		AB7*	ABC0*
41				+3.3 V
42				
43	GND			
44				+5 V
45				
46	+3.3 V			
47				GND
48		GA0*		
49	GND	GA3*	GA1*	GA2*
50	GA_PARITY*	N/A	GA4*	N/A

Figure 17-9—Pinout for SEM-E Stretch EC Futurebus+ 372-pin connector sections E and G

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	a	b	c	d
6		AS*		+3.3 V
7	ET*	CA0*	DS*	RF*
8	GND	SLD*	CA1*	RED*
9	1-SB1*	AD0*	1-SB0*	+5 V
10	AD2*	AD4*	AD1*	AD3*
11	+3.3 V	AD7*	AD5*	AD6*
12	AD8*	AD9*	BP0*	GND
13	AD11*	AD13*	AD10*	AD12*
14	+5 V US	BP1*	AD14*	AD15*
15		ST0*		GND
16	ST2*	AI*	ST1*	ST3*
17	+5 V	CA2*	DI*	RE*
18		AD16*		GND
19	AD18*	AD20*	AD17*	AD19*
20	+28 V A	AD23*	AD21*	AD22*
21	AD24*	AD25*	BP2*	+28 V A RTN
22	AD27*	AD29*	AD26*	AD28*
23	GND	BP3*	AD30*	AD31*
24		N/A		+2.1 V
27		ST5*	N/A	ST4*
28	GND	AK*	ST6*	ST7*
29	TED*	PN	DK*	+28 RTN A
30	TR1*	CM1*	TR0*	CM0*
31	+28 V A	CM4*	CM2*	CM3*
32	CM6*	CM7*	CM5*	GND
33		PFI*	CP*	NED*
34	-15 V	GR*	RUN*	SR*
35	RQ0*	RQ1*	PE*	GND
36		1-AQ*		AR*
37	+3.3 V US	AC1*	AP*	AC0*
38	AB1*	AB2*	AB0*	GND
39	AB4*	AB6*	AB3*	AB5*
40	+5 V		AB7*	ABP*
41				+3.3 V
42				
43	GND			
44				+5 V
45				
46	+3.3 V			
47				GND
48		GA0*		
49	GND	GA3*	GA1*	GA2*
50	GA_PARITY*	N/A	GA4*	N/A

Figure 17-10—Pinout for SEM-E Stretch Single Futurebus+ 372-pin connector sections E and G

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	a	b	c	d
6	User I/O*		User I/O*	
7				
8				
9				
10				
11				
12				
13				
14				
15	User I/O*		User I/O*	
16				
17				
18				
19				
20				
21				
22				
23				
24	User I/O*		User I/O*	
27	User I/O*			
28				
29				
30				
31				
32				
33	User I/O*			
34				
35				
36	User I/O*		User I/O*	
37				
38				
39				
40		User I/O*		
41	User I/O*	User I/O*	User I/O*	
42	User I/O*	User I/O*	User I/O*	User I/O*
43		User I/O*	User I/O*	User I/O*
44	User I/O*	User I/O*	User I/O*	
45	User I/O*	User I/O*	User I/O*	User I/O*
46		User I/O*	User I/O*	User I/O*
47	User I/O*	User I/O*	User I/O*	
48	User I/O*		User I/O*	User I/O*
49				
50				

Figure 17-11—User-Definable I/O for SEM-E Stretch Dual Futurebus+ 372-pin connector sections E and G

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	a	b	c	d
6	User I/O*		User I/O*	
7				
8				User I/O*
9				
10				
11				
12				
13				
14				
15	User I/O*		User I/O*	
16				
17				
18				
19				
20				
21				
22				
23				
24	User I/O*		User I/O*	
27	User I/O*			
28				
29				
30				
31				
32				
33	User I/O*		User I/O*	
34				
35				
36	User I/O*		User I/O*	
37				
38				
39				
40		User I/O*		
41	User I/O*	User I/O*	User I/O*	
42	User I/O*	User I/O*	User I/O*	User I/O*
43		User I/O*	User I/O*	User I/O*
44	User I/O*	User I/O*	User I/O*	
45	User I/O*	User I/O*	User I/O*	User I/O*
46		User I/O*	User I/O*	User I/O*
47	User I/O*	User I/O*	User I/O*	
48	User I/O*		User I/O*	User I/O*
49				
50				

Figure 17-12—User-Definable I/O for SEM-E Stretch Error Correcting Futurebus+ 372-pin connector sections E and G

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	a	b	c	d
6	User I/O*		User I/O*	
7				
8				
9				
10				
11				
12				
13				
14				
15	User I/O*		User I/O*	
16				
17				
18	User I/O*		User I/O*	
19				
20				
21				
22				
23				
24	User I/O*		User I/O*	
27	User I/O*			
28				
29				
30				
31				
32				
33	User I/O*			
34				
35				
36	User I/O*		User I/O*	
37				
38				
39				
40		User I/O*		
41	User I/O*	User I/O*	User I/O*	
42	User I/O*	User I/O*	User I/O*	User I/O*
43		User I/O*	User I/O*	User I/O*
44	User I/O*	User I/O*	User I/O*	
45	User I/O*	User I/O*	User I/O*	User I/O*
46		User I/O*	User I/O*	User I/O*
47	User I/O*	User I/O*	User I/O*	
48	User I/O*		User I/O*	User I/O*
49				
50				

Figure 17-13—User-Definable I/O for SEM-E Stretch Futurebus+ 372-pin connector sections E and G

17.3.2.3 Connector sections F and H

Connector sections F and H shall contain data, control, utility, and arbitration lines for the Dual Bus, Error Correcting, and Single 64-bit Futurebus+ configurations. In the Dual Bus configuration, section H shall contain the entire Futurebus+ 2. In the Error Correcting configuration, section H shall contain the A and B cop-

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ies of the control, utility, and arbitration lines and the spare lines. In the Single 64-bit configuration, section H shall contain the address and data lines corresponding to **AD[63..32]*** as well as the Bus Parity lines **BP[4..7]***. No signals shall be reserved in the Single 32-bit configuration. All positions not reserved for signals in a particular configuration are available as User I/O signals.

Figure 17-14 shows the connector sections F and H pinouts for a Dual Bus Configuration. Figure 17-15 shows these pinouts for the Error Correcting configuration. Figure 17-16 shows these pinouts for a Single 64-bit configuration. Figure 17-17 shows these pinouts for a Single 32-bit configuration. Figures 17-18 through 17-21 show the corresponding User I/O pins in each configuration.

Connector sections F and H shall also be used for central arbitration signals, distributed arbitration signals, power, and ground. Modules shall support central arbitration, but distributed arbitration is optional. If distributed arbitration is not implemented, the pins may be used for user-defined I/O. All SEM-E Stretch configurations provide at least one set of all central and distributed arbitration signals for each bus implemented.

For the Dual Futurebus+ and the Error Correcting configuration, several of the system control lines are duplicated to provide fault tolerance. Details of this feature are given in Table 17-1. The remaining area may be used for any local interconnects or user-defined I/O. As a minimum, connector section H shall contain the power pattern specified in Figure 17-26. If not used, these pins shall be reserved. The user may also define additional power and ground pins, if a unique keying is assigned to that configuration. Note that all signals in sections F and H (except **PN** and the sparing pins) are active low.

Table 17-1—Occurrence of space profile system control lines

Signal	32/64 Single Futurebus+	Dual Futurebus+	Error Correcting configuration
Utility Spares **UPSP*, UWSP**	0	0	2
Nuclear Event Detect **NED***	1	2	3
Power Failure Imminent **PFI***	1	2	3
Power Normal **PN**	1	2	3
Reset **RE***	1	2	3
Duplicate Reset **RED***	1	2	0
Reset Spare **RES***	0	0	1
Run **RUN***	1	1	1
Serial Bus 0 **SB0***	1	2	2
Serial Bus 1 **SB1***	1	2	2
Trigger 0 Start and Stop **TR0***	1	1	1
Trigger 1 Start and Stop **TR1***	1	1	1
System Reset **SR***	1	2	3

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The 64-bit Futurebus+ is a modification of the Dual Futurebus+ where the second Futurebus+ pin definition is renamed to define address/data bits 32 through 63 and parity bits 4 through 7. The second set of control signals should be deleted. Note that a Dual Bus backplane may have Dual Bus modules and Single 32-bit modules both present concurrently. Single 64-bit modules may be plugged into a Dual Bus backplane if all other modules on the backplane are also Single 64-bit modules. Also note that an Error Correcting configuration backplane may have Error Correcting configuration modules and Single 32-bit modules both present concurrently, but the ECC and TMR on all Error Correcting configuration modules must be disabled. Single 64-bit backplanes may have Single 64-bit modules and Single 32-bit modules both present concurrently.

The SEM-E Stretch Dual Bus module shall provide pins for two copies of all central and distributed arbitration signals. The Error Correcting configuration module shall provide pins for three copies of the central arbitration request lines. Only one grant line shall be provided, however, due to coding on the grant line. The distributed arbitration lines are covered by ECC and TMR as described in the fault tolerance section of this document. The Single 32-bit and Single 64-bit configurations shall provide one set of all central and distributed arbitration signals. All implementations shall provide two +28 V input pins and two +28 V return pins for distributed power.

Table 17-2 shows how the various fault tolerant configurations are overlaid in connector section H. The empty column and row in Table 17-2 show why Single 32-bit modules can operate in backplanes designed for other configurations. This is because the Single 32-bit configuration does not use section H for any of its signals, therefore it does not interfere with them. This allows other modules to use section H as if the Single 32-bit module were not present.

Table 17-2—Table 17-2ÑSEM-E Stretch overlays (section H)

Futurebus+ Signals	Dual	Error Correcting	Single 32-bit	Single 64-bit
Control:Copy2,A	X	X		
Control:CopyB		X		
AD[31:0]*,FB+1				
AD[31:0]*,FB+2	X	Spares		AD[63:32]*

Table 17-3 shows the combinations possible SEM-E Stretch modules and backplanes containing the same optional features. The size of the backplane is the size of the largest possible configuration (64-bit for the Single Futurebus+, 32-bit (2) for the Dual Futurebus+, and 32-bit for the Error Correcting configuration). “No” is used in Table 17-3 to indicate where full configuration connection cannot be achieved physically. In all cases, a single 32-bit Futurebus+ could work as a degraded mode of any of the modules in any of the backplanes, but this is not recommended for final product; such use is envisioned only in laboratory or prototype environments when existing assets are being utilized in a less than optimum manner. Keying is used to prevent invalid combinations in the final product; however, a non-keyed backpanel used for rapid prototyping or other non-flight demonstrations is envisioned to allow the combinations shown in Table 17-3.

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Table 17-3—SEM-E Stretch backplane/module combinations

		MODULE (32-bit/64-bit)		
		Single Futurebus+	**Dual Futurebus+**	**Error Correcting configuration**
BACKPLANE	**Single Futurebus+**	Yes/Yes	No/NA	No/NA
	Dual Futurebus+	Yes/Yes[a]	Yes/NA	No/NA
	Error Correcting configuration	Yes/No	No/NA	Yes/NA

[a] This configuration is possible if the only type of module present is a Single 64-bit Futurebus+.

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	e	f	g	h
6				+3.3 V
7				
8	GND			
9				+5 V
10		2-ABP*		
11	+3.3 V	2-AB5*	2-AB7*	2-AB6*
12	2-AB3*	2-AB2*	2-AB4*	GND
13	2-AB0*	2-AC0*	2-AB1*	2-AC1*
14	+5 V US	2-AR*	2-AP*	2-AQ*
15		2-RQ1*		GND
16	2-PE*	2-SR*	2-RQ0*	2-GR*
17	+3.3 V	2-NED*		2-PFI*
18	2-CP*	2-CM7*		GND
19	2-CM5*	2-CM3*	2-CM6*	2-CM4*
20	+28 V B	2-CM0*	2-CM2*	2-CM1*
21		2-PN		+28 V B RTN
22	2-DK*	2-ST7*	2-TED*	2-AK*
23	GND	2-ST4*	2-ST6*	2-ST5*
24		N/A		+2.1 V
27		2-AD31*	N/A	2-BP3*
28	GND	2-AD28*	2-AD30*	2-AD29*
29	2-AD26*	2-AD25*	2-AD27*	+28 RTN B
30	2-BP2*	2-AD22*	2-AD24*	2-AD23*
31	+28 V B	2-AD19*	2-AD21*	2-AD20*
32	2-AD17*	2-AD16*	2-AD18*	GND
33		2-RE*		2-CA2*
34	-15 V	2-ST3*	2-DI*	2-AI*
35	2-ST2*	2-ST0*	2-ST1*	GND
36		2-AD15*		2-BP1*
37	+3.3 V US	2-AD12*	2-AD14*	2-AD13*
38	2-AD10*	2-AD9*	2-AD11*	GND
39	2-BP0*	2-AD6*	2-AD8*	2-AD7*
40	+5 V	2-AD3*	2-AD5*	2-AD4*
41	2-AD1*	2-AD0*	2-AD2*	+3.3 V
42		2-RED*		2-SLD*
43	GND	2-RF*	2-CA1*	2-CA0*
44	2-DS*	2-AS*	2-ET*	+5 V
45				
46	+3.3 V			
47				GND
48				
49	GND			
50		N/A		N/A

Figure 17-14—Pinout for SEM-E Stretch Dual Futurebus+ 372-pin connector sections F and H

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	e	f	g	h
6				+3.3 V
7				
8	GND			
9				+5 V
10		AIA*		
11	+3.3 V	AKA*	ASA*	ETA*
12	DIA*	DKA*	DSA*	GND
13	CAA0*	CAA1*	CAA2*	CC0*
14	+5 V US	CC1*	CC2*	CC3*
15		CC4*		GND
16	CMS0*	CMS1*	STA0*	STA1*
17	+3.3 V	STA2*		STA3*
18	STA4*	STA5*		GND
19	STA6*	STA7*	ADS2*	ADS1*
20	+28 V B	ADS0*	ADS4*	BCS0*
21		ADS3*		+28 V B RTN
22	ADS6*	ADS5*	ADS7*	AIB*
23	GND	AKB*	ASB*	ETB*
24		N/A		+2.1 V
27		DIB*	N/A	DKB*
28	GND	DSB*	CAB0*	CAB1*
29	CAB2*	STB0*	STB1*	+28 RTN B
30	STB2*	STB3*	STB4*	STB5*
31	+28 V B	STB6*	STB7*	TMRS3*
32	TMRS4*	REA*	UWSP	GND
33		BCS1*		UTSP*
34	-15 V	PFIB*	NEDA*	PFIA*
35	PNB	SRB*	PNA	GND
36		SRA*		NEDB*
37	+3.3 V US	REB*	RES*	ARA*
38	AQA*	APA*	ACA0*	GND
39	ACA1*	ABC1*	ABC2*	ABC3*
40	+5 V	ABC4*	ABS0*	ABS1*
41	GCP*	GC0*	GC1*	+3.3 V
42		RQA0*		RQA1*
43	GND	GC2*	PEA*	GC3*
44	GC4*	GC5*	GCS*	+5 V
45	GRS*	ARBS*	PEB*	RQB1*
46	+3.3 V	RQB0*	ACB1*	ACB0*
47	APB*	AQB*	ARB*	GND
48				
49	GND			
50		N/A		N/A

Figure 17-15—Pinout for SEM-E Stretch Error Correcting Futurebus+ 372-pin connector sections F and H

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	e	f	g	h
6				+3.3 V
7				
8	GND			
9				+5 V
10				
11	+3.3 V			
12				GND
13				
14	+5 V US			
15				GND
16				
17	+3.3 V			
18				GND
19				
20	+28 V B			
21				+28 V B RTN
22				
23	GND			
24		N/A		+2.1 V
27		AD63*	N/A	BP7*
28	GND	AD60*	AD62*	AD61*
29	AD58*	AD57*	AD59*	+28 RTN B
30	BP6*	AD54*	AD56*	AD55*
31	+28 V B	AD51*	AD53*	AD52*
32	AD49*	AD48*	AD50*	GND
33				
34	-15 V			
35				GND
36		AD47*		BP5*
37	+3.3 V US	AD44*	AD46*	AD45*
38	AD42*	AD41*	AD43*	GND
39	BP4*	AD38*	AD40*	AD39*
40	+5 V	AD35*	AD37*	AD36*
41	AD33*	AD32*	AD34*	+3.3 V
42				
43	GND			
44				+5 V
45				
46	+3.3 V			
47				GND
48				
49	GND			
50		N/A		N/A

Figure 17-16—Pinout for SEM-E Stretch 64-bit Futurebus+ 372-pin connector sections F and H

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	e	f	g	h
6				+3.3 V
7				
8	GND			
9				+5 V
10				
11	+3.3 V			
12				GND
13				
14	+5 V US			
15				GND
16				
17	+3.3 V			
18				GND
19				
20	+28 V B			
21				+28 V B RTN
22				
23	GND			
24		N/A		+2.1 V
27			N/A	
28	GND			
29				+28 RTN B
30				
31	+28 V B			
				GND
33				
34	-15 V			
35				GND
36				
37	+3.3 V US			
38				GND
39				
40	+5 V			
41				+3.3 V
42				
43	GND			
44				+5 V
45				
46	+3.3 V			
47				GND
48				
49	GND			
50		N/A		N/A

Figure 17-17—Pinout for SEM-E Stretch 32-bit Futurebus+ 372-pin connector sections F and H

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	e	f	g	h
6	User I/O*	User I/O*	User I/O*	+3.3 V
7	User I/O*	User I/O*	User I/O*	User I/O*
8	GND	User I/O*	User I/O*	User I/O*
9	User I/O*	User I/O*	User I/O*	+5 V
10	User I/O*		User I/O*	User I/O*
11	+3.3 V			
12				GND
13				
14	+5 V US			
15	User I/O*		User I/O*	GND
16				
17	+3.3 V		User I/O*	
18			User I/O*	GND
19				
20	+28 V B			
21	User I/O*		User I/O*	+28 V B RTN
22				
23	GND			
24	User I/O*	N/A	User I/O*	+2.1 V
27	User I/O*		N/A	
28	GND			
29				+28 RTN B
30				
31	+28 V B			
32				GND
33	User I/O*		User I/O*	
34	-15 V			
35				GND
36	User I/O*		User I/O*	
37	+3.3 V US			
38				GND
39				
40	+5 V			
41				+3.3 V
42	User I/O*		User I/O*	
43	GND			
44				+5 V
45	User I/O*	User I/O*	User I/O*	User I/O*
46	+3.3 V	User I/O*	User I/O*	User I/O*
47	User I/O*	User I/O*	User I/O*	GND
48	User I/O*	User I/O*	User I/O*	User I/O*
49	GND	User I/O*	User I/O*	User I/O*
50	User I/O*	N/A	User I/O*	N/A

Figure 17-18—User I/O for SEM-E Stretch Dual Futurebus+ 372-pin connector sections F and H

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	e	f	g	h
6	User I/O*	User I/O*	User I/O*	+3.3 V
7	User I/O*	User I/O*	User I/O*	User I/O*
8	GND	User I/O*	User I/O*	User I/O*
9	User I/O*	User I/O*	User I/O*	+5 V
10	User I/O*		User I/O*	User I/O*
11	+3.3 V			
12				GND
13				
14	+5 V US			
15	User I/O*		User I/O*	GND
16				
17	+3.3 V		User I/O*	
18			User I/O*	GND
19				
20	+28 V B			
21	User I/O*		User I/O*	+28 V B RTN
22				
23	GND			
24	User I/O*	N/A	User I/O*	+2.1 V
27	User I/O*		N/A	
28	GND			
29				+28 RTN B
30				
31	+28 V B			
32				GND
33				
34	-15 V			
35				GND
36	User I/O*		User I/O*	
37	+3.3 V US			
38				GND
39				
40	+5 V			
41				+3.3 V
42	User I/O*		User I/O*	
43	GND			
44				+5 V
45				
46	+3.3 V			
47				GND
48	User I/O*	User I/O*	User I/O*	User I/O*
49	GND	User I/O*	User I/O*	User I/O*
50	User I/O*	N/A	User I/O*	N/A

Figure 17-19—User I/O for SEM-E Stretch EC Futurebus+ 372-pin connector sections F and H

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	e	f	g	h
6	User I/O*	User I/O*	User I/O*	+3.3 V
7	User I/O*	User I/O*	User I/O*	User I/O*
8	GND	User I/O*	User I/O*	User I/O*
9	User I/O*	User I/O*	User I/O*	+5 V
10	User I/O*	User I/O*	User I/O*	User I/O*
11	+3.3 V	User I/O*	User I/O*	User I/O*
12	User I/O*	User I/O*	User I/O*	GND
13	User I/O*	User I/O*	User I/O*	User I/O*
14	+5 V US	User I/O*	User I/O*	User I/O*
15	User I/O*	User I/O*	User I/O*	GND
16	User I/O*	User I/O*	User I/O*	User I/O*
17	+3.3 V	User I/O*	User I/O*	User I/O*
18	User I/O*	User I/O*	User I/O*	GND
19	User I/O*	User I/O*	User I/O*	User I/O*
20	+28 V B	User I/O*	User I/O*	User I/O*
21	User I/O*	User I/O*	User I/O*	+28 V B RTN
22	User I/O*	User I/O*	User I/O*	User I/O*
23	GND	User I/O*	User I/O*	User I/O*
24	User I/O*	N/A	User I/O*	+2.1 V
27	User I/O*		N/A	
28	GND			
29				+28 RTN B
30				
31	+28 V B			
32				GND
33	User I/O*	User I/O*	User I/O*	User I/O*
34	-15 V	User I/O*	User I/O*	User I/O*
35	User I/O*	User I/O*	User I/O*	GND
36	User I/O*		User I/O*	
37	+3.3 V US			
38				GND
39				
40	+5 V			
41				+3.3 V
42	User I/O*	User I/O*	User I/O*	User I/O*
43	GND	User I/O*	User I/O*	User I/O*
44	User I/O*	User I/O*	User I/O*	+5 V
45	User I/O*	User I/O*	User I/O*	User I/O*
46	+3.3 V	User I/O*	User I/O*	User I/O*
47	User I/O*	User I/O*	User I/O*	GND
48	User I/O*	User I/O*	User I/O*	User I/O*
49	GND	User I/O*	User I/O*	User I/O*
50	User I/O*	N/A	User I/O*	N/A

Figure 17-20—User I/O for SEM-E Stretch 64-bit Futurebus+ 372-pin connector sections F and H

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	e	f	g	h
6	User I/O*	User I/O*	User I/O*	+3.3 V
7	User I/O*	User I/O*	User I/O*	User I/O*
8	GND	User I/O*	User I/O*	User I/O*
9	User I/O*	User I/O*	User I/O*	+5 V
10	User I/O*	User I/O*	User I/O*	User I/O*
11	+3.3 V	User I/O*	User I/O*	User I/O*
12	User I/O*	User I/O*	User I/O*	GND
13	User I/O*	User I/O*	User I/O*	User I/O*
14	+5 V US	User I/O*	User I/O*	User I/O*
15	User I/O*	User I/O*	User I/O*	GND
16	User I/O*	User I/O*	User I/O*	User I/O*
17	+3.3 V	User I/O*	User I/O*	User I/O*
18	User I/O*	User I/O*	User I/O*	GND
19	User I/O*	User I/O*	User I/O*	User I/O*
20	+28 V B	User I/O*	User I/O*	User I/O*
21	User I/O*	User I/O*	User I/O*	+28 V B RTN
22	User I/O*	User I/O*	User I/O*	User I/O*
23	GND	User I/O*	User I/O*	User I/O*
24	User I/O*	N/A	User I/O*	+2.1 V
27	User I/O*	User I/O*	N/A	User I/O*
28	GND	User I/O*	User I/O*	User I/O*
29	User I/O*	User I/O*	User I/O*	+28 RTN B
30	User I/O*	User I/O*	User I/O*	User I/O*
31	+28 V B	User I/O*	User I/O*	User I/O*
	User I/O*	User I/O*	User I/O*	GND
33	User I/O*	User I/O*	User I/O*	User I/O*
34	-15 V	User I/O*	User I/O*	User I/O*
35	User I/O*	User I/O*	User I/O*	GND
36	User I/O*	User I/O*	User I/O*	User I/O*
37	+3.3 V US	User I/O*	User I/O*	User I/O*
38	User I/O*	User I/O*	User I/O*	GND
39	User I/O*	User I/O*	User I/O*	User I/O*
40	+5 V	User I/O*	User I/O*	User I/O*
41	User I/O*	User I/O*	User I/O*	+3.3 V
42	User I/O*	User I/O*	User I/O*	User I/O*
43	GND	User I/O*	User I/O*	User I/O*
44	User I/O*	User I/O*	User I/O*	+5 V
45	User I/O*	User I/O*	User I/O*	User I/O*
46	+3.3 V	User I/O*	User I/O*	User I/O*
47	User I/O*	User I/O*	User I/O*	GND
48	User I/O*	User I/O*	User I/O*	User I/O*
49	GND	User I/O*	User I/O*	User I/O*
50	User I/O*	N/A	User I/O*	N/A

Figure 17-21—User I/O for SEM-E Stretch 32-bit Futurebus+ 372-pin connector sections F and H

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	e	f	g	h
3	Bus A dc+	Bus A dc–		GND
4	Bus A–	Bus B–	Bus A+	Bus B+
5	+5 V		Bus B dc+	Bus B dc–

Figure 17-22—Optional MIL-STD-1553 B I/O for SEM-E Stretch 372-pin connector section D

17.3.3 Central arbiter definition

For central arbiter modules, most of the locations previously reserved for user-defined I/O are redefined to support central arbitration. These locations are distributed across connector sections E, F, G, and H. Arbitration lines are assigned starting with section F, then E, then G, and finally H.

Each SEM-E Stretch configuration supports a different number of modules, depending upon the number of arbitration lines required and the number of unused connector pins. Each bus of a Dual Futurebus+ module requires three unique lines: **1-RQ0*, 1-RQ1*, and 1-GR*, or 2-RQ0*, 2-RQ1*,** and **2-GR***. When all unused connector pins are assigned to central arbitration this module will support 15 external modules. Each Error Correcting configuration module requires seven unique lines: **RQ0*, RQA0*, RQB0*, RQ1*, RQA1*, RQB1*,** and **GR***. When all unused connector pins are assigned to central arbitration this module will support 12 external modules. Both the Single 32-bit Futurebus+ and the Single 64-bit Futurebus+ require only three unique lines for each module: **RQ0*, RQ1*,** and **GR***. These modules easily support the full 31 modules specified by IEEE Std 896.2-1991. The Space Profile Working Group only simulated systems up to 15 slots in size. If a larger configuration is planned, sufficient simulation to guarantee operation needs to be done prior to implementation.

Note that the Dual Bus central arbiter slot can accept either Dual Bus or Single 32-bit Futurebus+ Profile S central arbiter modules. Like the Dual Bus configuration, the Error Correcting configuration can also use Single 32-bit Profile S central arbiter modules, but the error correcting functionality on the Error Correcting configuration modules must be disabled. Single Futurebus+ central arbiter slots can only be occupied by Single Futurebus+ central arbiters, but 32-bit and 64-bit central arbiters will properly operate in a 64-bit backplane, and 32-bit central arbiters will properly operate in a 32-bit backplane.

Figures 17-23 through 17-25 show the central arbitration assignments for all SEM-E Stretch configurations. Note that all central arbiter signals are active low.

The Central Arbiter function for each of the two buses of a Dual Futurebus+ configuration may either be combined into a single slot or spread across two slots. If combined, then Figure 17-23 shall be used to assign the pins. If separate, then Figure 17-25 shall be used to assign the pins for each bus. This allows the same Central Arbiter Module Type to be used for each module. Additionally, more than one slot per bus may be occupied by a central arbiter module. In this case, only one module shall be actively driving Central Arbiter grants (**GR-x***) and preempt (**PE*** during reset) at a time. Others on the same bus must be disabled and tristated or powered off. When redundancy is used, stub lengths and spacings for the **RQ0-x*, RQ1-x*, and GR-x*** for each bus shall be maintained. In a single central arbiter per bus system, these signals have no stub length requirements since they are wired point to point.

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	a	b	c	d	e	f	g	h
1		1-RQ1-10*		1-RQ0-10*				
2		1-RQ1-11*	1-GR-10*	1-RQ0-11*				
3	1-RQ0-12*	1-RQ1-12*	1-GR-11*					
4	1-RQ0-13*	1-GR-13*	1-GR-12*	1-RQ1-13*				
5		1-GR-14*	1-RQ0-14*	1-RQ1-14*		2-RQ0-14*	2-GR-14*	2-RQ1-14*
6	1-RQ1-5*		1-RQ0-5*		2-RQ1-13*	2-RQ0-13*	2-GR-13*	
7					2-RQ1-12*	2-GR-11*	2-GR-12*	2-RQ0-12*
8						2-GR-10*	2-RQ1-11*	2-RQ0-11*
9					2-RQ0-10*	2-GR-9*	2-RQ1-10*	
10					2-RQ0-9*		2-RQ1-9*	2-GR-8*
11								
12								
13								
14								
15	1-RQ0-6*		1-GR-5*		2-RQ0-8*		2-RQ1-8*	
16								
17							2-GR-7*	
18							2-RQ1-7*	
19								
20								
21					2-GR-6*		2-RQ0-7*	
22								
23								
24								
25								
26								
27								
28								
29								
30								
31								
32								
33					2-RQ0-6		2-RQ1-6*	
34								
35								
36	1-GR-6*		1-RQ1-6*		2-RQ1-5*		2-GR-5*	
37								
38								
39								
40		1-RQ0-7*						
41	1-GR-7*	1-RQ0-8*	1-RQ1-7*					
42	1-GR-8*		1-RQ1-8*				2-RQ0-5*	
43		1-GR-9*	1-RQ0-9*	1-RQ1-9*				
44	1-RQ1-0*	1-GR-0*	1-RQ0-0*					
45	1-RQ1-1*	1-RQ0-2*	1-RQ0-1*	1-GR-1*	2-RQ1-4*	2-GR-3*	2-GR-4*	2-RQ0-4*
46		1-RQ0-3*	1-RQ1-2*	1-GR-2*		2-GR-2*	2-RQ1-3*	2-RQ0-3*
47	1-GR-3*	1-RQ0-4*	1-RQ1-3*		2-RQ0-2*	2-GR-1*	2-RQ1-2*	
48	1-GR-4*		1-RQ1-4*		2-RQ0-1*	2-RQ1-0*	2-RQ1-1*	2-GR-0*
49					2-RQ0-0*			
50								

Figure 17-23—Maximum central arbiter definition for SEM-E Stretch 372-pin Dual Futurebus+

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	a	b	c	d	e	f	g	h
1		RQ0-10*		RQA0-10*				
2		RQ1-10*	GR-10*	RQB0-10*				RQB0-12*
3	RQA1-10*	RQB1-10*	GR-11*		RQA1-12*	RQB1-12*	RQA0-12*	
4	RQ0-11*	RQA0-11*	RQB0-11*	RQ1-11*	RQ1-12*	GR-12*	RQ0-12*	RQB1-9*
5		RQA1-11*	RQB1-11*	GR-9*		RQA0-9*	RQB0-9*	RQA1-9*
6	RQ0-2*		RQA0-2*		RQ1-1*	RQ0-1*	GR-1*	
7					RQB1-0*	RQA1-0*	RQ1-0*	RQB0-0*
8				RQB0-2		GR-0*	RQ0-0*	RQA0-0*
9					RQB0-1*	RQA1-1*	RQB1-1*	
10					RQA0-1*		RQ1-9*	GR-2*
11								
12								
13								
14								
15	RQ1-2*		RQA1-2*		RQ0-9*		RQB1-8*	
16								
17							RQA1-8*	
18							RQ1-8*	
19								
20								
21					RQA0-8*		RQB0-8*	
22								
23								
24								
25								
26								
27								
28								
29								
30								
31								
32								
33			RQB1-2*		GR-8*		RQ0-8*	
34								
35								
36	GR-3*		RQ0-3*		RQA1-7*		RQB1-7*	
37								
38								
39								
40		RQA0-3*						
41	RQB0-3*	RQ1-3*	RQA1-3*					
42	GR-4*		RQB1-3*				RQ1-7*	
43		RQ0-4*	RQA0-4*	RQB0-4*				
44	RQ1-4*	RQA1-4*	RQB1-4*					
45	RQ0-5*	RQA0-5*	RQB0-5*	GR-5*				
46		RQ1-5*	RQA1-5*	RQB1-5*				
47	GR-6*	RQ0-6*	RQA0-6*					
48	RQ1-6*		RQA1-6*		RQ0-7*	RQA0-7*	RQB0-7*	GR-7*
49					RQB1-6*			
50								

Figure 17-24—Maximum central arbiter definition for SEM-E Stretch 372-pin Error Correcting configuration

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	a	b	c	d	e	f	g	h
1		RQ1-28*		RQ0-28*		RQ0-30*		RQ1-30*
2		RQ1-27*	GR-28*	RQ0-27*		GR-30*		
3	RQ0-26*	RQ1-26*	GR-27*					
4	RQ0-25*	GR-25*	GR-26*	RQ1-25*				
5		GR-24*	RQ0-24*	RQ1-24*		RQ0-29*	GR-29*	RQ1-29*
6	RQ1-23*		RQ0-23*		RQ1-13*	RQ0-12*	GR-13*	
7					RQ1-12*	GR-11*	GR-12*	RQ0-12*
8						GR-10*	RQ1-11*	RQ0-11*
9					RQ0-10*	GR-9*	RQ1-10*	
10					RQ0-9*		RQ1-9*	GR-8*
11								
12								
13								
14								
15	RQ0-22*		GR-23*		RQ0-8*		RQ1-8*	
16								
17							GR-7*	
18							RQ1-7*	
19								
20								
21					GR-6*		RQ0-7*	
22								
23								
24								
25								
26								
27								
28								
29								
30								
31								
32								
33					RQ0-6*		RQ1-6*	
34								
35								
36	GR-22*		RQ1-22*		RQ1-5*		GR-5*	
37								
38								
39								
40		RQ0-21*						
41	GR-21*	RQ0-20*	RQ1-21*					
42	GR-20*		RQ1-20*				RQ0-21*	
43		GR-19*	RQ0-19*	RQ1-19*				
44	RQ1-18*	GR-18*	RQ0-18*					
45	RQ1-17*	RQ0-16*	RQ0-17*	GR-17*	RQ1-20*	GR-19*	GR-20*	RQ0-20*
46		RQ0-15*	RQ1-16*	GR-16*		GR-18*	RQ1-19*	RQ0-19*
47	GR-15*	RQ0-14*	RQ1-15*		RQ0-18*	GR-17*	RQ1-18*	
48	GR-14*		RQ1-14*		RQ0-17*	RQ1-16*	RQ1-17*	GR-16*
49					RQ0-16*			
50								

Figure 17-25—Maximum central arbiter definition for SEM-E Stretch 372-pin Single 32-bit and Single 64-bit Futurebus+

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17.3.4 Power pin assignments

All connector sections shall be utilized for supplying digital power to Profile S SEM-E Stretch modules. Connector sections E, F, G, and H shall be utilized for supplying digital ground to Profile S SEM-E Stretch modules in all configurations. Connector sections C and D shall also be used to supply power and ground in non-fiber applications. The power pin assignments for the connector sections shall be as shown in Figure 17-26. If unused on the module, these pins shall remain reserved.

Table 17-4 lists the required (+28 V, +5 V, +2.1 V, and +3.3 V) power pins per voltage level and ground pins for the SEM-E Stretch module. Wiring of +28 V, +5 V, +2.1 V and +3.3 V in the backplane is required. Support of these voltages on the modules, beyond maintaining the required pin assignments, is optional. Additional power pins may be implemented on connector sections E, F, G, and H if appropriate keying definitions are created.

Table 17-4—Required power pins per voltage level for module SEM-E Stretch

Voltage	Number of pins
+5 V	8
+5 V US	2
+3.3 V	8
+3.3 V US	2
2.1 V	2
+28 V	4
28 V-RTN	4
GND (5 V, 3.3 V and 2.1 V RTN)	28

The +28 V supplies have been labeled A and B in case independent supplies are provided. A module may use power from either +28 V supply or both. A module shall treat the two supplies as separate power sources and provide separate return paths to the appropriate return signals.

Two +5 V and two +3.3 V pins have been designated as unswitched power inputs, **5 V US** and **3.3 V US**. If there is any power switching in the system, then these signals shall be used to pass unswitched power to the module separate from the switched power passed on the other **+5 V** and **+3.3 V** power inputs in order to power specific elements continuously (such as clocks or non-volatile memory). Both switched and unswitched power returns shall use 0 V (**GND**). If a module is always powered it shall only use the switched power pins.

The pin assignments for power and ground for all SEM-E Stretch implementations are given in Figure 17-29.

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	a	b	c	d	e	f	g	h
1								
2	GND				GND			
3				GND				GND
4								
5	+5 V				+5 V			
6				+3.3 V				+3.3 V
7								
8	GND				GND			
9				+5 V				+5 V
10								
11	+3.3 V				+3.3 V			
12				GND				GND
13								
14	+5 V US				+5 V US			
15				GND				GND
16								
17	+5 V				+3.3 V			
18				GND				GND
19								
20	+28 V A				+28 V B			
21				+28 V A RTN				+28 V B RTN
22								
23	GND				GND			
24				+2.1 V				+2.1 V
25								
26								
27								
28	GND				GND			
29				+28 V A RTN				+28 V B RTN
30								
31	+28 V A				+28 V B			
32				GND				GND
33								
34	-15 V				-15 V			
35				GND				GND
36								
37	+3.3 V US				+3.3 V US			
38				GND				GND
39								
40	+5 V				+5 V			
41				+3.3 V				+3.3 V
42								
43	GND				GND			
44				+5 V				+5 V
45								
46	+3.3 V				+3.3 V			
47				GND				GND
48								
49	GND				GND			
50								

Figure 17-26—Power pin assignments for module SEM-E Stretch

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17.3.5 Connector keying

Keying is a required feature used to avoid interoperability conflicts between Profile S modules, or between modules that belong to different profiles but have compatible mechanical characteristics. Keying puts constraints on which modules can be inserted into which slots. Keying is necessary where a backplane has been built with slot-unique characteristics. Keying is also necessary when non-896.10 electrical compliant drivers may assert signals on user defined lines. Each 372-pin SEM-E Stretch module shall contain three keying pins: alpha, beta, and gamma (referenced and defined in EIA IS E700A). Each of these keys shall have eight different positions. The alpha key shall be located at the end of the connector labelled with the lowest row number. The beta key shall be located at the end of the connector labelled with the highest row number. The gamma key shall be located in the middle support of the connector. All SEM-E Stretch modules shall use keying. It is required that matching keying is used on all Profile S SEM-E Stretch Backplanes although the absence of such keying is allowed in a lab environment at a degraded level (single bus) for demonstrations and concept proving activities.

The alpha key shall be used to represent the bus size and configuration. The keys used shall be

Position A: 32-Bit Single Futurebus+
Position B: 32-Bit Dual Futurebus+
Position C: 32-Bit Error Correcting configuration
Position D: 64-Bit Single Futurebus+
Position E–H: Reserved

The beta key shall be used to represent the various options present: The keys used shall be

Position A: No options present
Position B: MIL-STD-1553B present
Position C: Central Arbiter present
Position D: MIL-STD-1553B and Central Arbiter present
Position E-H: Reserved

The gamma key shall be reserved for vendor applications.

17.3.6 EMI shield pins

The EMI shield of the 372 pin connector provides 20 solder pins (designated Y1 to Y10 and Z1 to Z10). These 20 pins shall be tied to the ground of the backpanel.

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Annex A

(informative)

Bibliography

[B1] MIL-HDBK-217E, Reliability Prediction for Electronic Equipment, United States Air Force, 1991.

[B2] MIL-HDBK-217F, Reliability Prediction for Electronic Equipment, United States Air Force, Notice 1990.

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